OPERATING AND SERVICE MANUAL

8662A Synthesized Signal Generator

10 kHz — 1280 MHz



Volume 2

Manual Changes
Service
- Block Diagrams
- Schematics
- Principles of Operation
- Troubleshooting
- Component Locations
- Disassembly

HEWLETT PACKARD

MANUAL CHANGES

MANUAL IDENTIFICATION

Model Number: 8662A
Date Printed: December 1982
Part Number: 08662-90062

SYNTHESIZED SIGNAL GENERATOR OPERATING AND SERVICE MANUAL VOLUME 2

This supplement contains important information for correcting manual errors and for adapting the manual to instruments containing improvements made after the printing of the manual.

To use this supplement, make all ERRATA corrections first, then incorporate all appropriate serial number related changes indicated to the tables below.

SERIAL PREFIX OR NUMBER	MAKE MANUAL CHANGES
1830A-2114A	Errata Only
2128A	1-3
2132A	1-4
2136A	1-5
2138A	1-6
2145A	1-8
2148A	1-9
2151A	1-10
2201A	1-11
2222A	1-12
2224A	1-13

SERIAL PREFIX OR NUMBER	MAKE MANUAL CHANGES
2232A	1-14
2237A	1-15
2240A	1-16
2242A	1-17
2244A	1-18
2301A, 2302A	1-19
2322A	1-20

>> NEW ITEM

NOTE:
Manual change supplements are revised as often as necessary to keep manuals as current and accurate as possible. Hewlett-Packard recommends that you periodically request the latest edition of this supplement. Free copies are available from all HP offices. When requesting copies, quote the manual identification information from your supplement or the model number and print date from the title page of the manual.

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13 July 1983
11 Text Pages
8 Illustrations

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SUMMARY OF COMPONENT CHANGES BY SERVICE SHEET

NOTE

The information in each column is in following order: Service Sheet, Reference Designation, and Change Number or Errata (E).

C	A6A3	(6)	22	(A6A9)		40	(A4A9)	
				R8	(16)		CR9	(17)
D	A6A6	(6)		R9	(16)		R60	(9)
							R61	(9)
E	A4A2	(4)	23	(A6A6)			R62	(9)
				R3	(6)		U9	(17)
6	A2A6	(10)		R5	(6)			
	C1	(13)		R7	(6)	41	(A5A4)	
	C7	(10)					C6	(E)
	C14	(10)	30	(A4A4)				
	DL1	(10)		C26,28	(14)	43	(A5A5)	
	R7	(13)		C36,38	(14)		R1-R6	(16)
	R29,30,31	(10)		R49	(E)			
	U2	(10)				44	(A5A2)	
	VR1	(10)	32	(A4A3)	(15)		R13-R18	(16)
				L4, L6	(15)		R19-R21	(16)
7	A2A6	(10)						
			33	A4A2	(4)	45	(A5A1)	
11	A1A1	(5)		CR3	(17)		R1-R12	(16)
				R9, R10	(16)			
16	(A2A2)			U5	(17)	50	(A3A6)	
	CR6	(17)					R1,R3,R4	
	U5	(17)	34	(A4A1)			R7,R8,	
				L8	(15)		R10,R11	
18	A8A3	(8)					R14,R15,	
			36	(A3A1)			R20,R21,	
	A8A4	(7,E)		R17	(E)		R24,R25,	
	C11	(7)					R27,R28,	
	C28	(7)	37	(A4A7)			R30	(16)
	CR4	(7)		C25	(E)			
	R9	(7)		C26	(E)	52	(A3A9)	
	U2	(7)		C38	(E)		L5	(E)
	VR1	(7)		CR2	(17)		L7	(E)
				U8	(17)		L8	(E)
19	(A6A1)							
	R46		39	(A4A6)		57	(A7A2)	
				R4	(E)		C34	(7)
20	A6A3	(6)					C35	(7)
	R78,79	(6)					Q4	(7)
	R80	(6)						

ERRATA

Page 7-16, CHANGE D:
Service Sheet 34 (Schematic):
Change entry for C59 to read "Remove capacitor C59, 100 pF, between R19 and ground."

Page 7-17, CHANGE G:
Service Sheet 51 (Schematic):
Add following entry "Remove asterisk (*) from R5 and change typical value to 6180 ohms.

Page 7-18, CHANGE M:
Service Sheet 39 (Schematic):
Change value of C24 to 10 pF.
Change entry for attenuator network to read "Remove attenuator network consisting of R56*, R57*, and R58* from between junction of L4 and C24 and pin 1 of U2.
Service Sheet 55 (Schematic):
Change entry for R14 and C7 to read "Add R14, 5.6 ohms and C7, 0.056 uF in series across T3 pins 5 and 7.

Page 7-25, CHANGE S:
Service Sheet 5 (Schematic):
Add following entries:
In table entitled "Integrated Circuit Part Numbers", change part number of U10 to 08662-80015 and U11 to 08662-80016.
In table entitled "Reference Designations" under A2A5, change C1-9 to read "C1-7" and R1-5 to read "R1-3".
In table entitled "Integrated Circuit Voltage and Ground Connections", change U1-3, 10 to read "U1-3" and U11 to read "U10, 11".

Page 8-313, Service Sheet 6:
A2A6C1; For recommended replacement, refer to CHANGE 13.
A2A6R7; For recommended replacement, refer to CHANGE 13.

Page 8-333, Service Sheet 16:
A2A2U7; For recommended replacement, refer to CHANGE 17.

Page 8-335, Service Sheet 17 (Schematic):
In lower right-hand corner of schematic, change Service Sheet numbers associated with off-page connectors AY and AZ (START/STOP and SPAN respectively) from 1 to 2.

Page 8-402, Service Sheet 18 (Component Locator):
Replace Figure 8-401 with attached **A8A4 Reference Buffer Component Locations.**

Page 8-405, Service Sheet 19 (Schematic):
Change typical value of R46* to 42.2 ohms.

Page 8-410, Service Sheet 22:
A6A9R8 and R9; For recommended replacement refer to CHANGE 16.

Page 8-503, Service Sheet 30 (Schematic):
Change value of R49 to 46.4 ohms.
A4A4C26, C28, C36, C38; For recommended replacement, refer to CHANGE 14.

ERRATA (cont'd)

Page 8-507, Figure 8-509, Service Sheet 32 (Schematic--A4A3):
A4A3L4 and L6; For recommended replacement, refer to CHANGE 15.
>> At 2db pad delete R25 keeping an open circuit between pins 6 and 3.
>> At 2db pad add R25(12.1ohms) between pins 7 and 2.
>> At 4db pad delete R30 keeping an open circuit between pins 6 and 3.
>> At 4db pad add R30(23.7ohms) between pins 7 and 2.
>> At 8db pad delete R35 keeping an open circuit between pins 6 and 3.
>> At 8db pad add R35(56.2ohms) between pins 7 and 2.
Page 8-509, Service Sheet 33:
A4A2R9 and R10; For recommended replacement, refer to CHANGE 16.
A4A2U5; For recommeded replacement, refer to CHANGE 17.
Page 8-511, Service Sheet 34:
A4A1L8; For recommended replacement, refer to CHANGE 15.
Page 8-513, Service Sheet 35 (Schematic):
In lower left-hand portion of schematic, upper end of R55 is shown connected to +5.2V. Change this value to +5V.
>> Page 8-514, Figure 8-519 (Component Locator):
On Figure 8-519. Reverse Power Driver Component Locations, C9 is located below C6 and between R15 and Q1.
Page 8-515, Service Sheet 36 (Schematic):
Add an asterisk (*) to R17 and change its typical value to 51.1k.
Page 8-517, Figure 8-524, Service Sheet 37 (Schematic--A4A7):
>> In AGC Loop Gain Amplifier change Jumper Wire note to (note 2).
Change value of C25* to 0.022 uF.
Delete value shown for C38* (0.022 uF).
Change value of C26* to 0.015 uF.
A4A7U8; For recommended replacement, refer to CHANGE 17.
>> Page 8-519, Figure 8-529, Service Sheet 38 :
In INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS table change U6 to +5v(F2).
Page 8-521, Figure 8-532, Service Sheet 39 (Schematic--A4A6):
>> Change value of R4* to 5.62K.
>> Change value of R7* to 5.11K.
>> Change value of R29* to 3.83K.
>> Change value of R32* to 2.87K.
Change typical value of R4* to 5.11k.
Page 8-523, Service Sheet 40:
A4A9U9; For recommended replacement, refer to CHANGE 17.>> Page 8-627, Figure 8-644, Service Sheet 53 (Schematic--A3A10):
Change value of C9 to 110pf.
>> Page 8-637, Figure 8-658, Service Sheet 57 (Schematic--A7A2):
Change value of R37 to 21.5K ohms.
Page 8-603, Service Sheet 41 (Schematic):
Add an asterisk (*) to C6 and change its typical value to 470 pF.
Page 8-606, Service Sheet 43:
A5A5R1-R6; For recommended replacement, refer to CHANGE 16.
Page 8-608, Service Sheet 44:
A5A2R13-R18; For recommended replacement, refer to CHANGE 16.
A5A2R19-R21; For recommended replacement, refer to CHANGE 16.
Page 8-610, Service Sheet 45:
A5A1R1-R12; For recommended replacement, refer to CHANGE 16.

ERRATA (cont'd)

Page 8-615, Service Sheet 47:

A3A3R1-R8; For recommended replacement, refer to CHANGE 16.

Page 8-620, Service Sheet 50:

A3A6R1, R4, R8, R11, R15, R21, R25, and R28; For recommended replacement, refer to CHANGE 16.

A3A6R14; For recommended replacement, refer to CHANGE 16.

A3A6R3, R7, R10, R20, R24, R27, and R30; For recommended replacement, refer to CHANGE 16.

Page 8-625, Service Sheet 52 (Schematic):

Change values of L5 and L7 to 68 nH.

Change value of L8 to 51 nH.

Page 8-631, Service Sheet 55 (Schematic).

At far left-hand edge of schematic, change wire color code given for upper conductor of W57 (connected to 115V side of S2) from "1" to "0".

Page 8-637, Service Sheet 57 (Schematic):

Under reference designator for Q4 add "(NOTE 2)".

Add following to NOTES:

"2. If Q4 is replaced, a ferrite bead (E1) should be added to its base."

CHANGES 1-3:

Changes 1-3 do not apply directly to Volume 2.

CHANGE 4

Page 8-219, Service Sheet E (Block Diagrams):
In Block Diagram 33, add an amplifier symbol (that is,) in series with line running from FILTER TUNING D/A CONVERTER to bandpass filter in A4U3 MODULATOR. Label this amplifier MODULATOR-FILTER TRACKING AMPLIFIER.

Page 8-508, Service Sheet 33 (Principles of Operation):
Replace two paragraphs and NOTE entitled **Filter Tuning D/A Converter** with following:

Filter Tuning Circuitry

The tune voltages for two voltage-tuned filters, one in Doubler-Filter U2 and other in Modulator-Filter U3, are developed by ROM U4 and D/A Converter U5 working in conjunction with Doubler-Filter Tracking Amplifier U1A and Modulator-Filter Tracking Amplifier U1B.
Information for automatic correction of tuning curves for each of voltage-tuned filters is stored in ROM U4. This information is used to determine which frequencies will be passed or rejected by two voltage-tuned filters. Each filter can be programmatically advanced in 2 MHz steps from 640 MHz to 1280 MHz. The actual frequency selection signals that address data stored in ROM come from DCU. The ROM output is enabled at same time as doubler in U2. Although addresses that select ROM outputs to D/A Converter cannot be listed in a truth table, ROM address lines can be incremented by placing instrument in sweep mode. Verification can be made by stepping frequency in 2 MHz increments from 640 MHz to 1280 MHz while monitoring doubler band output on a spectrum analyzer at J2. It should be noted that frequency will still increment even if filter is not working.

/!\ | CAUTION |

The output of J2 is at a dc level of about +12 Vdc. Some spectrum analyzers are dc coupled and cannot be connected directly to this output. If input of spectrum analyzer is dc coupled, a blocking capacitor adapter must be used in series with input or damage will occur.

CHANGE 4 (cont'd)

Page 8-508, Service Sheet 33 (Principles of Operation) (cont'd):

NOTE

Anytime either one or both of microcircuits U2 or U3 are replaced, a new ROM U4 must also be replaced. Any non-linearities that exist within two microcircuits are accounted for when ROM is programmed. The data stored in ROM is unique to two microcircuits, therefore, a new ROM must be programmed whenever either microcircuit is replaced.

Transistor Q3 forms a constant reference voltage source which can be adjusted by DOUBLER-FILTER TRACKING HIGH pot R29. This source provides voltage reference to D/A Converter U5 which determines maximum frequency pass band of voltage-tuned filter in Doubler-Filter U2. The ROM output is used by D/A Converter to attenuate this reference voltage and produce a current which will track tuning curves of voltage-tuned filters.

This current is coupled to input of Doubler-Filter Tracking Amplifier U1A where it is converted into tune voltage for voltage-tuned filter in Doubler-Filter U2. The DOUBLER-FILTER TRACKING LOW pot R40 sets lower limit for this tune voltage.

The tune voltage from Doubler-Filter Tuning Amplifier U1A is also coupled to input of Modulator-Filter Tracking Amplifier U1B. The MODULATOR-FILTER TRACKING LOW pot R56 sets lower limit for tune voltage to voltage-tuned filter in Modulator-Filter U3, while MODULATOR-FILTER TRACKING HIGH pot R58 sets upper limit.

Page 8-508, Service Sheet 33 (Component Locations):

Replace Figure 8-510 with attached A4A2 Component Locations.

Page 8-509, Service Sheet 33 (Block Diagrams):

In lower block diagram, add an amplifier symbol (that is, -|>-) in series with line running from FILTER TUNING D/A CONVERTER to bandpass filter in MODULATOR-FILTER. Label this amplifier MODULATOR-FILTER TRACKING AMPLIFIER.

Page 8-509, Service Sheet 33 (Schematic):

Replace appropriate potion of schematic with attached par tial schematic.

In NOTE 2, change part number of exchange PC board to 08662-60309, and delete second sentence regarding partial PC board.

In table entitled "Reference Designations" under A4A2, change C1--18, 23--25, 27--29, 31--33, 35 to read C1--18, 23--25, 27--29, 31--33, 35--38; change R1--55 to read R1--51, 53, 54, 56--62; and change TP1--9 to read TP1--10.

In table entitled "Transistor and Integrated Circuit Part Numbers", change part number of U1 to 1826-0547.

CHANGE 5

Page 8-323, Service Sheet 11 (Schematic):
Change A1A1 READOUT BOARD part number to 08662-60307.

CHANGE 6

Page 8-215, Service Sheet C (Block Diagram):
Change power level at A6A3J4 to -6 dBm.
Page 8-217, Service Sheet D (Block Diagram):
Change power level at A6A6J2 to -6 dBm.
Page 8-407, Service Sheet 20 (Schematic):
Change part number for A6A3 assembly to 08662-60314.
Change value of R78 to 316 ohm.
Add two resistors (R79 and R80) in conjunction with R78 to form a 3 dB Pad. Refer to **P/O Schematic 20, A6A3 HF Multiplier (P/O Change 6).**
Page 8-413, Service Sheet 23 (Schematic):
Change value of R3 and R7 to 316 ohm.
Change value of R5 to 17.8 ohm.
Change value shown for pad consisting of R3, R5, and R7 to 3 dB.
Change power level at J2 to -6 dBm.

CHANGE 7

Page 8-402, Service Sheet 18 (Component Locations):
Replace Figure 8-401 with attached A8A4 Component Locations.
Page 8-403, Service Sheet 18 (Schematic):
Change part number of A8A4 assembly to 08662-60306.
Replace appropriate portion of schematic with attached partial schematic.
In table entitled "Reference Designations" under A8A4, change C1--12, 14--25, 27, to read C1--12, 14--25, 27, 28; change CR1--3 to read CR1--4; change R1--11, 13--42 to read R1--8, 10, 11, 13--42; change U1 to read U1, 2; and delete VR1.
In table entitled "Transistor and Integrated Circuit Part Numbers," add U2 with part number 1826-0275.
Page 8-637, Service Sheet 57 (Schematic):
Add capacitor A7A2C34, 0.01 uF, in parallel with C3.
Add Capacitor A7A2C35, 0.01 uF, in parallel with C18.
In table entitled "Reference Desigations" under A7A2, change C1--33 to read C1--35.

CHANGE 8

Page 8-102, Paragraph 8-10:
Add following sentences before last sentence in paragraph 8-10. "The Operating & Service Manual for A8A3 10 MHz Reference Oscillator, part no. 10811A, is included with each service accessory kit to provide field service and repair information for oscillator. This manual may be ordered separately with part no. 10811-90002."
Page 8-403, Service Sheet 18 (Schematic):
Change part number of A8A3 assembly to 10811A.

CHANGE 9

Page 8-523, Service Sheet 40 (Schematic):
Change value of R60 to 900 ohm.
Delete R61 and connect R60 to R62.
In table entitled "Reference Designations" under A4A9, change R1--84 to read R1--60, 62--84.

CHANGE 10

Page 8-312, Service Sheet 6 (Component Locations):
Replace Figure 8-316 with attached A2A6 Component Locations.
Page 8-313, Service Sheet 6 (Schematic):
Change part number of A2A6 assembly to 08662-60315.
Replace appropriate portion of schematic with attached partial schematic.
In table entitled "Reference Designations" under A2A6:
Change C1-12, 14 to read C1-6, 8-12;
Add DL1;
Change R1-29 to read R1-28, 30, 31;
Change U1, 2, 4-13, 23, 24 to read U1, 4-13, 23, 24;
Delete VR1.
In table entitled "Integrated Circuit Part Numbers," change part number of U1 to 1820-2369 and delete U2 part number.
In table entitled "Integrated Circuit Voltage and Ground Connections," change pin numbers associated with U1 to read +5V -11, 14--16; \/ -1, 8, 9; and NC -10, 12, 13. Also change U2, 4, 9--12 to read U4, 9--12.
Page 8-314, Service Sheet 7 (Component Locations):
Replace Figure 8-319 with attached A2A6 Component Locations.
Page 8-315, Service Sheet 7 (Schematic):
Change part number of A2A6 assembly to 08662-60315.

CHANGE 11

Change 11 does not apply directly to Volume 2.

CHANGE 12

Change 12 does not apply directly to Volume 2.

CHANGE 13

Page 8-313, Service Sheet 6:
Change value of A2A6C1 to 2.2uF.
Change value of A2A6R7 to 121K ohms.

CHANGE 14

Page 8-503, Service Sheet 30:
Change A4A4C26 and A4A4C36 to 16 pF.
Change A4A4C28 and A4A4C38 to 29 pF.

CHANGE 15

Change 15 does not apply directly to Volume 2.

CHANGE 16

Change 16 does not apply directly to Volume 2.

CHANGE 17

Page 8-507, Service Sheet 32:
Change values of A4A3L4 and L6 to 630 uH.
Page 8-511, Service Sheet 34:
Change value of A4A1L8 to 630 uH.

CHANGE 18

Page 8-410, Service Sheet 22:
Change values of A6A9R8 and R9 to 196 ohms.
Page 8-508, Service Sheet 33:
Change values of A4A2R9 and R10 to 562 ohms.
Page 8-606, Service Sheet 43:
Change values of A5A5R1-R6 to 178 ohms.
Page 8-608, Service Sheet 44:
Change values of A5A2R13-R18 to 348 ohms.
Change values of A5A2R19-R21 to 681 ohms.
Page 8-610, Service Sheet 45:
Change values of A5A1R1-R12 to 348 ohms.
>> Page 8-615, Service Sheet 47:
Change values of A3A3R1-R8 to 178 ohms.
Page 8-620, Service Sheet 50:
Change values of A3A6R1, R4, R8, R11, R15, R21, R25, and R28 to 909 ohms.
Change value of A3A6R14 to 681 ohms.
Change values of A3A6R3, R7, R10, R20, R24, R27, and R30 to 2.37K ohms.

CHANGE 19

Page 8-333, Service Sheet 16:
Delete A2A2CR6.
In Transistor and Integrated Circuit Part Numbers table, change U5 to part number 1826-0921.
Page 8-509, Service Sheet 33:
Delete A4A2CR3.
In Transistor and Integrated Circuit Part Numbers table, change U5 to part number 1826-0921.
Page 8-517, Service Sheet 37:
Delete A4A7CR2.
In Transistor and Integrated Circuit Part Numbers table, change U8 to part number1826-0921.
Page 8-523, Service Sheet 40:
Delete A4A9CR9.
In Transistor and Integrated Circuit Part Numbers table, change U9 to part number 1826-0921.

>> CHANGE 20

Page 8-415, Service Sheeet 24:
Change A8A2 part number to 08662-60317

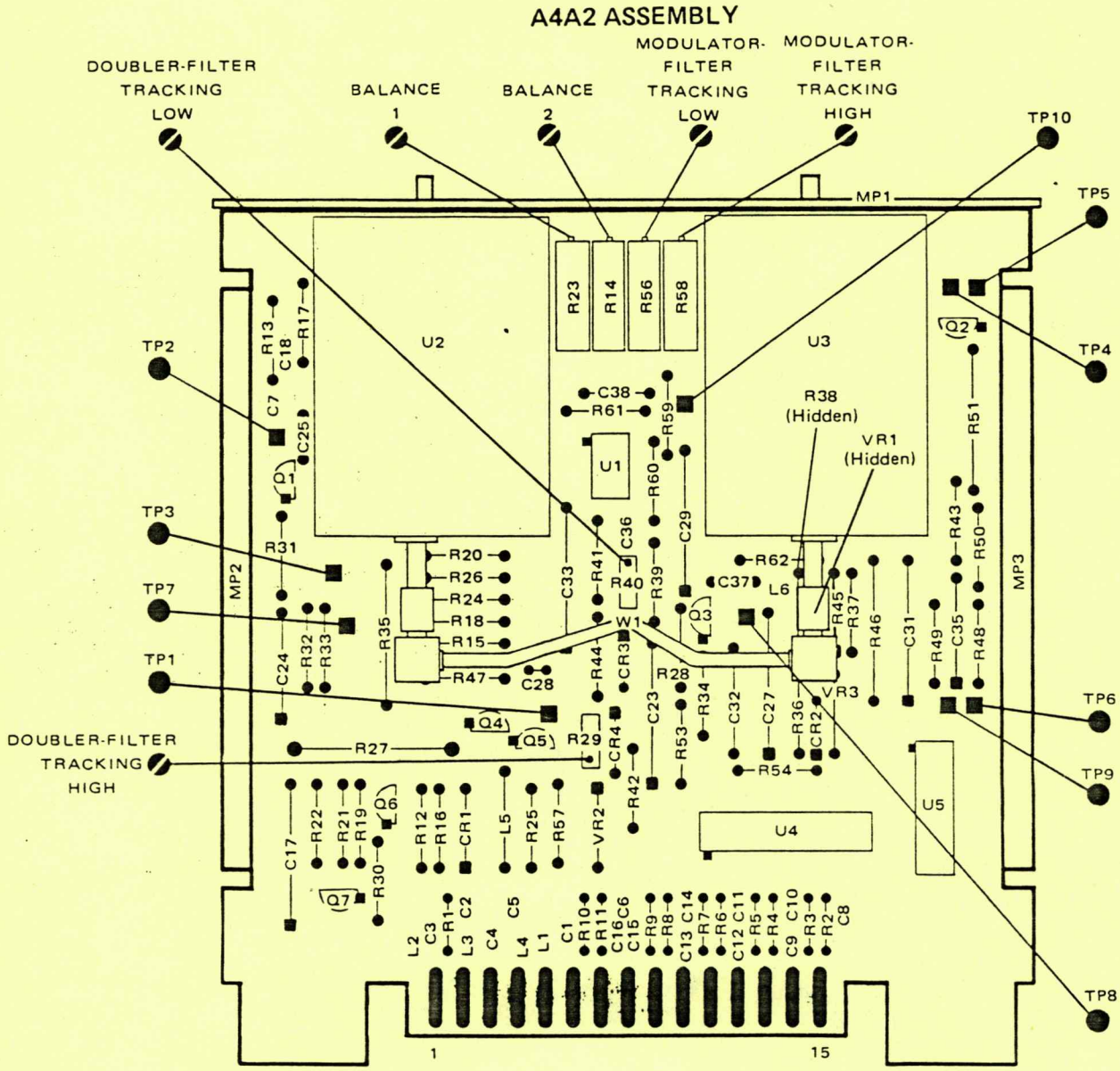
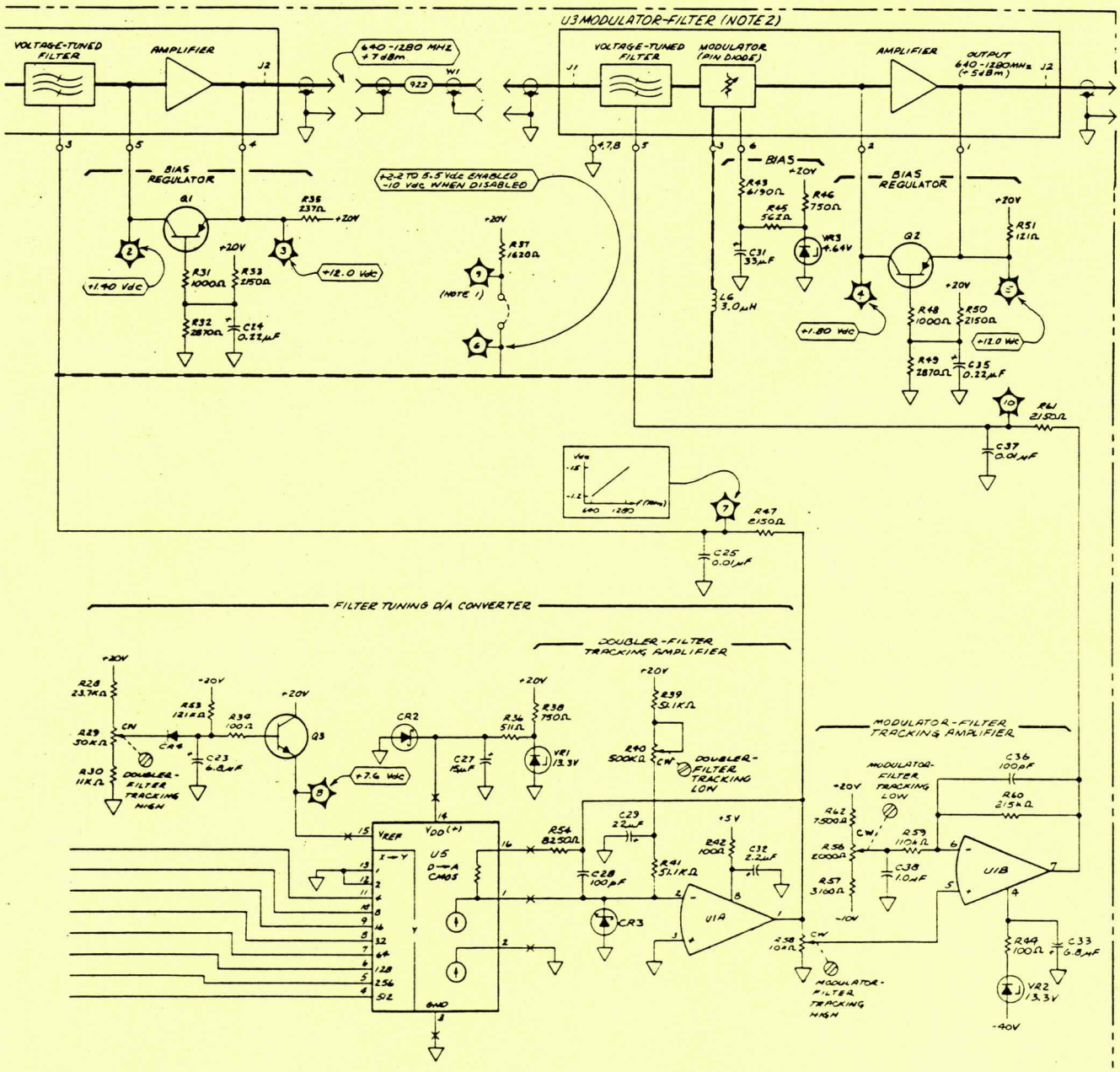
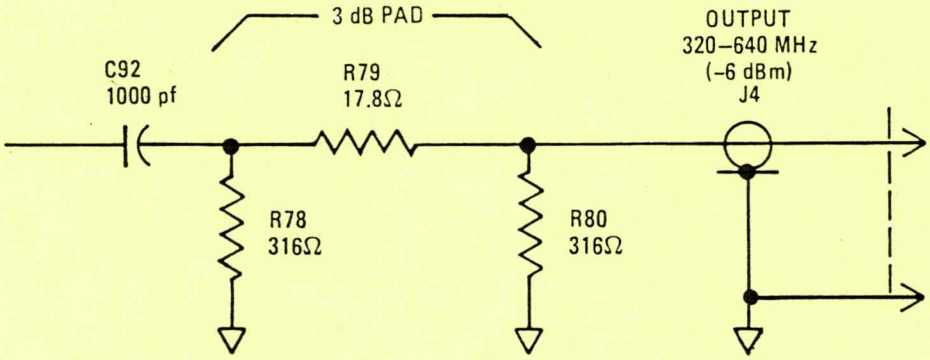


Figure 8-510. A4A2 Output Section Doubler Component Locations (P/O Change 4)



P/O Figure 8-512. A4A2 Output Section Doubler Schematic (P/O Change 4)



P/O Schematic 20, A6A3 HF Multiplier (P/O Change 6)

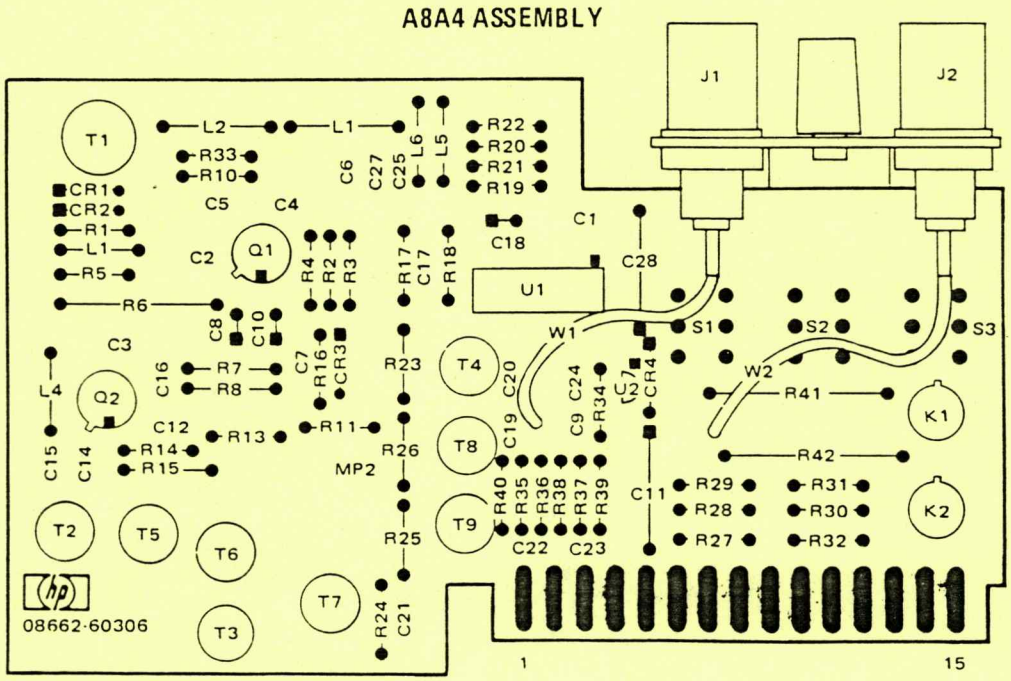
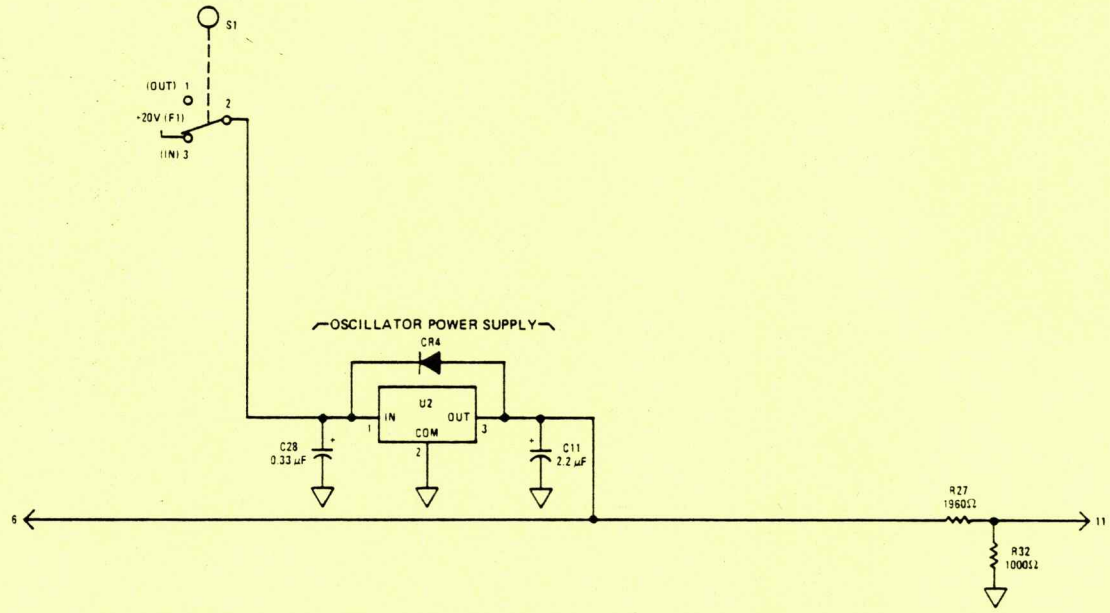


Figure 8-401. A8A4 Reference Buffer Component Locations (P/O Change 7)



P/O Schematic 18, A8A3 and A8A4 10 MHz Reference Oscillator and Buffer (P/O Change 7)

P/O A2A6 ASSEMBLY

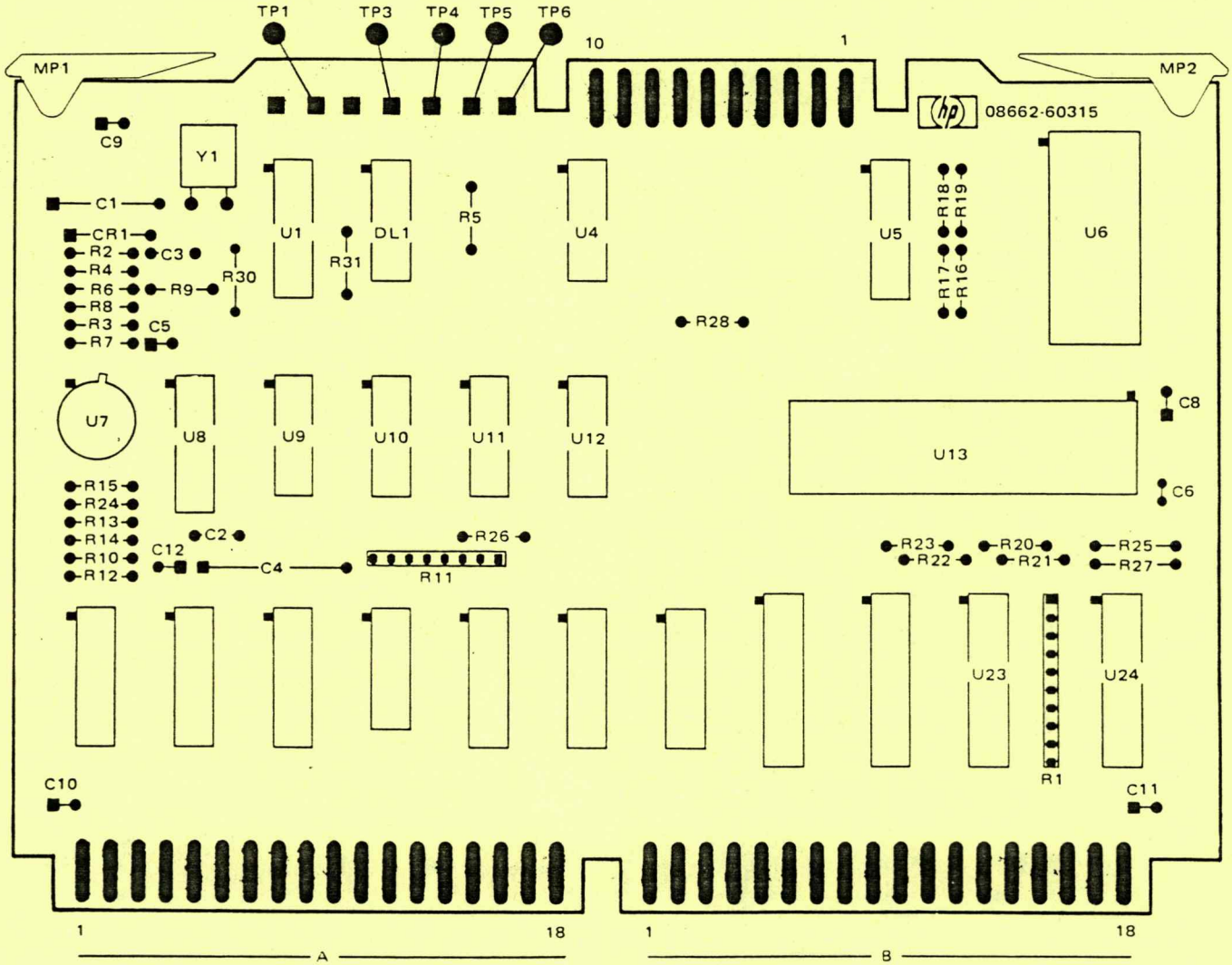
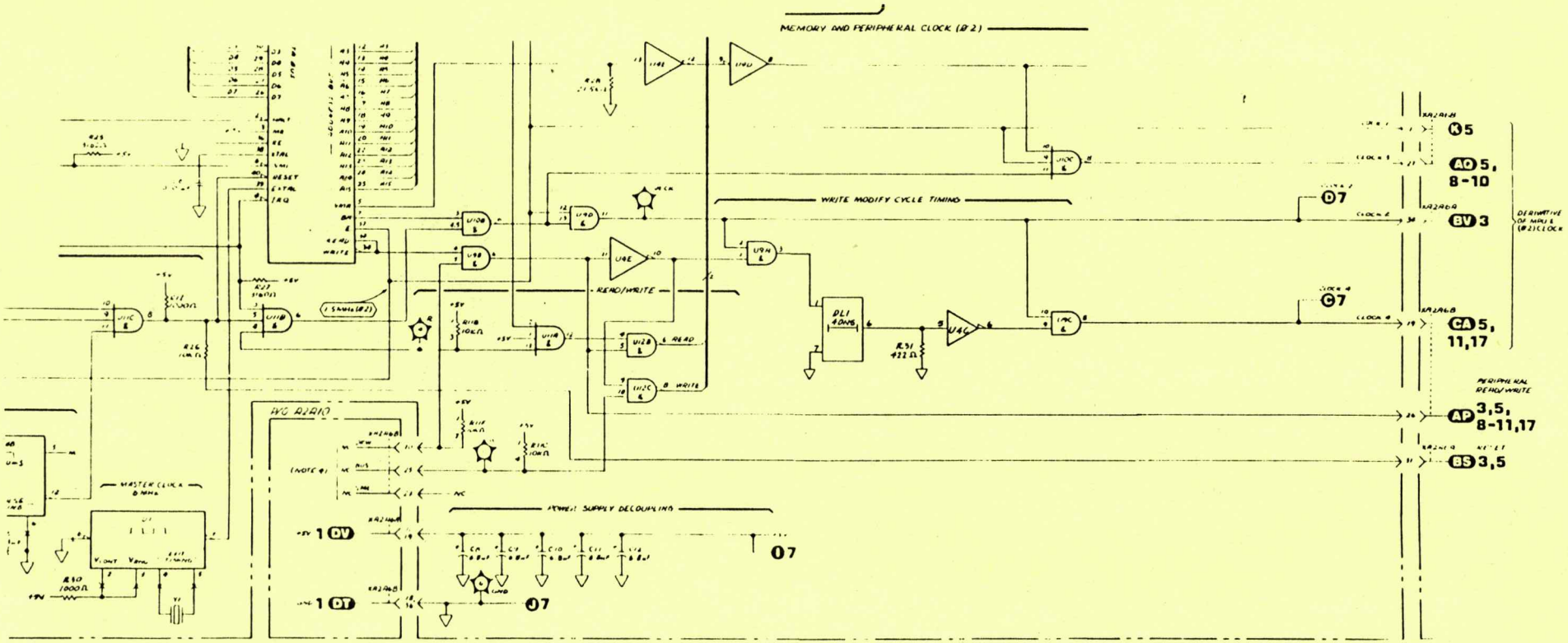


Figure 8-316. P/O A2A6 Microprocessor/Decoder Component Locations (P/O Change 10)



P/O Schematic 6, P/O A2A6 Microprocessor/Decoder (P/O Change 10)

P/O A2A6 ASSEMBLY

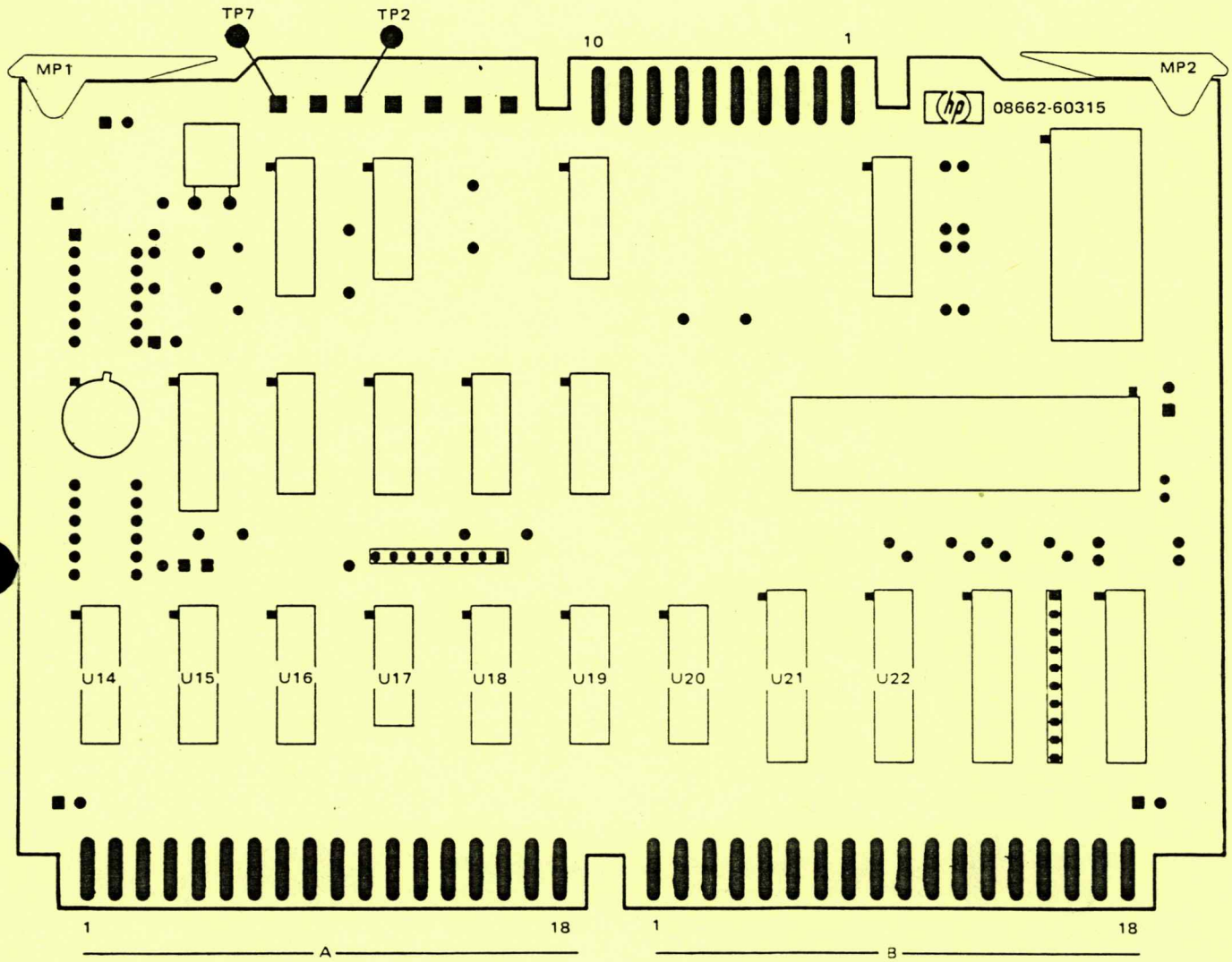


Figure 8-319. P/O A2A6 Microprocessor/Decoder Component Locations (P/O Change 10).

OPERATING AND SERVICE MANUAL
VOLUME 2

8662A
Synthesized Signal Generator
10 kHz — 1280 MHz

SERIAL NUMBERS

This manual applies directly to instruments with serial numbers prefixed 2114A.

For additional important information about serial numbers see INSTRUMENTS COVERED BY MANUAL in Section I of Volume 1.

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CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard instrument product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

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SERVICE MANUAL

8662A Synthesized Signal Generator

10 kHz — 1280 MHz



Section VII
Part 2
Manual Changes

HEWLETT PACKARD

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GENERAL INFORMATION
INSTALLATION
OPERATION

These sections are bound separately in Volume 1 with a separate table of contents.

Sections IV and V
PERFORMANCE TESTS
ADJUSTMENTS

These sections are bound separately in Volume 1 with a separate table of contents.

Sections VI and VII — Part 1
REPLACEABLE PARTS
MANUAL CHANGES — Volume 1

These sections are bound separately in Volume 1 with a separate table of contents.

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SECTION VII — Part 2
MANUAL CHANGES — Volume II

7-3. INTRODUCTION

This section contains manual changes instructions for backdating Volume II of this manual for HP 8662A Synthesized Signal Generators having serial number prefixes lower than 2114A. This section also contains instrument modification suggestions and procedures that are recommended to improve the performance and reliability of your Generator.

7-4. MANUAL CHANGES

To adopt this manual to your instrument, refer to table 7-3 and make all manual changes listed opposite your serial number prefix. The manual changes are listed in serial number prefix sequence and should be made in the sequence listed. Table 7-4 is a summary of changes by service sheet.

If your instrument's serial number prefix is not listed on the title page of this manual or in Table 7-3, it may be documented in a MANUAL CHANGES supplement. For additional important information about serial number coverage, refer to INSTRUMENTS COVERED BY MANUAL in Section I.

Table 7-3. Manual Changes By Serial Number Prefix

Serial Prefix or Number	Make Manual Changes	Serial Prefix or Number	Make Manual Changes
1830A	X to A	1930A	X to M, K
1832A	X to B	1939A	X to N
1833A	X to C	1940A	X to P, N
1835A	X to D	1943A	X to O
1840A	X to E	1946A	X to P
1841A	X to F	2002A	X to Q
1845A	X to G	2020A	X to R
1850A	X to H	2021A	X to S
1902A	X to I	2024A	X to T
1904A	X to J	2026A	X to U
1908A	X to K	2033A	X to V
1925A	X to K	2058A	X to W
1928A	X to L	2107A	X

Table 7-4. Summary of Changes By Service Sheet

Service Sheet No.	Reference Designation	Change No.	Service Sheet No.	Reference Designation	Change No.
B	A2A8	S	31	A4A5C32, R21, R42	D
B1	A2A6	G	32	A4A3R16	R
B2	XA2A2A, A2A6	S	33	A4A2R43	V
B3	A2A5, A2A9	S	34	A4A1C59, R19, R107	D
1	A2A10L1	D	35	A4A1Q4, Q11, Q14	R
3	A2A1C8, A2A1R12	W		A4A1E3	M
4	A2A1U4A, A2A1U11, A2A1C7	B		A4A1C53	D
5	A2A5U11, A2A5C8, A2A5R4, A2A5C9, A2A5R5	S		A4A1C47	B
7	A2A6U16, A2A6TP7	G	36	A3A1C9	T
8	A2A8	S	37	A4A7R83, R86	K
9	A2A9U1, 2, 8	P		A4A7R69, R70	C
	A2A9, A2A9R11, A2A9U1-12	S		A4A7C29	B
	A2A9R11	U		A4A7R56	A
10	A2A7U18, A2A7U20—U22	X	38	A4A8Q3, U6A	J
	A2A7U18—U20, U23, A2A7R6E—H	D	39	A4A6	M
12	A2A4R5	J		A4A6C24, C28, L4, R51, R56—R58	M
14	A2A3R20—R25	S		A4A6C22, C24 L4,	E
15	A2A3	S	41	A5A4C6	D
17	A2A2U10	S	42	A5A3VR3, VR4, R86, R87	J
18	A8A4	Q	46	A3A3C13	G
	A8P1, A8A5J5	X		A3A3C9, L2	V
	A8A4K1, K2, A8A4S1—S3	Q	47	A3A3E1, E2	U
	A8L1	F		A3A3R98, R122	G
19	A6A1R21, R25	N	48	A3A4C23—C25, C26	G
20	A6A3L39, R78	O		A3A4C32	H
	A6A3R23	L		A3A4C22, C23, C25, C26	G
	A6A3R76	I		A3A4CR4—CR6	D
23	A6A6R3, R5, R7	O	51	A3A7C23, C24, C26, C27	G
24	A6A5R34, R156	U	53	A3A10R27	Q
28	A6A4R34, R156	U	54	A3A8R33, R34	L
30	A4A4R61, C57	L	55	A7A3F1, F2	V
	A4A4C27, C28, C32, C37, C38	D		A7A3R14, C7, C12, C13, R15, R16	M

CHANGE A

Service Sheet 37 (schematic):
Change R56 to 12.1 kΩ.

CHANGE B

Service Sheet 4 (Principles of Operation):
In the second paragraph under "Malfunction Detection Circuitry" change the appropriate portions of the third and fourth sentences to read "formed by U4A to produce a 45 ms pulse. If the code at pins 9, 11, 14 and 1 persists for more than 45 ms, . . .".

Service Sheet 4 (Schematic):
Change R11 to 100K.
Change C7 to 1.0 μF.
Change the pulse duration, described in U4A to 45 ms.

Service Sheet 35 (Schematic):
Change C47 to 1.0 μF and add a polarity sign (+).

Service Sheet 37 (Schematic):
Change C29 to 1.0 μF.

CHANGE C

Service Sheet 37 (Schematic):
Change R69 and R70 to 1000Ω.

CHANGE D

Service Sheet 1 (Schematic):
Remove inductor A2A10L1 (on mother board) in series on the 20V supply line between TP4 and the +20V side of C1. Connect the +20V side of C1 to TP4.

Service Sheet 10 (troubleshooting):
Replace the table of RAM Board (A2A7) Signatures with the following table:

RAM Board (A2A7) Signatures

U18-		U19-		U20-		U23-	
1	2H70	1	----	1	0001	1	0000
2	HPP0	2	----	2	383C	2	HC89
3	1293	3	----	3	383A	3	HC89
4	0000	4	----	4	0001	4	52F8
5	0000	5	----	5	----	5	52F8
6	383C	6	----	6	0000	6	UPFH
7	UHUF	7	0000	7	0000	7	UPFH
8	0000	8	822C	8	822A	8	OAFA
9	A756	9	3827	9	822C	9	OAFA
10	7528	10	3C96	10	0001	10	0000
11	2H54	11	HAP7	11	0001	11	5H21
12	0P63	12	383C	12	----	12	5H21
13	6541	13	822A	13	383C	13	7F7F
14	2317	14	0001	14	0001	14	7F7F
15	72H8					15	CCCC
16	0001					16	CCCC
						17	5555
						18	5555
						19	0000
						20	0001

CHANGE D (cont'd)

Service Sheet 10 (Schematic)

Replace the appropriate portion of schematic with the attached partial schematic (Figure 7-3):

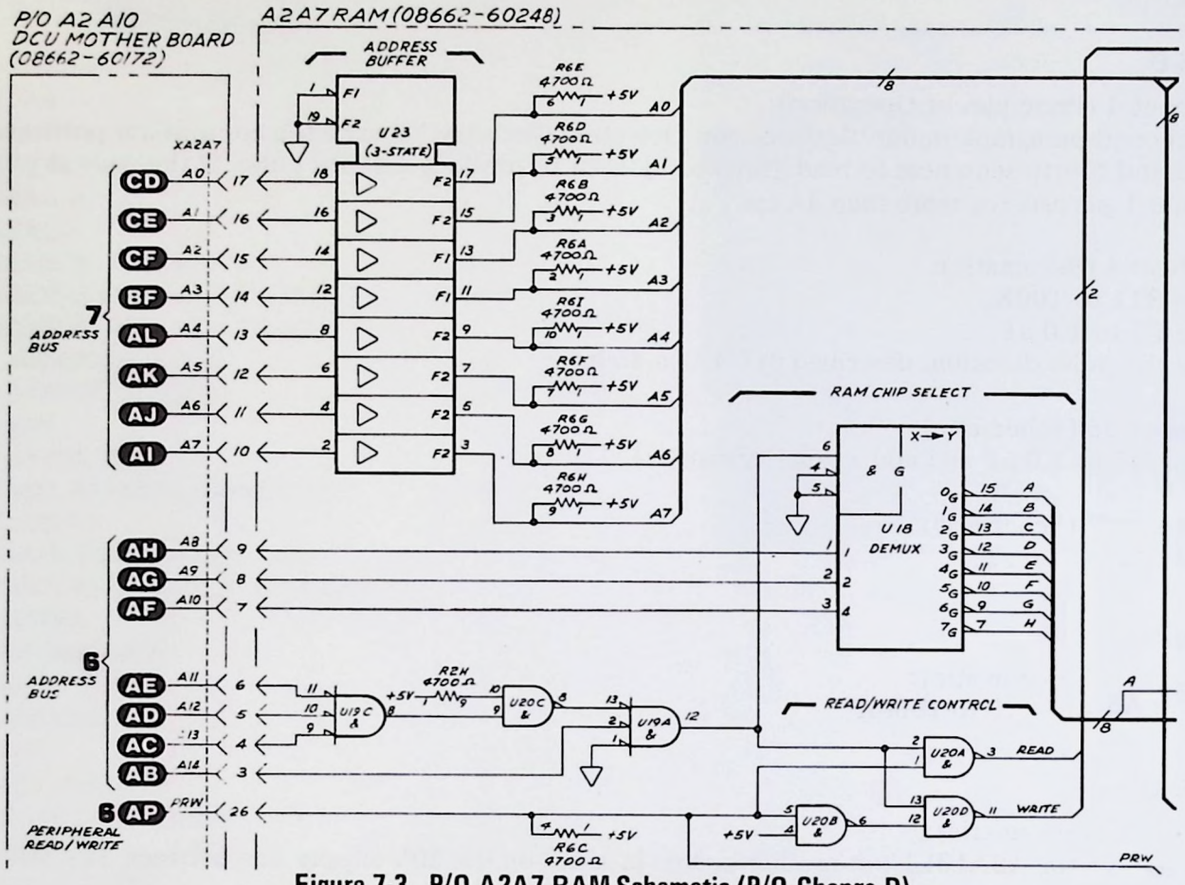


Figure 7-3. P/O A2A7 RAM Schematic (P/O Change D)

Service Sheet 30 (Schematic):

Change C27 and C37 to 22 pF.
Change C28 and C38 to 27 pF.
Change C32 to 33 pF.

Service Sheet 31 (Schematic):

Remove capacitor C32 between R21 and ground. Connect R21 to ground.
Remove resistor R42 between ground and the junction of L19, L8 and R18.

Service Sheet 34 (Schematic):

Remove capacitor C59, 100 pF, between R21 and ground.
Connect R19 from the junction of CR3, CR4 and L14 to ground.
Remove resistor R107, 750Ω.

Service Sheet 35 (Schematic):

Change C53 to 1000 pF.

Service Sheet 41 (Schematic):

Remove C6, 1000 pF capacitor, between the emitter of Q3 and ground.

Service Sheet 48 (Schematic):

Change diodes CR4—6 from simple diodes to Shottky diodes.

CHANGE E

Service Sheet 39 (Schematic):
Change C24 to 24 pF.
Change L4 to 51 nH.
Change the label for the C22-L4-C24 network to "145 MHz LP Filter".

CHANGE F

Service Sheet 18 (Schematic):
Remove inductor A8L1, 500 μH, in series on the 20V supply line between A8C2 and pin 1 of P1. Connect pin 1 of P1 to A8C2.
Delete Note 2.

CHANGE G

Service Sheet B1 (Mainframe Stimulus Diagnostic):
In the table under SET-UP step 5, change the A2A6 entry for CLOCK to U16 pin 15.

Service Sheet 4 (Schematic):
In the table "Integrated Circuit Part Numbers" change U8 to 1820-1442.

Service Sheet 7 (Schematic):
On the line to U16 pin 5, delete TP7.

Service Sheet 46 (Schematic):
Change C13 to 1000 pF.

Service Sheet 47 (Schematic):
Change R98 to 3160Ω.
Remove resistor R122, 38.3 kΩ between pins 2 and 7 of U10.

Service Sheet 48 (Schematic):
Change C22 to 100 pF.
Add capacitors C23, C25, C26, 100 pF, in parallel between the junction of CR7, CR8 and R33 and ground.

Service Sheet 51 (Schematic):
Change C23 to 100 pF.
Add capacitors C24, C26 and C27, 100 pF, in parallel between the junction of CR13, CR14 and R34 and ground.

CHANGE H

Service Sheet 48 (Schematic):
Change C32 to 2.4 pF.

CHANGE I

Service Sheet 20 (Schematic):
Remove resistor R76, 147 kΩ connected from the base of Q3 and −5.11V.

CHANGE J

Service Sheet 12 (Schematic):
Remove 100Ω resistor A2A4R5 from between U17 pin 9 and pin 24 on the output connector. Connect U17 pin 9 directly to pin 24 on the output connector.

CHANGE J (cont'd)

Service Sheet 38 (Schematic):
Remove the ground on U6A pin 2. Connect a line from U6A pin 2 to the collector of Q3.

Service Sheet 42 (Schematic):
Remove diode VR3 connected between pins 4 and 7 of U3 and resistor R86 connected from pin 4 of U3 and −40V(F2). Connect pin 4 of U3 to −40V(F2) and pin 7 of U3 to −10V(F2).
Remove diode VR4 connected between pins 4 and 7 of U6 and resistor R87 connected from pin 4 of U6 and −40V(F2). Connect pin 4 of U6 to −40V(F2) and pin 7 of U6 to −10V(F2).

CHANGE K

Service Sheet 37 (Schematic):
Change R83 to 825Ω.
Change R86 to 7.5 kΩ.

CHANGE L

Service Sheet 20 (Schematic):
Change the part number for the A6A3 assembly to 08662-60112.
Change the value of R23 to 1000Ω.
Remove the PIN diode switch (CR6) and resistor (R77).
Connect diode CR3 to capacitor C31 and R23.

Service Sheet 30 (Schematic):
Remove the RC network (R61 and C57) from the +5V(F2) line. Connect L12 to the junction of L9 and L11.

Service Sheet 54 (Schematic):
Change R33 to 38.3Ω.
Change R34 to 147Ω.

CHANGE M

Service Sheet 35 (Schematic):
Remove the ferrite bead, E3 (⊣/⊢) between the base of Q23 and the junction of C45 and R65.

Service Sheet 39 (Component Locations):
Replace Figure 8-530 with the attached Figure 7-4. A4A6 Component Locations.

Service Sheet 39 (Schematic):
Change C24 to 24 pF.
Change L4 to 100 nH.
Change R51 to 56.2Ω.
Remove C28 from between the junction of C22 and L4 and ground.
Remove the attenuator network consisting of R56*, R57* and R58 from between the junction of L4 and C24.
Connect pin 1 of U2 to the junction of L4 and C24.

Service Sheet 55 (schematic):
Change the part number for A7A3 to 08662-60159.
Add R14, 5.6Ω and C7, 0.056 μF.
Remove the R15-C12 and R16-C13 snubber networks on CR6 and CR7.

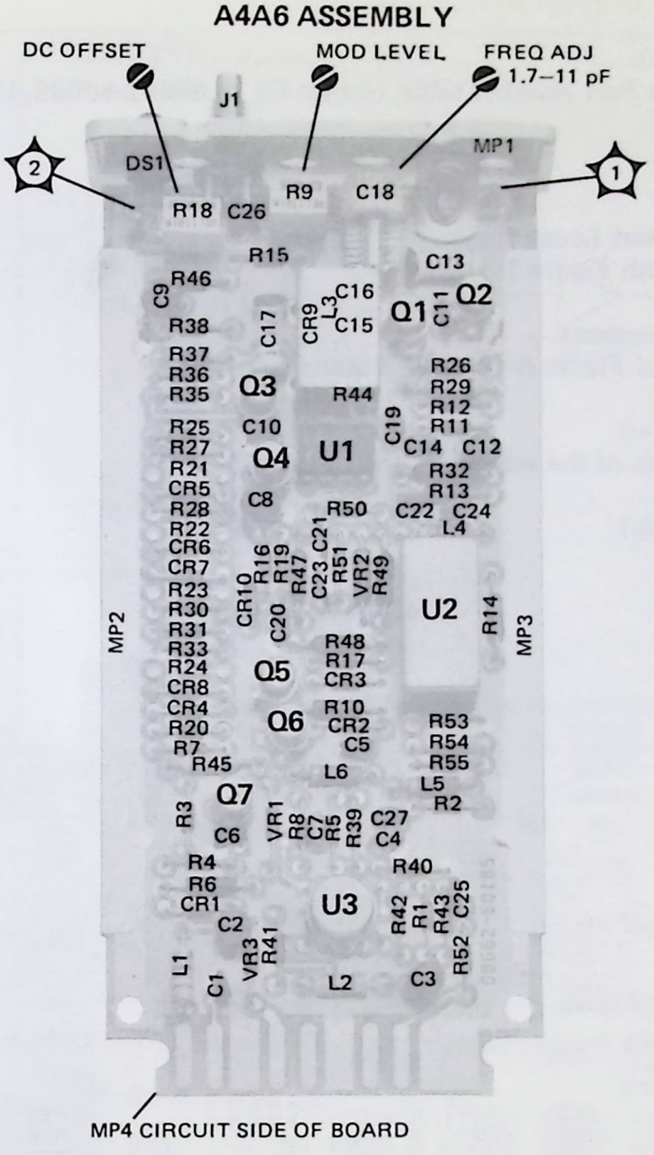


Figure 7-4. A4A6 FM Loop VCO Component Locations (P/O Change M)

CHANGE N

Service Sheet 19 (Schematic):
Change R21 to 1000Ω.
Change R25 to 2870Ω.

CHANGE O

Service Sheet 20 (Schematic):
Change L39 to R70 10Ω.
Remove R78 from between the J4 side of C92 and ground.

Service Sheet 23 (Schematic):
Change the value of R3 and R7 to 316Ω.
Change the value of R5 to 17.8Ω.
Change the value shown for the pad consisting of R3, R5, R7 to 3 dB.

CHANGE P

Service Sheet 9 (schematic):
In the Integrated Circuit Part Number table, change U1 to 08662-80029, U2 to 08662-80030 and U8 to 08662-80036.

CHANGE Q

Service Sheet 18 (Component Locations):
Replace Figure 8-401 with Figure 7-5.

Service Sheet 18 (Block Diagram):
Replace the lower part of Figure 8-402 with Figure 7-6.

Service Sheet 18 (Schematic):
Replace appropriate parts of the schematic with Figure 7-7.

Service Sheet 53 (Schematic):
Change R27 to 2370Ω.

A8A4 ASSEMBLY

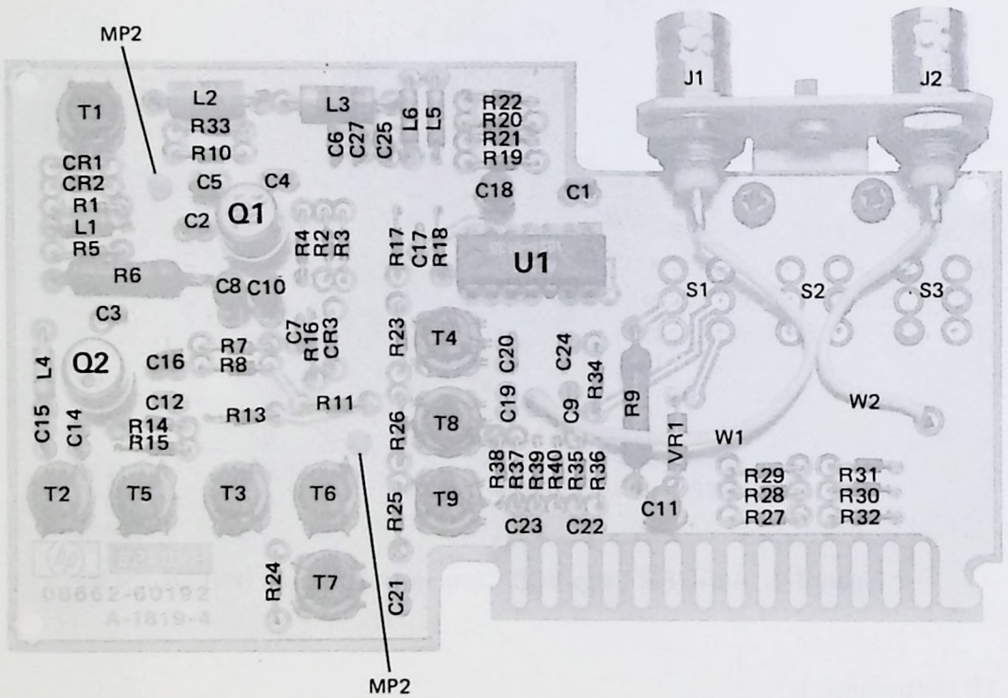


Figure 7-5. A8A4 Reference Buffer Component Locations (P/O Change Q)

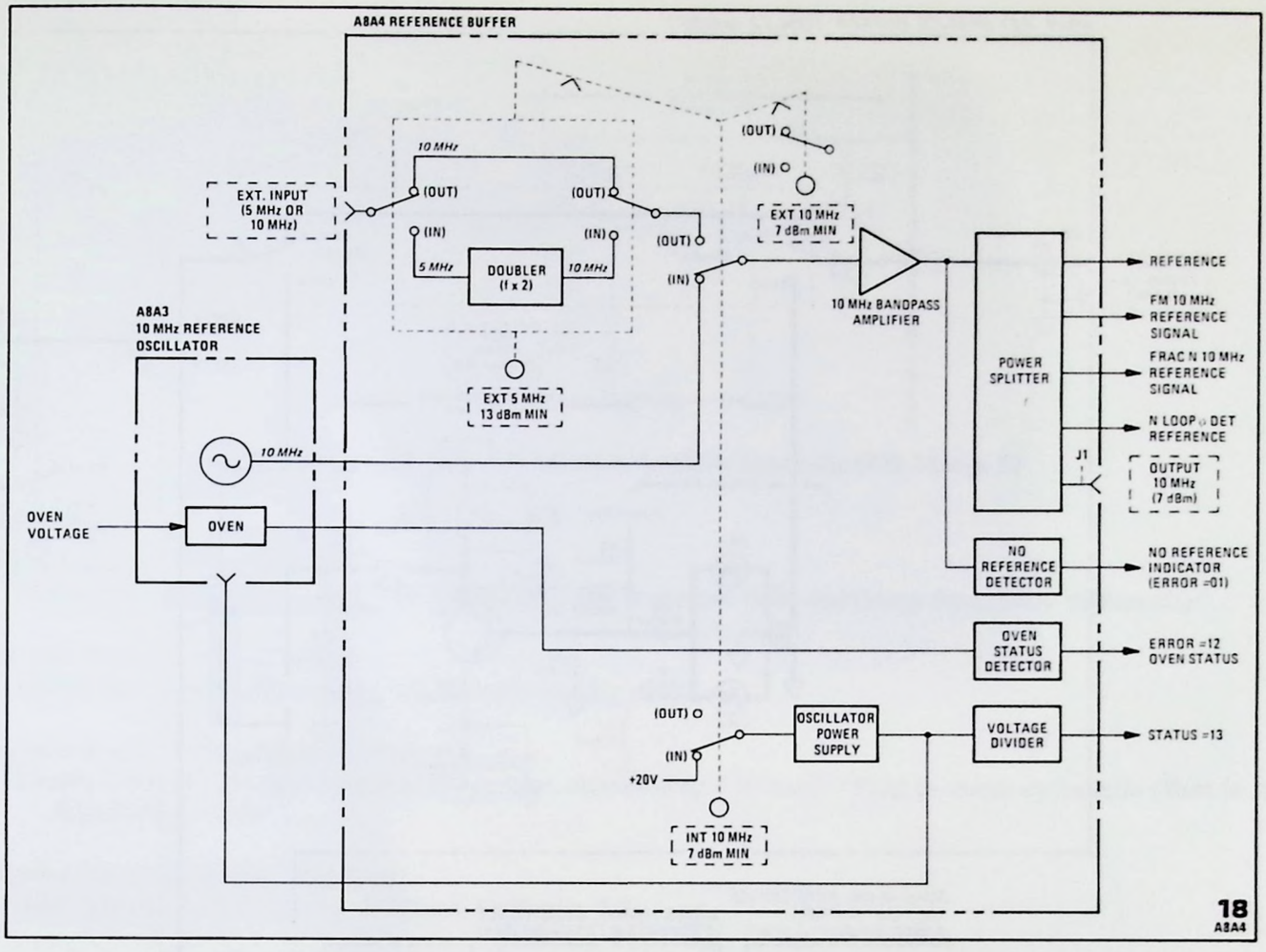


Figure 7-6. P/O A8A3 and A8A4 10 MHz Reference Oscillator and Buffer Block Diagrams (P/O Change Q)

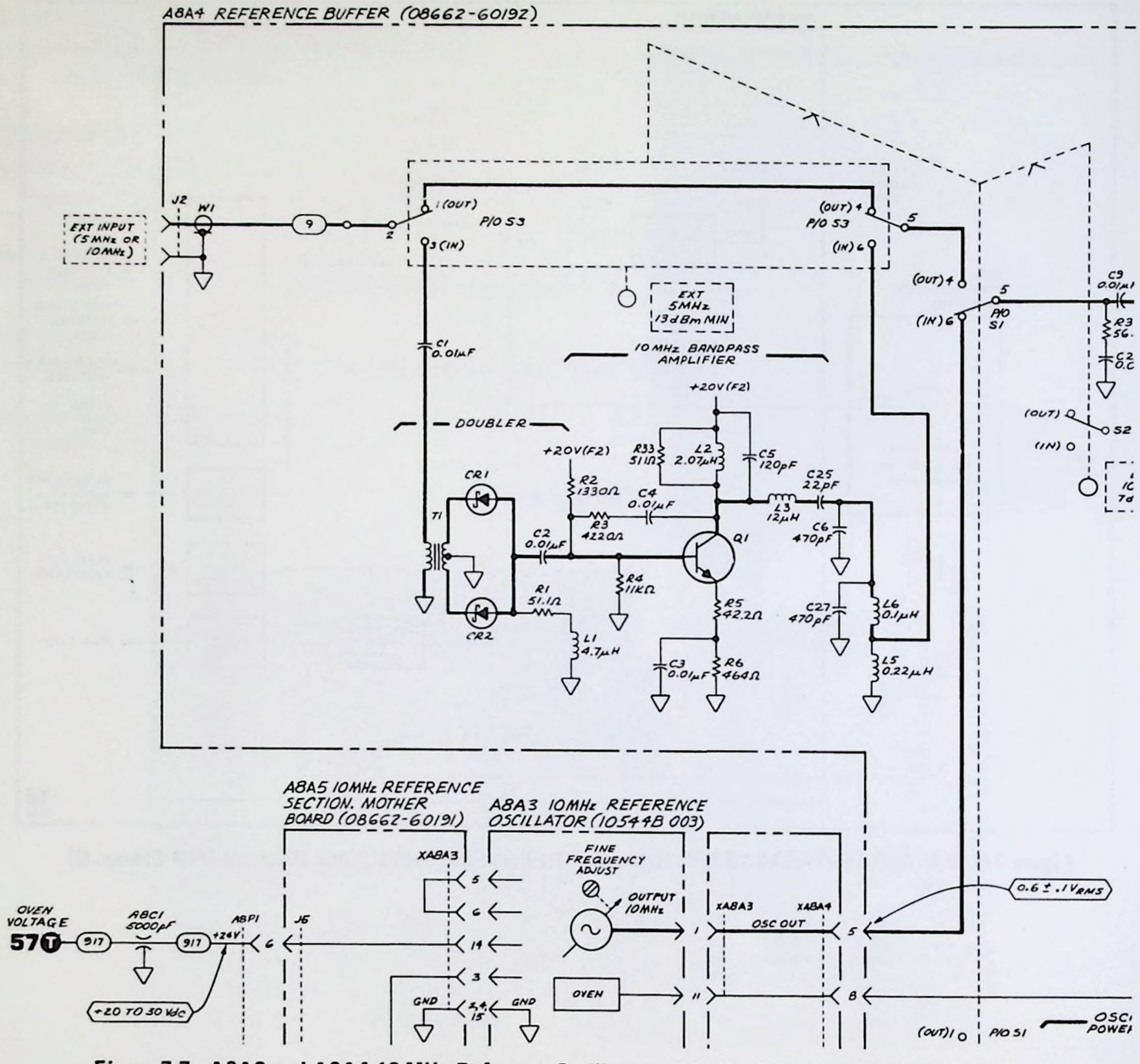


Figure 7-7. A8A3 and A8A4 10 MHz Reference Oscillator and Buffer Schematic (P/O Change Q)

CHANGE R

Service Sheet 32 (Schematic):

Change the value of R16 to 14.7Ω.

Service Sheet 35 (Schematic):

Delete Notes 4 and 5.

Replace the appropriate portion of the schematic with the following partial schematic (Figure 7-8).

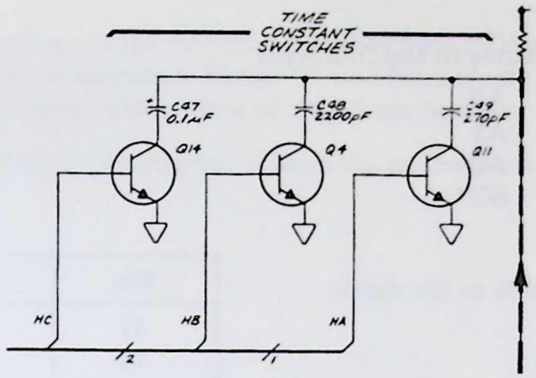


Figure 7-8. P/O A4A1 Output Amplifier Schematic (P/O Change R)

CHANGE S

Service Sheet A, Table 8-203:
Delete the following entry: "49 Sweep step size is greater than start/stop frequency difference".

Service Sheet A, Table 8-204:
Delete the following entry: "89 Factory testing only".

Service Sheet B (Troubleshooting):
Under General Troubleshooting Procedure, change step f to read: "Plug in memory boards (that is A2A7, A2A8 and A2A9) . . . ".

Service Sheet B (Block Diagram):
Add A2A8 (ROM1) block as shown in Figure 7-9.

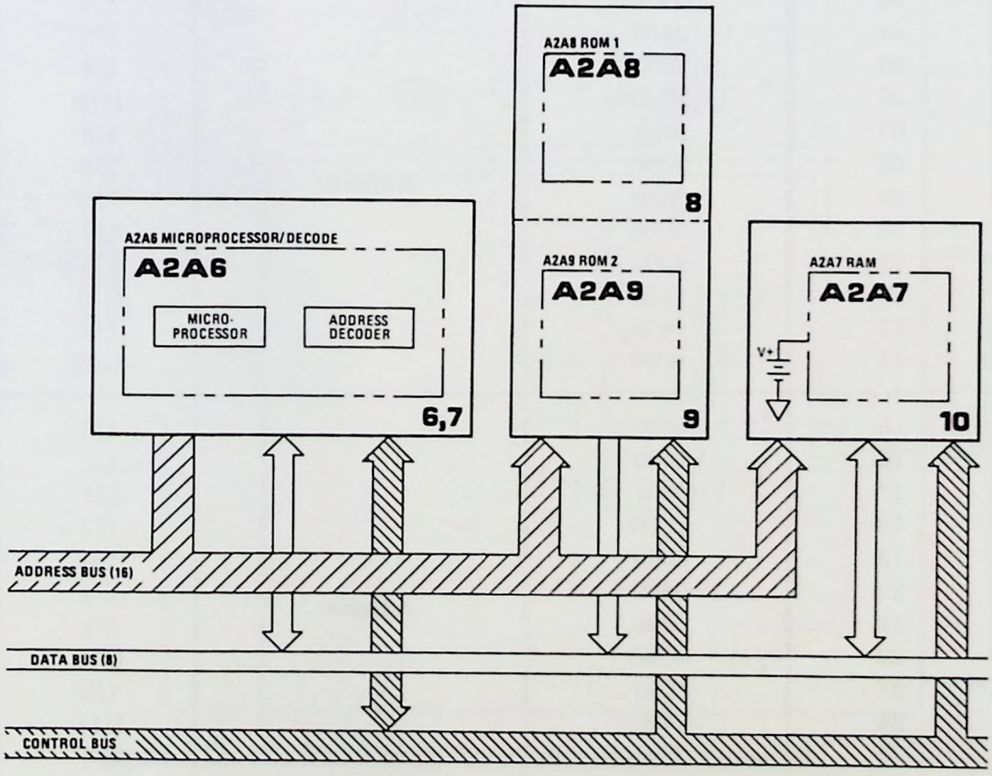


Figure 7-9. P/O Digital Control Unit (DCU) Block Diagram (P60 Change S)

CHANGE S (cont'd)

Service Sheet B2, Table 8-209:
Change the appropriate signatures to the following:

XA2A2A —	25	6169	A0
	24	1925	A1
	23	P8U1	A2
	22	P572	SC0

Service Sheet B2, Table 8-212:
Replace the table with the table to the right.

Pin	Signature
11	5785
12	U191
13	F2A0
14	1820
15	65H0
16	U995
17	233A
18	4CU8

Service Sheet B3, Table 8-215:
Replace the table with Table 7-5 below.

Table 7-5. ROM Test Error Codes (P/O Change S)

Error Code	Memory Address	Hardware Failure	
		Assembly (Service Sheet)	Device
01	1800	A2A5(5)	U11
02	1C00		U10
03	2000	A2A9(9)	U9
04	2400		U3
05	2800		U4
06	2C00		U10
07	3000		U8
08	3400		U2
09	3800		U1
10	3C00		U7
11	4000		U5
12	4400		U11
13	4800		U6
14	4C00		U12
15	5000	A2A8(8)	U8
16	5400		U2
17	5800		U1
18	5C00		U7
19	6000		U9
20	6400		U3
21	6800		U4
22	6C00		U10
23	7000		U5
24	7400		U11
25	7800		U6
26	7C00		U12

CHANGE S (cont'd)

Service Sheet 5 (Troubleshooting):

Change step 1 to read:

1. Perform the ROM test by selecting special function 83. This tests ROMs U10 and U11 and the associated data buffers and address decoders. Errors 01 and 02 indicate U11 and U10 respectively. If the ROM test passes (00 displayed) these parts of A2A5 are normal.

In the table entitled HP-IB Board (A2A5) Signatures, change the appropriate signatures to the following:

U7—	37	HP06
	38	8F57
	39	F5HH

Service Sheet 5 (Schematic):

Delete C8 and C9.

Remove R4 and connect the REN line to U6 pin 2.

Remove R5 and connect the IFC line to U6 pin 6.

Replace the appropriate portion of the schematic with the attached partial schematic (Figure 7-10).

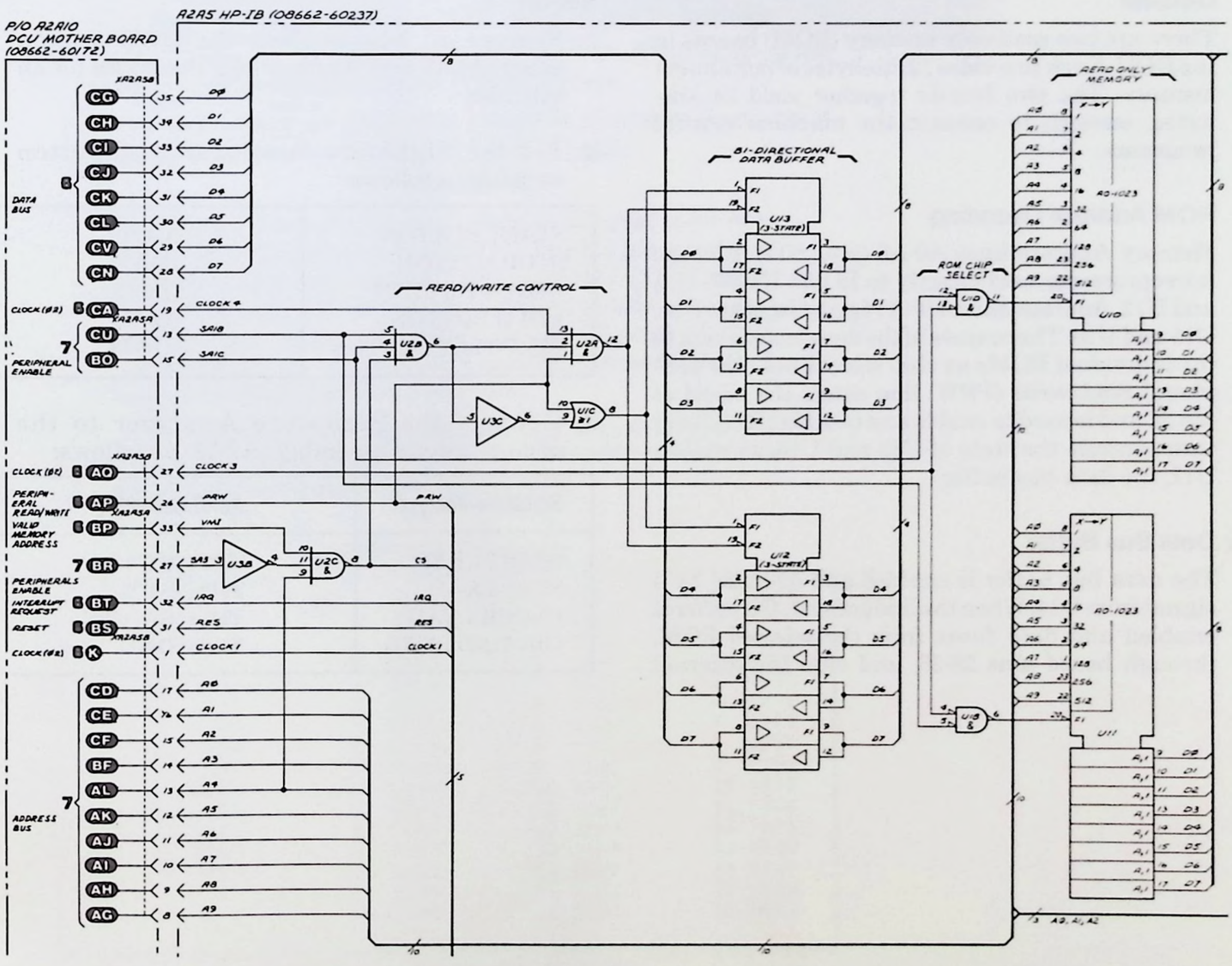


Figure 7-10. P/O A2A5 HP-IB Board Schematic (P/O Change S)

CHANGE S (cont'd)

Service Sheet 6 (Schematic):
In the Integrated Circuit Part Numbers table, change the part number for U6 to 08662-80014.

Service Sheet 8:
Add the attached Service Sheet 8 (Principles of Operation, Troubleshooting, Component Locations, Block Diagrams and Schematic).

SERVICE SHEET 8
A2A8 ROM 1 ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram B
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

There are two read-only memory (ROM) boards in the DCU. Each pro-vides 12 kilobytes of permanent memory. The two boards together yield 24 kilobytes, enough to contain the machine control programs.

ROM Address Decoding

Memory Address lines A0-A9 (pins 8-17) from the microprocessor feed directly to ROMs U1-U9, U11 and U12. Address lines A10-A14 go to decoders U14, U15 and U16. The outputs of the decoders are sent to the individual ROMs as chip select lines. The peripheral read/write (PRW) line enters the board at pin 26 and is used to enable and disable U14. U14 in turn controls the state of U15 and U16, as well as U17, the data bus buffer.

Data Bus Buffer

The data bus buffer is enabled and disabled by a signal from U14. When the line goes HI, the buffer is enabled and data flows from the selected ROM, through board pins 28-35, and onto the external data bus. The clock 3 line (pin 27) provides clocking for the board.

TROUBLESHOOTING

Signature Analysis can be used to troubleshoot the A2A8 assembly. The instructions for using this technique are given below.

Set-up

1. Remove all boards from the DCU section except A2A6 and A2A8. Place the A2A8 on an extender.

2. Set the Signature Analyzer pushbutton switches as follows:

START BUTTON	(OUT)
STOP BUTTON	(IN)
CLOCK BUTTON	(IN)
HOLD BUTTON	(OUT)
SELF-TEST BUTTON	(OUT)

3. Connect the Signature Analyzer to the microprocessor assembly (A2A6) as follows:

Signature Analyzer	A2A6 Assembly
START LEAD	TP2 ("ST")
STOP LEAD	TP2 ("ST")
CLOCK LEAD	TP1 ("SA, CK")
GROUND LEAD	TP6 ("GND")

CHANGE S (cont'd)

SERVICE SHEET 8 (cont'd)

4. Connect a ground lead between the ground pin (near the tip of the Signature Analyzer probe) and A2A6TP6.
5. Connect a jumper between A2A6TP4 and A2A6TP6. If the 10 pin shorting connector is plugged into the top of the Microprocessor Board, remove it. This puts the microprocessor board into a FREE RUN mode.

Pretest Procedure

1. Turn on the Signal Generator and the Signature Analyzer. Touch the Signature Analyzer probe to any convenient +5 Vdc pin, push the RESET button on the Signature Analyzer probe and then release. The Signature Analyzer should indicate "0000" and then "0001". If this does not occur, go back and re-check all connections and switch positions as outlined in the preceding setup procedure. Also, the UNSTABLE SIGNATURE lamp on the Signature Analyzer should be OFF and the GATE lamp should be flashing.
2. For this test, ignore anything displayed on the front panel of the Signal Generator. Any display is meaningless.
3. No button, switch or connection should be altered in the course of taking signatures on the ROM 1 board (A2A8).

NOTE

In the Signature listings the reference designator for each device is followed by a + or − sign; or each pin number is preceeded by a + or − sign. A + indicates the CLOCK button on the Signature Analyzer should be set to take signatures on the positive edge of the reference CLOCK pulse (CLOCK button OUT). A − indicates a negative or trailing edge signature reading (CLOCK button IN).

In the Signature listings some devices have a dashed line (----) substituted for the signature. The dash line indicates there is no valid Signature for that pin.

ROM 1 (A2A8) Signatures

U13-		U14-		U15-		U16-	
1	----	1	3C96	1	1293	1	1293
2	----	2	3827	2	HAP7	2	HAP7
3	----	3	755U	3	3C96	3	0000
4	----	4	0000	4	UA42	4	P255
5	----	5	0000	5	0001	5	0001
6	----	6	0001	6	0001	6	0001
7	0000	7	P255	7	1920	7	0001
8	UA42	8	0000	8	0000	8	0000
9	U3H5	9	U3H5	9	C34C	9	C001
10	0996	10	0996	10	597C	10	C001
11	1816	11	6H49	11	UA87	11	0001
12	P255	12	F2A6	12	2FF3	12	7A71
13	UA42	13	PC01	13	7807	13	U81U
14	0001	14	12U3	14	H6F4	14	8F14
		15	4P0A	15	71H4	15	PF2P
		16	0001	16	0001	16	0001

A2A8 ASSEMBLY

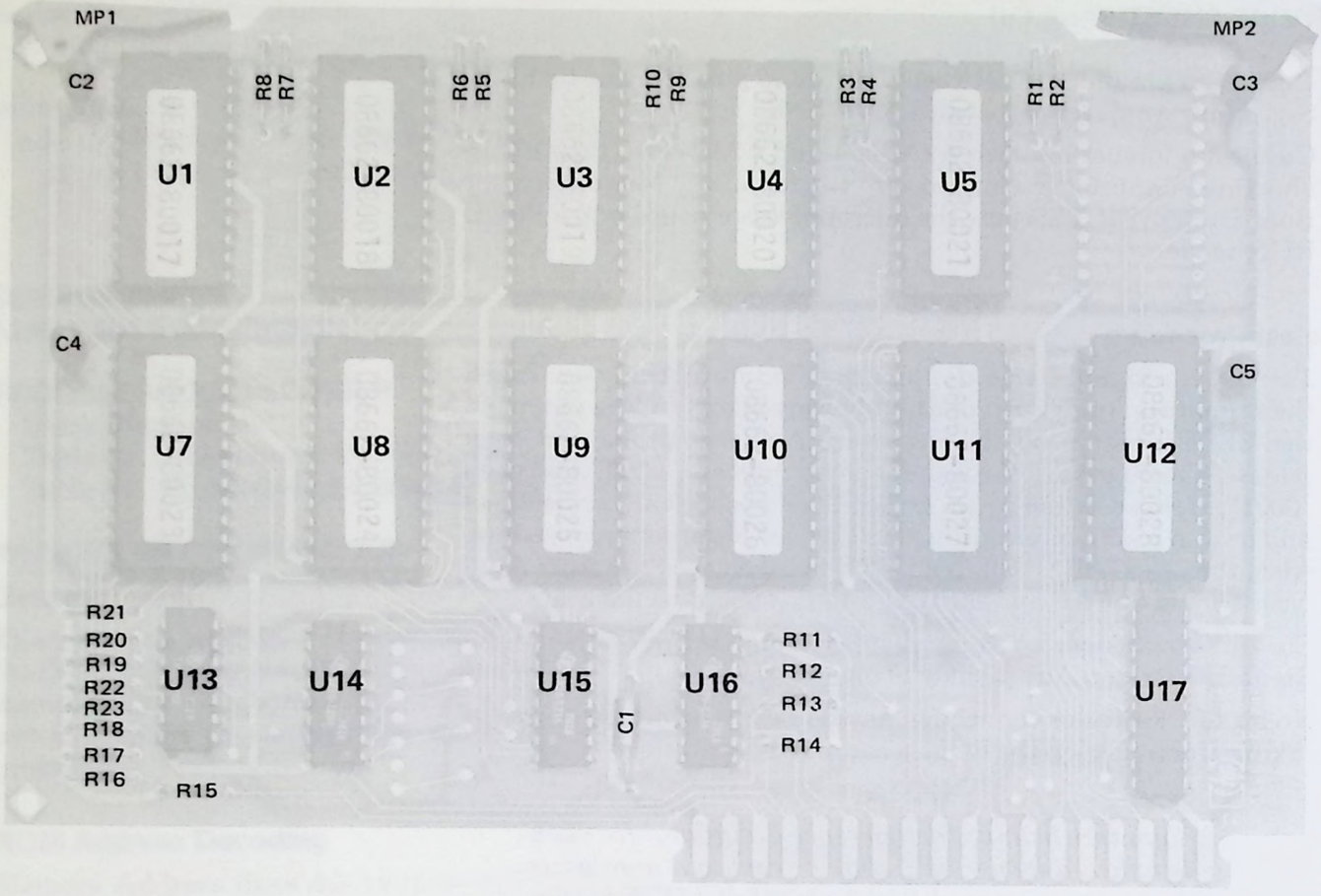


Figure 7-11. A2A8 ROM1 Component Locations (P/O Change S)

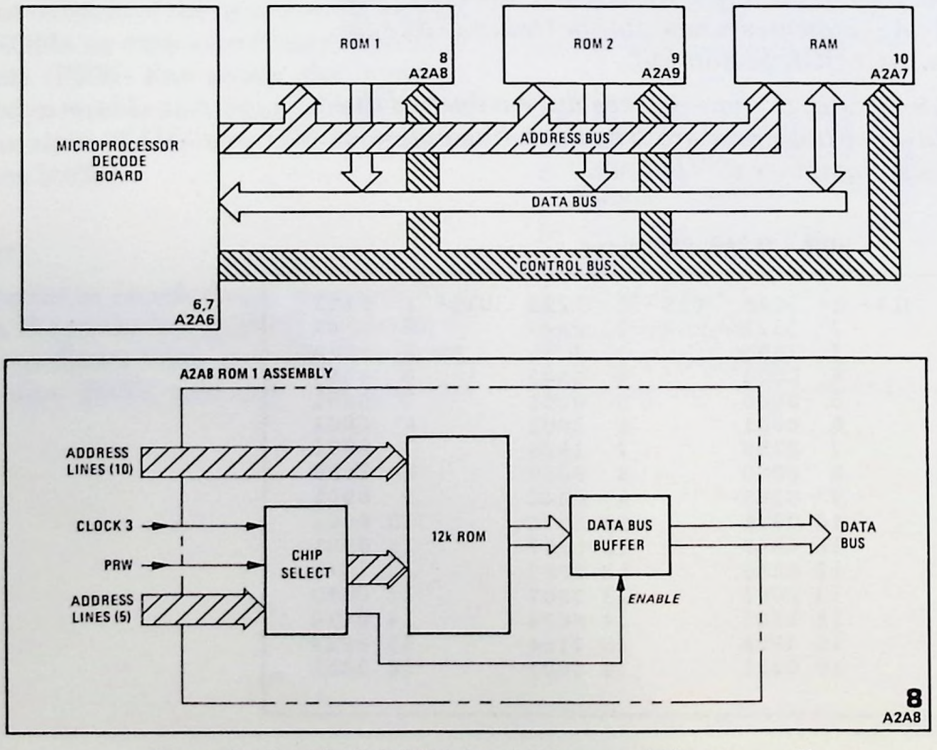
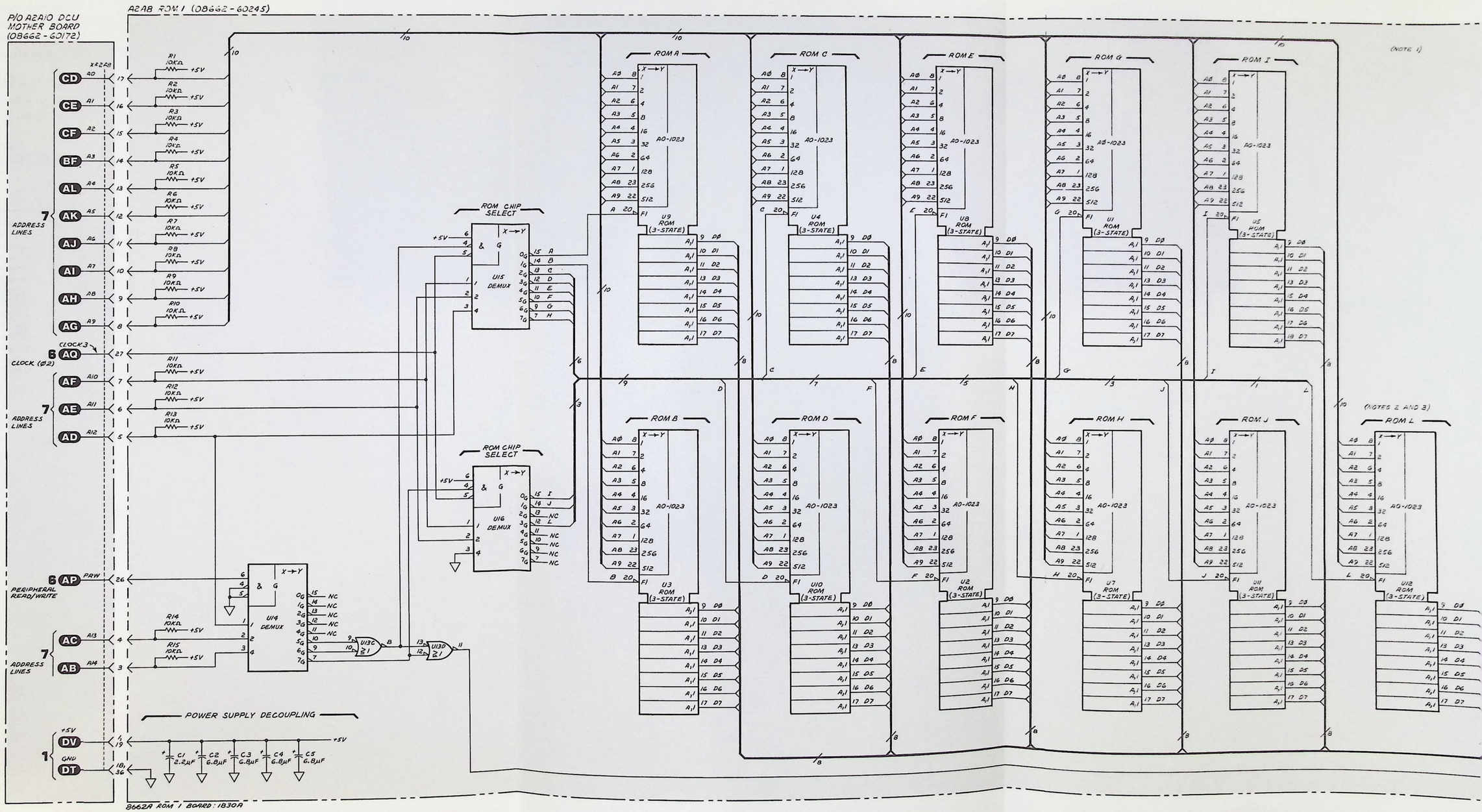


Figure 7-12. A2A8 ROM1 Block Diagrams (P/O Change S)


A2A8 ROM 1 (08662-60245)
P/O A2A10 DCU MOTHER BOARD (08662-60172)
X42A8
ADDRESS LINES
CLOCK (Ø2)
PERIPHERAL READ/WRITE
POWER SUPPLY DECOUPLING
ROM CHIP SELECT
U15 DEMUX
U16 DEMUX
U14 DEMUX
ROM A
ROM B
ROM C
ROM D
ROM E
ROM F
ROM G
ROM H
ROM I
ROM J
ROM L
A0-1023
U9 ROM (3-STATE)
U3 ROM (3-STATE)
U4 ROM (3-STATE)
U10 ROM (3-STATE)
U8 ROM (3-STATE)
U2 ROM (3-STATE)
U1 ROM (3-STATE)
U7 ROM (3-STATE)
U5 ROM (3-STATE)
U11 ROM (3-STATE)
U12 ROM (3-STATE)
U13C ≥1
U13D ≥1
(NOTE 1)
(NOTES 2 AND 3)
8662A ROM 1 BOARD: 1830A

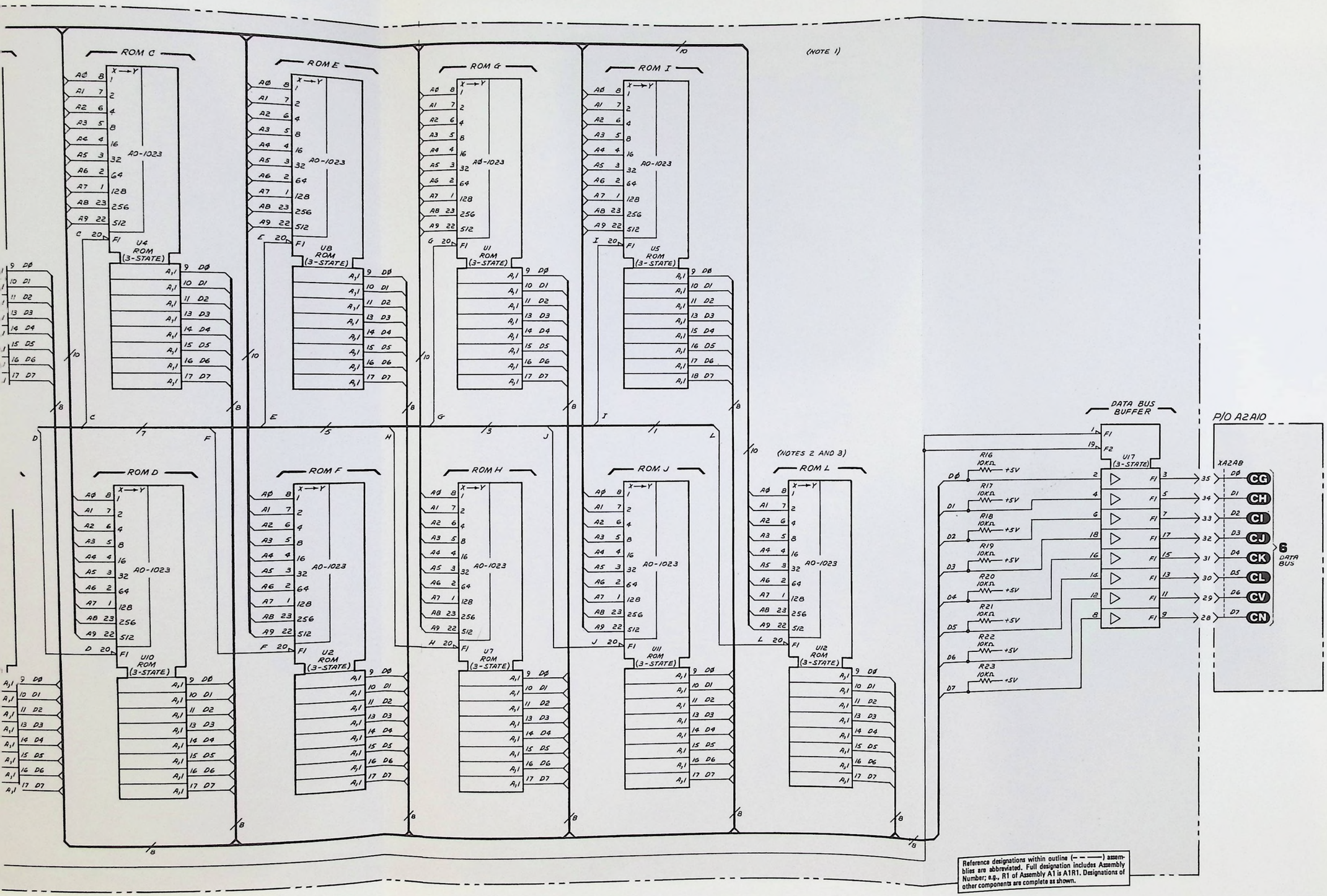


Figure 7-13. A2A8 ROM1 Schematic (P/O Change S)

NOTES

1. U6 (ROM K) IS NOT USED.
2. ROM U12 IS NOT SEPERATELY REPLACEABLE. IT MUST BE REPLACED AS PART OF A KIT THAT INCLUDES THE OUTPUT ATTENUATOR. SEE SECTION II FOR THE KITS PART NUMBER.
3. A NEW A2A8 PC BOARD WOULD COME EQUIPED WITH U12. HOWEVER, THERE WOULD BE NO AMPLITUDE CORRECTION DATA IN U12. IF THE ENTIRE A2A8 PC BOARD MUST BE REPLACED, SAVE AND USE U12 FROM THE OLD PC BOARD.

REFERENCE DESIGNATIONS

A2A8	A2A10
C1-5 R1-23 U1-5, 7-17	XA2B

LOGIC LEVELS

LOGIC	TTL	ECL	EECL	CMOS
HIGH (1)	≥ 2V	≥ -1.0V	≥ +4.9V	≈ VDD
LOW (0)	≤ 0.8V	≤ -1.5V	≤ +4.4V	≤ 0.1V
≤ = EQUAL TO OR MORE NEGATIVE THAN ≥ = EQUAL TO OR MORE POSITIVE THAN				
INPUT	TTL	ECL	EECL	CMOS
GROUND	LOW (0)	HIGH (1)	HIGH (1)	LOW (0)
OPEN	HIGH (1)	LOW (0)	LOW (0)	X
GROUND = 0V; X = UNDEFINED				

INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
U1	08662-80017
U2	08662-80018
U3	08662-80019
U4	08662-80020
U5	08662-80021
U7	08662-80023
U8	08662-80024
U9	08662-80025
U10	08662-80026
U11	08662-80027
U12	NOTE 2
U13	1820-1201
U14-16	1820-1216
U17	1820-1759

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U1-5, 7-12	+5V — 24 ▽ — 12
U13	+5V — 14 ▽ — 7
U14-16	+5V — 16 ▽ — 8
U17	+5V — 20 ▽ — 10

CHANGE S (cont'd)

Service Sheet 9 (Principles of Operation):

Replace the paragraph entitled GENERAL with the following:

"There are two read-only memory (ROM) boards in the DCU. Each provides 12 kilobytes of permanent memory. The two boards together yield 24 kilobytes, enough to contain the machine control program."

In the paragraph entitled ROM Address Decoding, change the first two senteces to read:

"Memory address lines A0—A9 (pins 8—17) from the microprocessor feed directly to ROMs U1—U9, U11 and U12. Address lines A10—A14 go to decoders U14, U15 and U16.

Service Sheet 9 (Troubleshooting):

Change the table entitled ROM2 (A2A9) Signatures to the following:

U13-		U14-		U15-		U16-	
1	----	1	3C96	1	1293	1	1293
2	----	2	3827	2	HAP7	2	HAP7
3	----	3	755U	3	3C96	3	0000
4	----	4	0000	4	29A6	4	6H49
5	----	5	0000	5	----	5	----
6	----	6	0001	6	0001	6	0001
7	0000	7	P255	7	942F	7	0001
8	29A6	8	0000	8	0000	8	0000
9	F2A6	9	U3H5	9	F042	9	0001
10	PC01	10	0996	10	131H	10	0001
11	44PP	11	6H49	11	85H4	11	0001
12	6H49	12	F2A6	12	5969	12	4154
13	29A6	13	PC01	13	0PC5	13	960F
14	0001	14	12U3	14	270P	14	84AF
		15	4P0A	15	9CH2	15	3PCF
		16	0001	16	0001	16	0001

CHANGE S (cont'd)

Service Sheet 9, (Block Diagrams):
Replace Figure 8-326 with Figure 7-14.

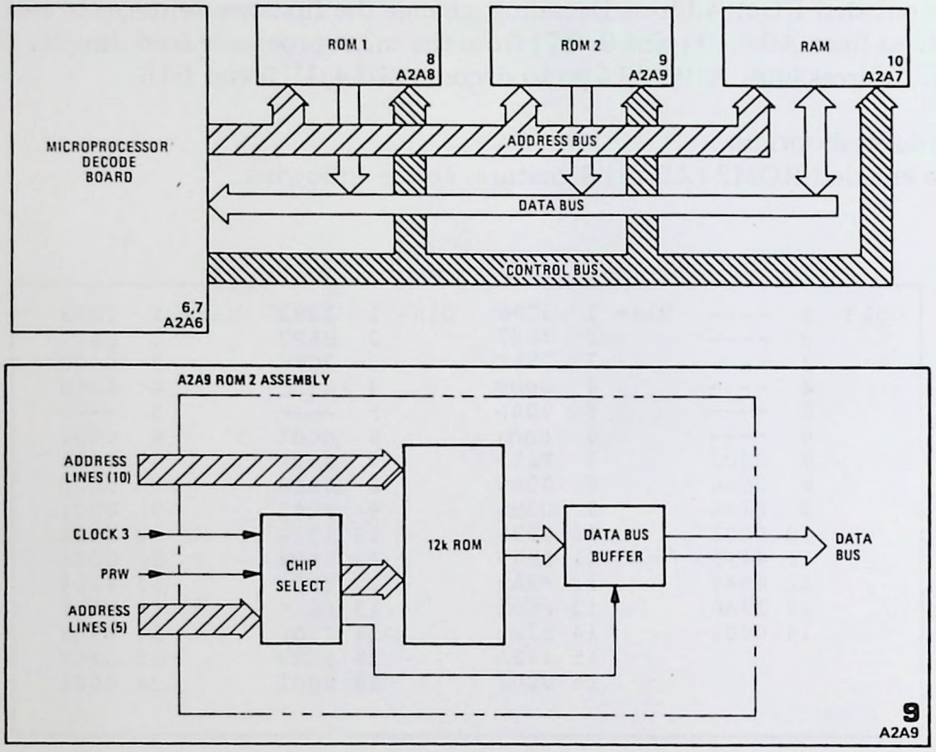
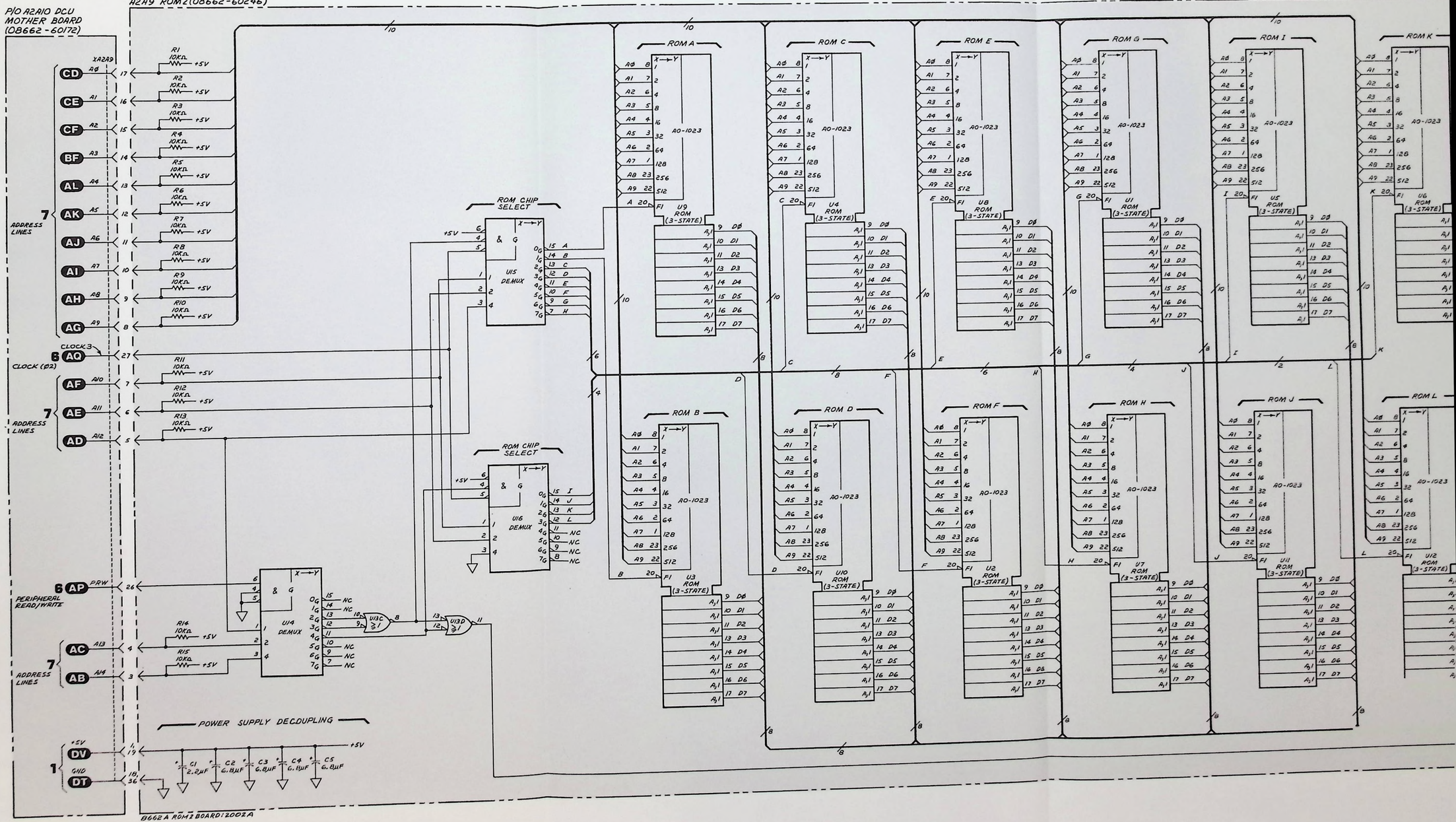


Figure 7-14. ROM2 Block Diagrams (P/O Change S)

Service Sheet 9, (Schematic):
Replace the schematic with the attached schematic, Figure 7-15 on the following page.

ROM 2
A2A9
SERVICE SHEET 9


A2A9 ROM2 (08662-60246)
P/O A2A10 DCU MOTHER BOARD (08662-60172)
XA2A9
CD
CE
CF
BF
AL
AK
AJ
AI
AH
AG
7 ADDRESS LINES
R1 10KΩ +5V
R2 10KΩ +5V
R3 10KΩ +5V
R4 10KΩ +5V
R5 10KΩ +5V
R6 10KΩ +5V
R7 10KΩ +5V
R8 10KΩ +5V
R9 10KΩ +5V
R10 10KΩ +5V
CLOCK 3
AQ
CLOCK (Ø2)
AF
AE
AD
7 ADDRESS LINES
R11 10KΩ +5V
R12 10KΩ +5V
R13 10KΩ +5V
AP PRW
PERIPHERAL READ/WRITE
AC
AB
7 ADDRESS LINES
R14 10KΩ +5V
R15 10KΩ +5V
DV
DT
1 GND
POWER SUPPLY DECOUPLING
C1 2.2μF
C2 6.8μF
C3 6.8μF
C4 6.8μF
C5 6.8μF
ROM CHIP SELECT
U15 DEMUX
U16 DEMUX
U14 DEMUX
U13C
U13D
ROM A
ROM B
ROM C
ROM D
ROM E
ROM F
ROM G
ROM H
ROM I
ROM J
ROM K
ROM L
A0-1023
U9 ROM (3-STATE)
U3 ROM (3-STATE)
U4 ROM (3-STATE)
U10 ROM (3-STATE)
U8 ROM (3-STATE)
U2 ROM (3-STATE)
U1 ROM (3-STATE)
U7 ROM (3-STATE)
U5 ROM (3-STATE)
U11 ROM (3-STATE)
U6 ROM (3-STATE)
U12 ROM (3-STATE)
B662A ROM2 BOARD: 2002A

REFERENCE DESIGNATIONS

A2A9	A2A10
C1-5 R1-23 U1-17	X2A9

LOGIC LEVELS

LOGIC	TTL	ECL	EECL	CMOS
HIGH (1)	≥ 2V	≥ −1.0V	≥ −1.3V	≈ VDD
LOW (0)	≤ 0.8V	≤ −1.5V	≤ −1.6V	≤ 0.1V
≤ = EQUAL TO OR MORE NEGATIVE THAN ≥ = EQUAL TO OR MORE POSITIVE THAN				
INPUT	TTL	ECL	EECL	CMOS
GROUND	LOW (0)	HIGH (1)	HIGH (1)	LOW (0)
OPEN	HIGH (1)	LOW (0)	LOW (0)	X
GROUND = 0V; X = UNDEFINED				

INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
U1	08662-80042
U2	08662-80043
U3	08662-80031
U4	08662-80032
U5	08662-80033
U6	08662-80034
U7	08662-80035
U8	08662-80044
U9	08662-80037
U10	08662-80038
U11	08662-80039
U12	08662-80040
U13	1820-1201
U14-16	1820-1216
U17	1820-1759

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PART NUMBERS
U1-12	+5V − 24 ▽ − 12
U13	+5V − 14 ▽ − 7
U14-16	+5V − 16 ▽ − 8
U17	+5V − 20 ▽ − 10

Reference designations within outline (– – – –) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

A2A9

Figure 7-15. A2A9 ROM2 Schematic (P/O Change S)

CHANGE S (cont'd)

Service Sheet 10 (Block Diagram):
Change the upper diagram per attached Figure 7-16.

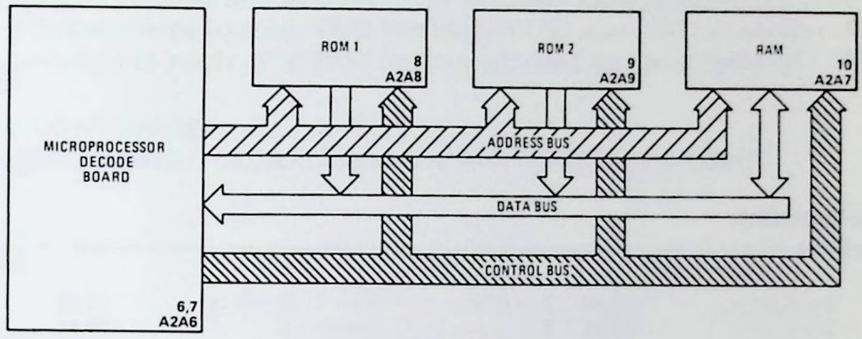


Figure 7-16. P/O A2A7 RAM Block Diagram (P/O Change S)

Service Sheet 14 (Schematic):
Replace the appropriate portion of the schematic with the partial schematic below (Figure 7-17).

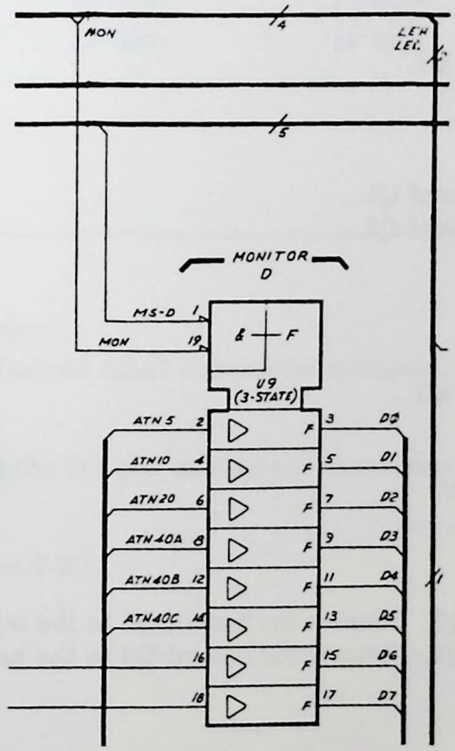


Figure 7-17. P/O A2A3 Level/Modulation Output Schematic (P/O Change S)

Change the A2A3 part number (in the upper left corner of the page) to 08662-60170.

Service Sheet 15 (Schematic):
Change the A2A3 part number (in the upper left corner of the page) to 08662-60170.

CHANGE S (cont'd)

Service Sheet 17 (Troubleshooting):
In the table entitled Sweep Board (P/O A2A2) Signatures, Make the following changes:

U10—1	6169
—2	1925
—3	P8U1
—4	P572

CHANGE T

Service Sheet 36 (Schematic):
Remove C9, 22 μF.

CHANGE U

Service Sheet 9 (Schematic):
Remove R11, 10 kΩ.

Service Sheet 24 (Schematic):
Change the value of R34 to 2.37 kΩ.
Change the value of R156 to 1 kΩ.

Service Sheet 28 (Schematic):
Change the value of R34 to 2.37 kΩ.
Change the value of R156 to 1 kΩ.

Service Sheet 47 (Schematic):
Delete ferrite bead E1 on the base of Q1.
Delete ferrite bead E2 on the base of Q2.

CHANGE V

Service Sheet 33 (Schematic):
Change the value of R43 to 5.11 kΩ.

Service Sheet 46 (Schematic):
Change the value of C9 to 220 μF.
Change the value of L2 to 75 μH.

Service Sheet 55 (Schematic):
Remove fuse F1 on the base of Q3. Connect the base of Q3 to the injunction of R9 and R7.
Remove fuse F2 on the base of Q4. Connect the base of Q4 to the junction of R10 and R8.

CHANGE W

Service Sheet 3 (Schematic):
Remove C8 from the A2A1 Key Code Board.
Disconnect C8 from pin 15 of U14 and +5V. Leave pin 15 of U14 unconnected (NC).
Remove R12 from between U22 pin 4 and +5V. Connect U22 pin 4 to +5V.

CHANGE X

Service Sheet 10 (Principles of Operation):

In the paragraph entitled Read/Write Control and RAM Chip Select, change the last sentence to read: "RAM selection is implemented by U18."

In the paragraph entitled Address and Bi-Directional Data Bus Buffers, make the following changes:

1. Change the third sentence to read: Data bus buffers U21 and U22 are bi-directional.
2. Add a fifth sentence to read: The PRW line is controlled by the outputs of U20.

Service Sheet 10 (Troubleshooting):

Replace the table of RAM Board (A2A7) Signatures with the following table:

U18-		U19-		U20-		U23-	
1	2H70	1	----	1	0001	1	383A
2	HPP0	2	----	2	383C	2	HC89
3	1293	3	----	3	383A	3	PF91
4	0000	4	----	4	0001	4	52F8
5	0000	5	----	5	0001	5	3U39
6	383C	6	----	6	0000	6	UPFH
7	UHUF	7	0000	7	0000	7	90F5
8	0000	8	383C	8	383A	8	0AFA
9	A756	9	HAP7	9	383C	9	C01U
10	7528	10	3C96	10	383C	10	0000
11	2H54	11	0001	11	0001	11	P262
12	0P63	12	3827	12	0000	12	5H21
13	6541	13	755U	13	383C	13	CA80
14	2317	14	0001	14	0001	14	7F7F
15	72H8					15	9128
16	0001					16	CCCC
						17	3562
						18	5555
						19	383A
						20	0001

Service Sheet 10 (Component Locations):

Replace Figure 8-328 with the attached A2A7 component locations (Figure 7-18).

Service Sheet 10 (Block Diagrams):

In the second block diagram, add the OR gate as shown in the attached block diagram, Figure 7-19.

Service Sheet 10 (Schematic):

Replace the schematic with Figure 7-20.

A2A7 ASSEMBLY

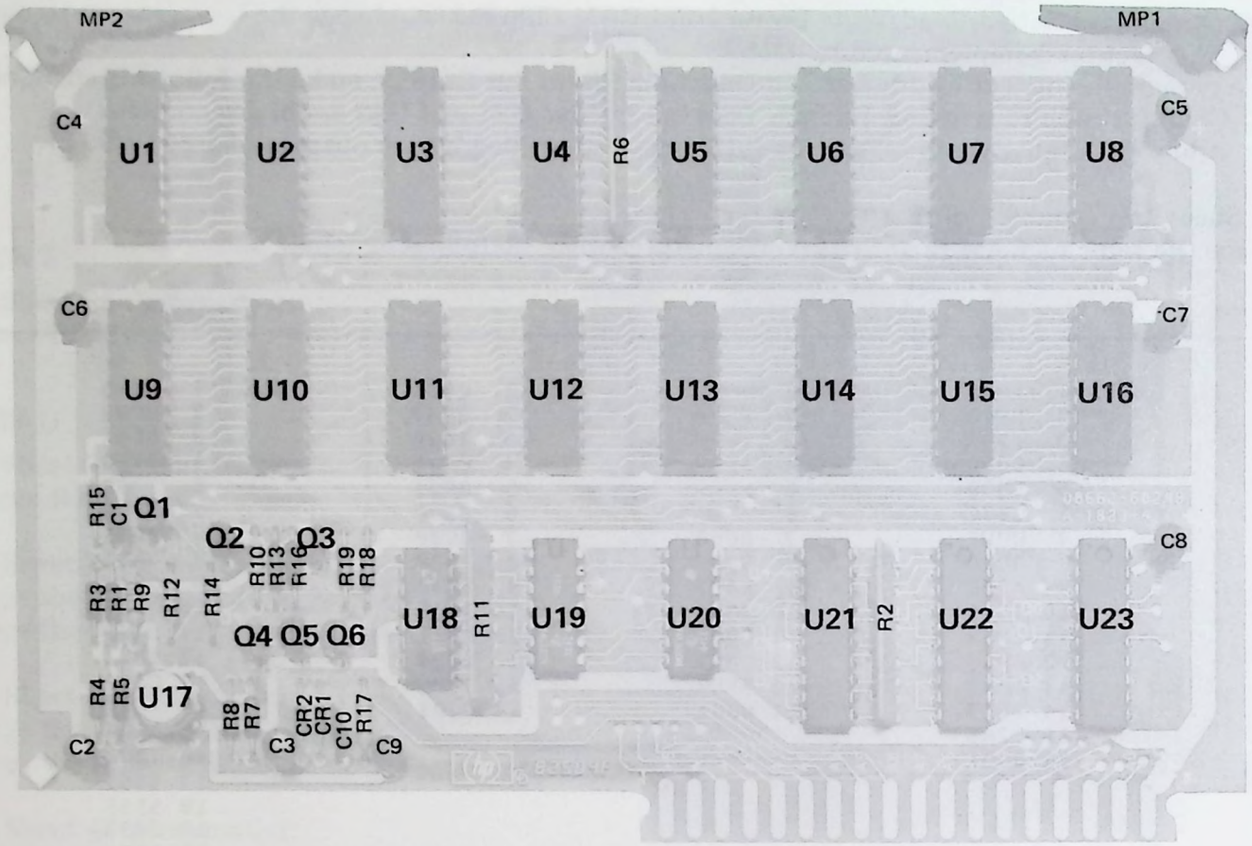


Figure 7-18. A2A7 RAM Component Locations (P/O Change X)

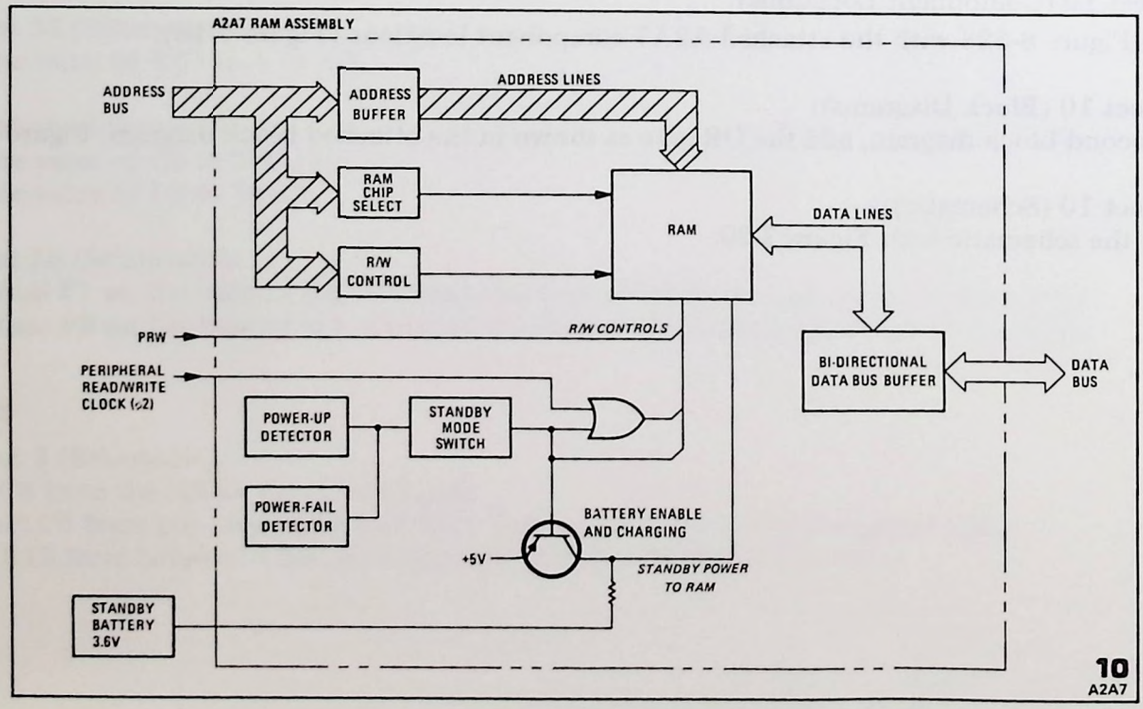
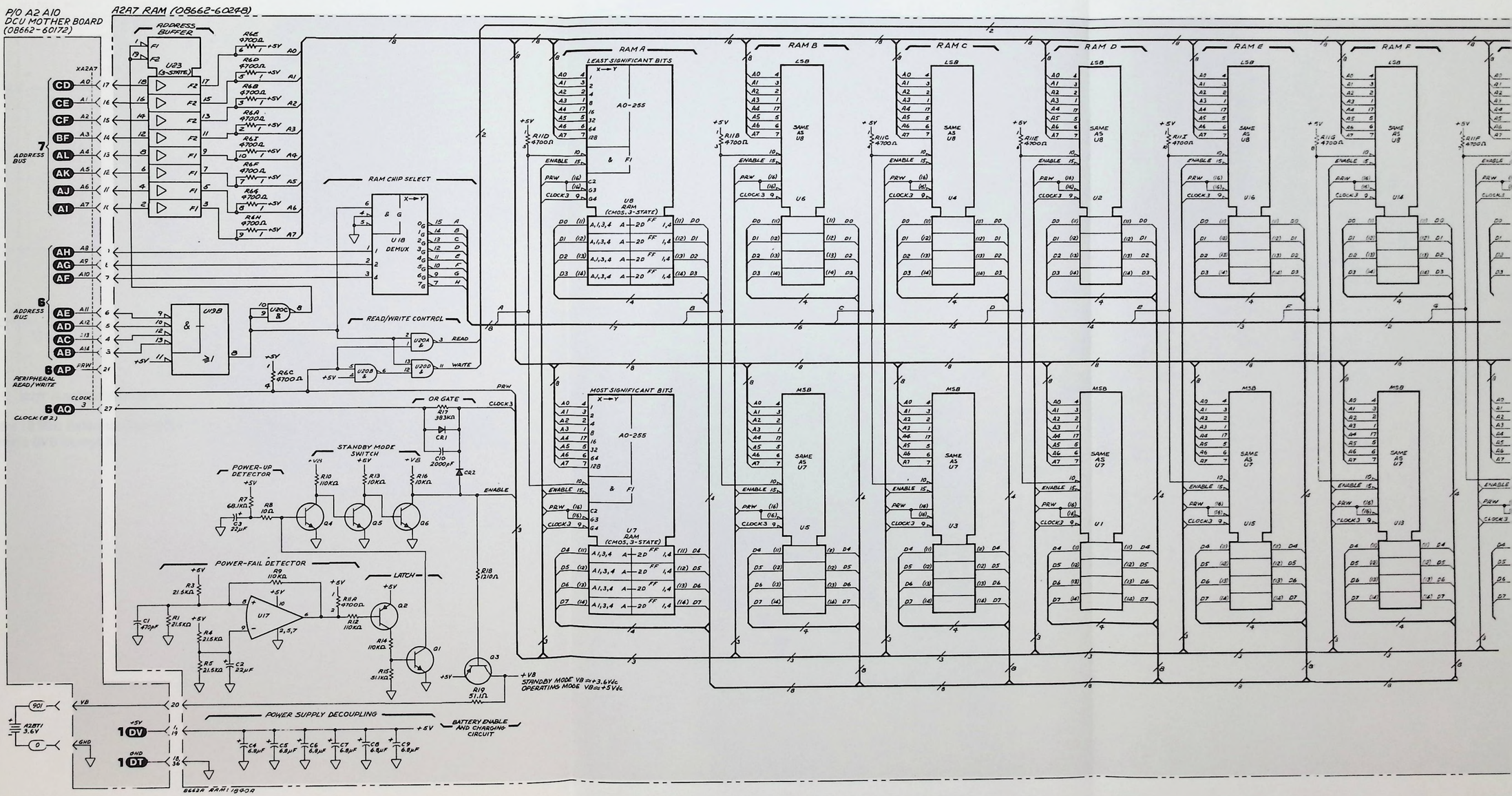
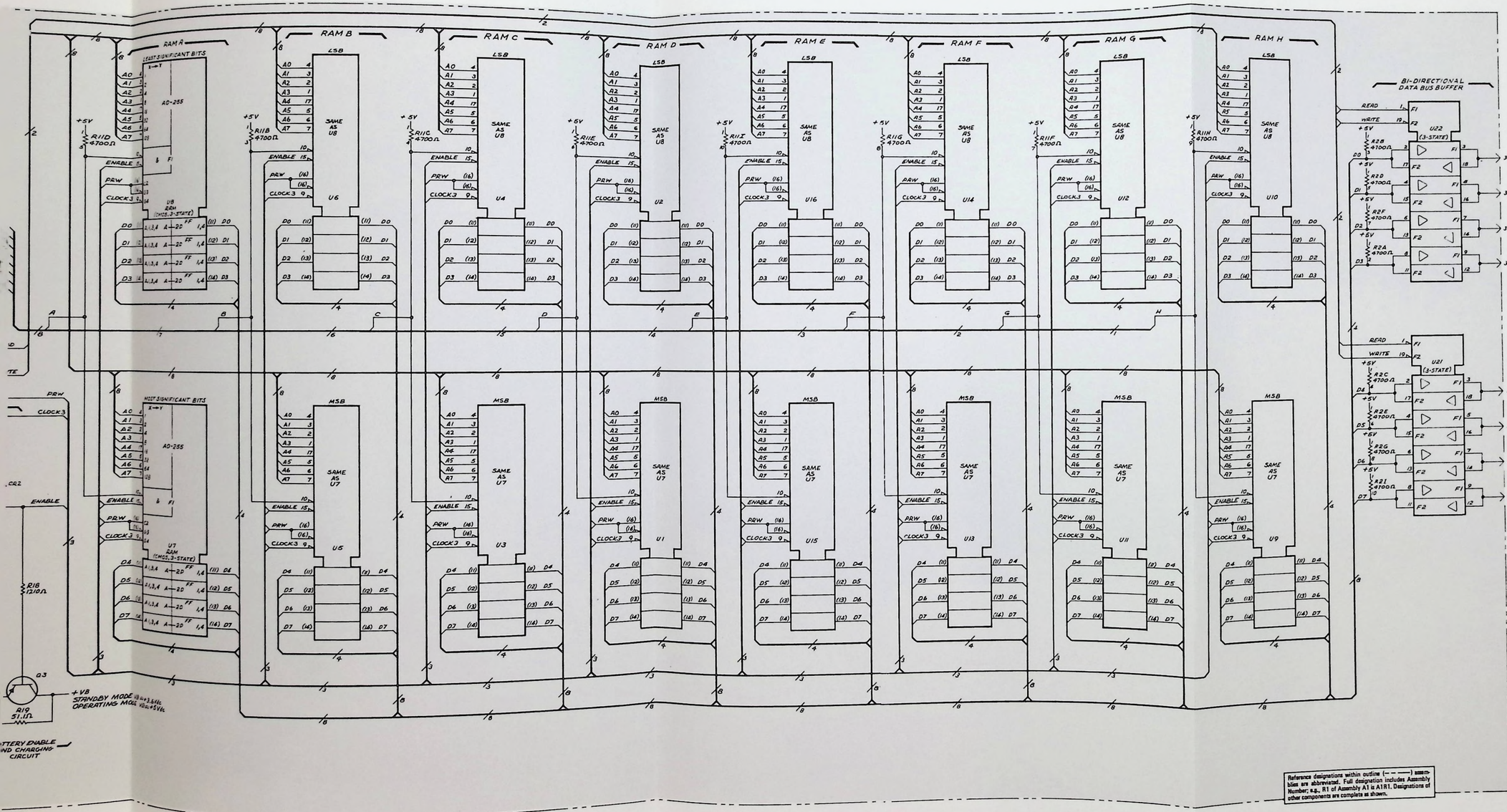


Figure 7-19. P/O A2A7 RAM Block Diagram (P/O Change X)


P/O A2 A10
DCU MOTHER BOARD
(08662-60172)
A2A7 RAM (08662-60278)
ADDRESS BUFFER
U23 (3-STATE)
RAM A
RAM B
RAM C
RAM D
RAM E
RAM F
LEAST SIGNIFICANT BITS
MOST SIGNIFICANT BITS
A0-255
U8 RAM (CMOS, 3-STATE)
U7 RAM (CMOS, 3-STATE)
SAME AS U8
SAME AS U7
RAM CHIP SELECT
U18 DEMUX
READ/WRITE CONTROL
OR GATE
STANDBY MODE SWITCH
POWER-UP DETECTOR
POWER-FAIL DETECTOR
LATCH
POWER SUPPLY DECOUPLING
BATTERY ENABLE AND CHARGING CIRCUIT
ADDRESS BUS
PERIPHERAL READ/WRITE
CLOCK (Ø2)
+VB STANDBY MODE VB ≅ +3.6Vdc
OPERATING MODE VB ≅ +5Vdc
A22BT/ 3.6V
8662A RAM: 19400



REFERENCE DESIGNATIONS

A2	A2 A10
BT1	XA2A10
A2A7	
C1-10 CR1,2 Q1-6 R1-19 U1-23	

LOGIC LEVELS

LOGIC	TTL	ECL	EECL	CMOS
HIGH (1)	≥ 2V	≥ +4.0V	≥ +4.5V	≥ VDD
LOW (0)	≤ 0.8V	≤ +3.5V	≤ +4.4V	≤ 0.1V
≤ = EQUAL TO OR MORE NEGATIVE THAN ≥ = EQUAL TO OR MORE POSITIVE THAN				
INPUT	TTL	ECL	EECL	CMOS
GROUND	LOW (0)	HIGH (1)	HIGH (1)	LOW (0)
OPEN	HIGH (1)	LOW (0)	LOW (0)	X
GROUND = 0V; X = UNDEFINED				

R22, 6, 11 BOTTOM VIEW

1	2	3	4	5	6	7	8	9	10

+5V A B C D E F G H I

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1,4-6	1854-0071
Q2,3	1853-0393
U1-16	1818-2429
U17	1826-0791
U18	1820-1216
U19	1820-0555
U20,21	1820-1548
U22	1820-2275
U23	1820-2024

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS	
U1-16	VB	18
	▽	8
U18	+5V	16
	▽	8
U19-20	+5V	14
	▽	7
U21-23	+5V	20
	▽	10

Figure 7-20. A2A7 RAM Schematic (P/O Change X)

CHANGE X (cont'd)

Service Sheet 18 (Schematic):

Replace appropriate parts of the schematic with the attached partial schematics (Figure 7-21 and 7-22).

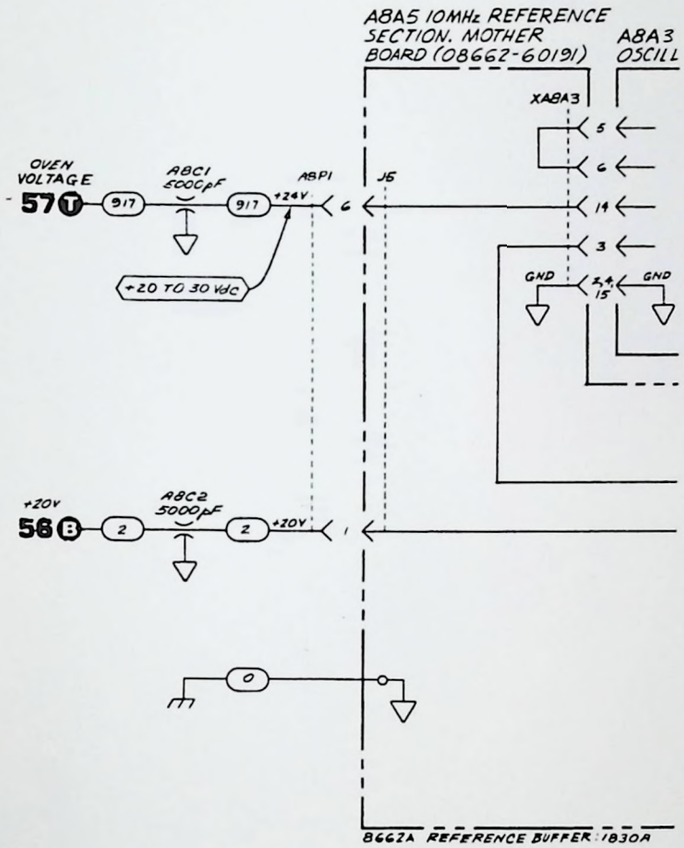


Figure 7-21. Input Side of the 10 MHz Reference Oscillator and Buffer Schematic (P/O Change X)

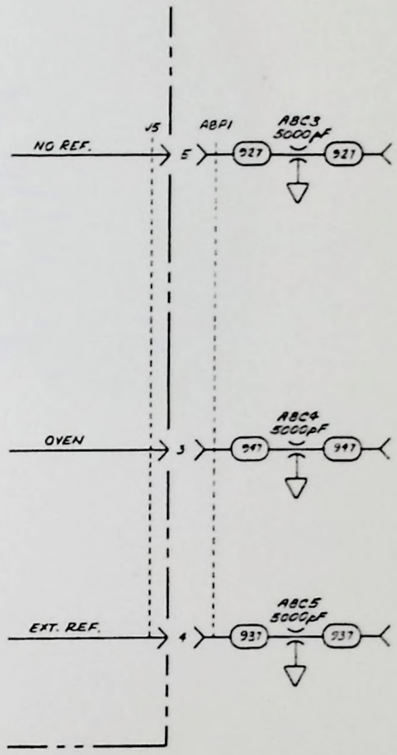


Figure 7-22. Output Side of the 10 MHz Reference Oscillator and Buffer Schematic (P/O Change X)



Printed in U.S.A.

SERVICE MANUAL

8662A Synthesized Signal Generator

10 kHz — 1280 MHz



P/O Section VIII
Service
General Information

HEWLETT PACKARD

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SAFETY CONSIDERATIONS

GENERAL

This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation.

This product is a Safety Class I instrument (provided with a protective earth terminal.

BEFORE APPLYING POWER

Verify that the product is set to match the available line voltage and the correct fuse is installed.

SAFETY SYMBOLS



Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual (refer to table of contents).



Indicates hazardous voltages.



Indicates earth (ground) terminal.

WARNING The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

CAUTIONS

The casual operator should not replace the LINE fuse. Replacing this fuse in a damaged Generator might cause additional damage. A qualified service person should first determine the cause of its failure, specifically with resistance checks in the power supply (see Service Sheet 55); repair the failure and then replace the fuse.

Do not unplug the A4A7 AGC board or the A4A9 Modulation board unless the instrument is unplugged or switched to standby. The A4A7 and A4A9 boards contain CMOS devices which may be damaged if the board is removed when the power is on.

RF testpoints on some pc boards (that is, the small two-contact cup connectors) require ac-coupling to test equipment. DC-coupling might damage the Generator or the test equipment. Use the ac-coupled RF Test Probe in the 11714A Service Accessory Kit.

WARNINGS

Maintenance described in this section is performed with power supplied to the instrument and with protective covers removed. Maintenance should be performed only by service trained personnel who are aware of the hazard involved (for example, fire and electrical shock). Where maintenance can be performed without power applied, the power should be removed.

When working on the power supply, remember that high voltage is present at all times when the line cord is plugged in (that is, plus and minus 160 Vdc and line voltage). Unplug the line cord before doing anything to the power supply. The line switch has no effect on the high voltage.

A pin-to-pin voltage difference of 60 Vdc may be found on many of the Generator's circuit board connectors. Be careful while working on the circuit boards with power supplied to the instrument. If a circuit board is placed on an extender board, the possibility of coming in contact with 60 Vdc is greatly increased. Be careful while working on the circuit boards with power supplied. Work with one hand. Do not touch the extender board.

Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

Any interruption of the protective (grounding) conductor (inside or outside the instrument) or disconnecting the protective earth terminal will cause a potential shock hazard that could result in personal injury. (Grounding one conductor of a two conductor outlet is not sufficient protection).

Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.

If this instrument is to be energized via an autotransformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the power source.

When working near the back of the Generator, take care not to let long hair be drawn into the fan. This could result in personal injury.

For continued protection against fire hazards, replace the LINE and OVEN fuses only with 250V normal blow fuses with the same current rating. Do not use repaired fuses or short circuited fuseholders.

SECTION VIII
SERVICE

8-1. INTRODUCTION

This section contains troubleshooting and repair information for the HP Model 8662A Synthesized Signal Generator. This section includes diagrams, circuit descriptions, troubleshooting instructions, component locators and disassembly instructions.

The remaining sections of the Operating and Service Manual are in Volume 1. They are General Information, Installation, Operation, Performance Tests, Adjustments, Replaceable Parts and Manual Changes.

8-2. INSTRUMENTS COVERED BY MANUAL

The contents of this manual apply to instruments with the serial number prefix(es) listed under SERIAL NUMBERS on the title page for Volume 2. A Manual Changes supplement for Volume 2 is provided to document instruments with prefixes higher than those on the title page. Section VII Part 2 (in Volume 2) is provided to document instruments with prefixes lower than those on the title page.

8-3. CIRCUIT DESCRIPTIONS

The Signal Generator's circuitry is described at three distinctly different levels.

1. Service Sheet A contains an overview of the entire Generator.

2. Service Sheets B through I contain block diagram level descriptions of functional sections within the Generator.

3. Service Sheets 1 through 57 contain detailed component-level descriptions of the circuitry within the functional sections.

8-4. TROUBLESHOOTING

8-5. General

The troubleshooting strategy employed in this manual is described in the introduction to Service Sheet A (in the Block Diagrams section).

8-6. Status Light and Status Codes

The STATUS light is a valuable troubleshooting aid but it should be used in conjunction with the other troubleshooting information in this manual. Its use and its numeric codes are described opposite Block Diagram A.

8-7. Signature Analysis

Signature analysis is a simple method of verifying the operation of digital circuitry. When properly used, signature analysis can detect extremely subtle hardware faults. Signatures must identically match those given in the signature tables located opposite the schematics. If everything is working correctly, signatures will all match exactly. If they don't match, by even one digit, something is wrong.

With the Generator's internal signature analysis routine, the signature analyzer's test probe is used to check nodes in the circuit under test. The signature analyzer converts the signals at the node into a four digit "signature", which it displays. The signature is then compared to the signature in the troubleshooting checks adjacent to the appropriate schematic. These two signatures must be identical.

Signature analysis can be speeded up if the following considerations are kept in mind:

1. Make sure that every step is performed as described in the set-up procedure. That is, make sure that the clock, start, and stop connections and triggering are correct.

Page Numbering

Pages in Section VIII are numbered in groupings of one hundred by subsection. This first subsection, that is "General Service Information", is the 8-100-grouping; the block diagrams are the 8-200-grouping; the DCU service sheets are the 8-300-grouping, etc.

Signature Analysis (Cont'd)

2. Double-check that the signatures are being taken at the correct node.
3. Make sure that the signature analyzer probe is making good contact with the pin being checked. Oxidation on pins can cause invalid signatures due to poor contacts.
4. When you think that you have found a bad signature, double check to make sure.
5. When checking a node, check that the unstable-signature indicator is not blinking.

8-8. RECOMMENDED TEST EQUIPMENT

Table 1-3 (in Volume 1) lists the equipment required for maintaining the Generator. The Critical Specification column describes the essential requirements for each piece of test equipment. Other equipment can be substituted if it meets or exceeds these critical specifications.

The Recommended Model column may suggest more than one model. The first model shown is usually the least expensive, single-purpose model. Alternate models are suggested for additional features that would make them a better choice in some applications. For example, reasons for recommending an alternate model might be:

- HP-IB programmability
  —or—
- Multi-function capability (that is, one model can replace two or more single-purpose models)

Table 1-4 presents the advantages of the alternate suggestions.

8-9. SERVICE TOOLS AND AIDS

8-10. Service Accessory Kit

A service accessory kit, Hewlett-Packard accessory number 11714A, is required for servicing and troubleshooting the Signal Generator. The service kit contains extender boards, connectors, cables, adapters and other service aids. For more details on the service accessory kit, see Table 1-5 in Volume 1.

8-11. Parts Locations

The locations of individual components mounted on printed circuit boards or other assemblies are shown adjacent to the schematic diagram on the appropriate service sheet. The part reference designator is the assembly designator plus the part designator. For example, A6R9 is R9 on the A6 assembly. For specific component descriptions and ordering information, refer to Table 6-3, Replaceable Parts in Volume 1. Chassis and frame parts, as well as mechanical parts, are identified on Figures 6-1 through 6-4.

8-12. Test Points and Adjustment Locations

Most test points and adjustments are indicated on the top covers of the individual assemblies. Test points and adjustments can also be found on the component locator photograph adjacent to the particular assembly's schematic.

8-13. Service Aids on Printed Circuit Boards

Service aids on printed circuit boards include test points, indicator lights, transistor and integrated circuit and relay designations, adjustment names, and assembly part numbers.

8-14. Pozidriv Screwdrivers

Many screws in the instrument appear to be Phillip's types, but are not. To avoid damage to the screw slots, Pozidriv screwdrivers should be used. HP 8710-0899 is the No. 1 Pozidriv. HP 8710-0900 is the No. 2 Pozidriv.

8-15. Tuning Tools

For adjustments requiring non-metallic tuning tools, use the HP 8710-0033 blade tuning tool or the HP 8710-1010 (JFD Model No. 5284) hex tuning tool. For other adjustments an ordinary small screwdriver or suitable tool is sufficient. No matter which tool is used, never force any adjustment control. This is especially critical when adjusting variable inductors or capacitors.

8-16. Silver Solder

Silver solder must be used whenever soldering mono-block capacitors and resistors (small, leadless components) to printed circuit boards. This restriction is due to the lower temperature requirements of the components. A small amount of silver solder is first applied to the printed circuit board at the mono-block connection points. The component is then laid down on the board with its silvered ends touching the pre-soldered printed circuit traces. Just enough heat must then be applied to the solder to make it melt and adhere to the ends of the block.

8-17. REPAIR

8-18. Factory-Selected Components (*)

Some component values are selected at the time of final checkout at the factory (see Table 5-1 in

Factory-Selected Components (*)(Cont'd)

Volume 1). These values are selected to provide optimum compatibility with associated components. These components are identified on individual schematics and the parts list by an asterisk (*).

8-19. Manual Backdating (†)

A dagger (†) by an item of service information means that information is different for Generators with serial number prefixes lower than the one that this manual applies to directly. Table 7-1 in Volume 1 lists the backdating changes by serial number prefix. The backdating changes are contained in Section VII. Recommended modifications are also contained in Section VII.

8-20. Disassembly Procedures

Procedures for removal of the top, bottom and side covers, and the front and rear panels of the instrument are described on the last foldout in Volume 2. The descriptions for disassembly of the rear panel is accompanied with an IPB (that is, an Illustrated Parts Breakdown). Additional IPB's are located at the end of Section VI (Replaceable Parts) in Volume 1.

8-21. Post-Repair Adjustments and Performance Tests

Table 5-2 (in Volume 1) describes the adjustment procedures that are related to repair or replacement of individual assemblies. Table 4-1 (also in Volume 1) describes the performance tests that are

Table 8-101. Etched Circuit Soldering Equipment

Item	Use	Specification	Item Recommended	HP Part No.
Soldering Tool	Soldering, Heat Staking	Wattage: 35W Tip Temp.: 390°-440°C (735°-825°F)	Ungar No. 135 Ungar Division Eldon Ind. Corp. Compton, CA 90220	8690-0167
Soldering Tip	Soldering, Unsoldering	* Shape: Chisel	*Ungar PL113	8690-0007
Soldering Tip	Heat Staking	Shape: Cupped	HP 5020-8160 or modified Ungar PL111 (See figure 8-2)	5020-8160
De-Soldering Aid	To remove molten solder from connection	Suction Device	Soldapullt by Edsyn Co., Van Nuys, CA 91406	8690-0060
Rosin (flux) Solvent	To remove excess flux from soldered area before application of protective coating	Must not dissolve etched circuit base board	Freon	8500-0232
Solder	Component replacement; Circuit Board repair wiring	Rosin (flux) core, high tin content (63/37 tin/lead), 18 gauge (SWG) 0.048 in. diameter preferred.		8090-0607
Silver Solder	Mono-block replacement	Rosin (flux) core, silver saturated tin/lead alloy 0.031 in. diameter.	X25 Rosin Core DIVCO 233 Division Lead Co. Summit, IL 60501	8090-0022

* For working on circuit boards; for general purpose work, use No. 555 Handle (8690-0261) and No. 4037 Heating Unit 47½ - 56½ W (HP 8690-0006); tip temperature of 850° - 900°F; and Ungar No. PL113 1/8" chisel tip.

Post-Repair Adjustments and Performance Tests (Cont'd)

related to repair or replacement of individual assemblies.

8-22. Post-Service Product Safety Checks

Visually inspect interior of instrument for any signs of abnormal internally generated heat, such as discolored printed circuit boards or components, damaged insulation, or evidence of arcing. Determine and remedy cause of any such condition.

Using a suitable ohmmeter, check resistance from instrument enclosure to ground pin on power cable plug. The reading must be less than one ohm. Flex the power cable while making this measurement to determine whether intermittent discontinuities exist.

Check any indicated front or rear panel ground terminals marked, using the above procedure.

Check resistance from instrument enclosure to the line and neutral (tied together) with the power switch on and the power source disconnected. The minimum acceptable resistance is two megohms. Replace any component which results in a failure.

8-23. Etched Circuits (Printed Circuit Boards)

The etched circuit boards in the Generator have plated-through holes which make a solderable path through to both sides of the insulating material. Soldering can be done from either side of the board with equally good results. When soldering to any circuit board, keep in mind the following recommendations:

1. Avoid unnecessary component substitution. Substitution can result in damage to the circuit board and/or adjacent components.

2. Do not use a high-power soldering iron on etched circuit boards. Excessive heat may lift a conductor or damage the board.

3. Use a suction device or wooden toothpick to remove solder from component mounting holes. DO NOT USE A SHARP METAL OBJECT SUCH AS AN AWL OR TWIST DRILL FOR THIS PURPOSE. SHARP OBJECTS MAY DAMAGE THE PLATED-THROUGH CONDUCTOR.

8-24. MOS and CMOS Integrated Circuit Replacement

MOS and CMOS integrated circuits are used in this instrument. They are prone to damage from both static and transients and must be handled carefully. When working on the Generator, keep in mind the following recommendations to avoid damaging these sensitive components.

1. Do not remove any board unless the Generator has been turned off or unplugged.
2. When removing a socketed MOS or CMOS device from an assembly, be careful not to damage it. High-grip sockets are used throughout the instrument. Avoid removing devices from these sockets with pullers. Instead, use a small screwdriver to pry the device up from one end, slowly pulling it up one row of pins at a time.
3. Once a MOS or CMOS device has been removed from an assembly, immediately stick it into a pad of conductive foam or other suitable holding medium.
4. When replacing a MOS or CMOS device, ground the foam on which it resides to the instrument before removing it. If a device requires soldering, make sure that the assembly is lying on a sheet of conductive foam, and that the foam and soldering iron tip are grounded to the assembly. Apply as little heat as possible.
5. Before turning the instrument off, remove any large ac sources which may be driving MOS switches.

8-25. LOGIC SYMBOLOGY

8-26. Basic Definitions

The logic symbols used in this manual are based on the American National Standard Institute (ANSI) Y32.14-1973, "Graphic Symbols for Logic Diagrams (Two State Devices)". A summary of this symbology is provided to aid in interpreting these symbols.

This section includes a brief description of the basic logic symbols used on the service sheets (see Figure 8-101), a summary of indicator symbols (see Figure 8-102), a discussion of contiguous blocks, control blocks, and dependency notation, and a summary of symbology for some of the more complex devices.

Qualifiers. Qualifiers are that portion of a device symbol that denotes the logic function. For exam-

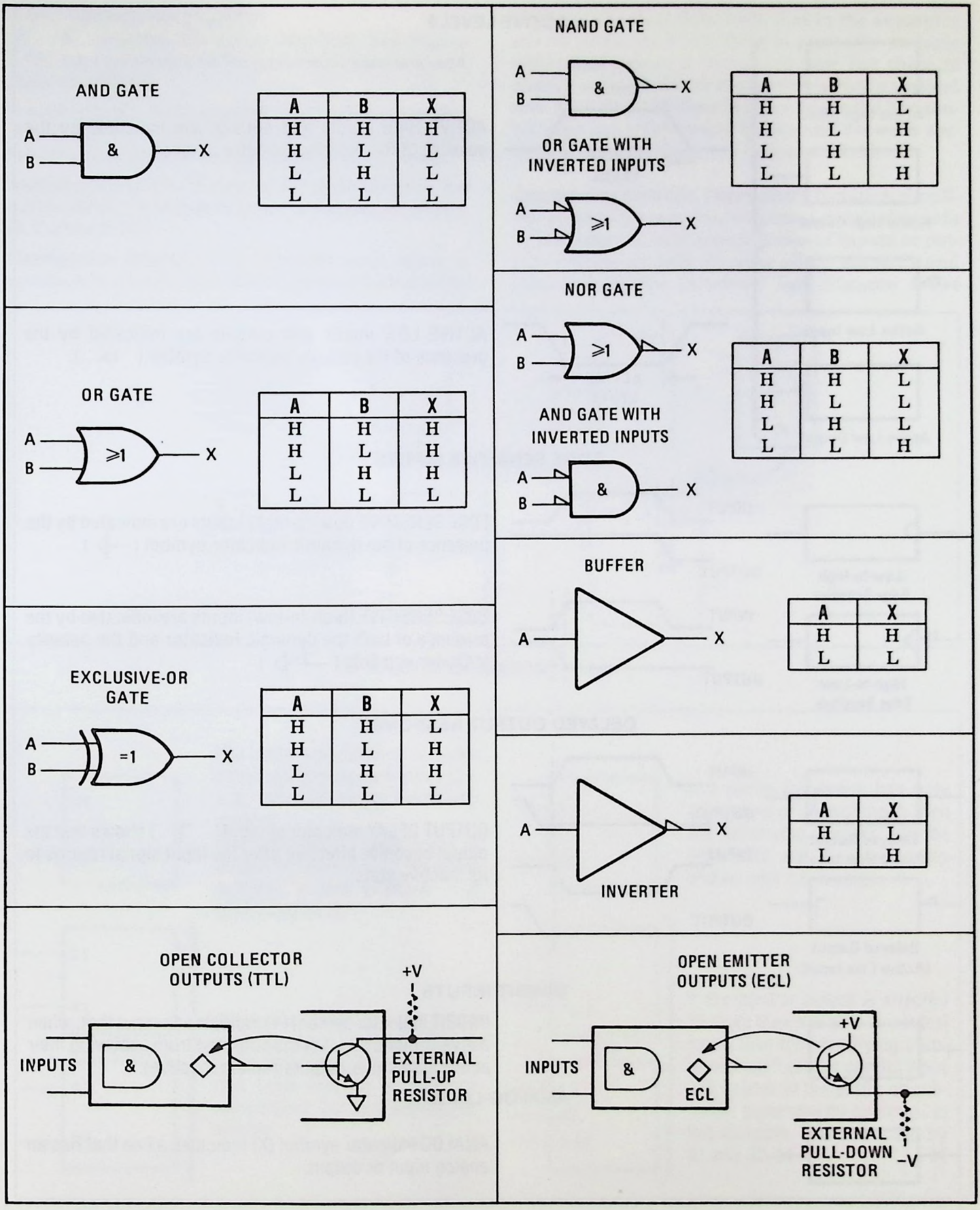


Figure 8-101. Basic Logic Symbols and Qualifiers

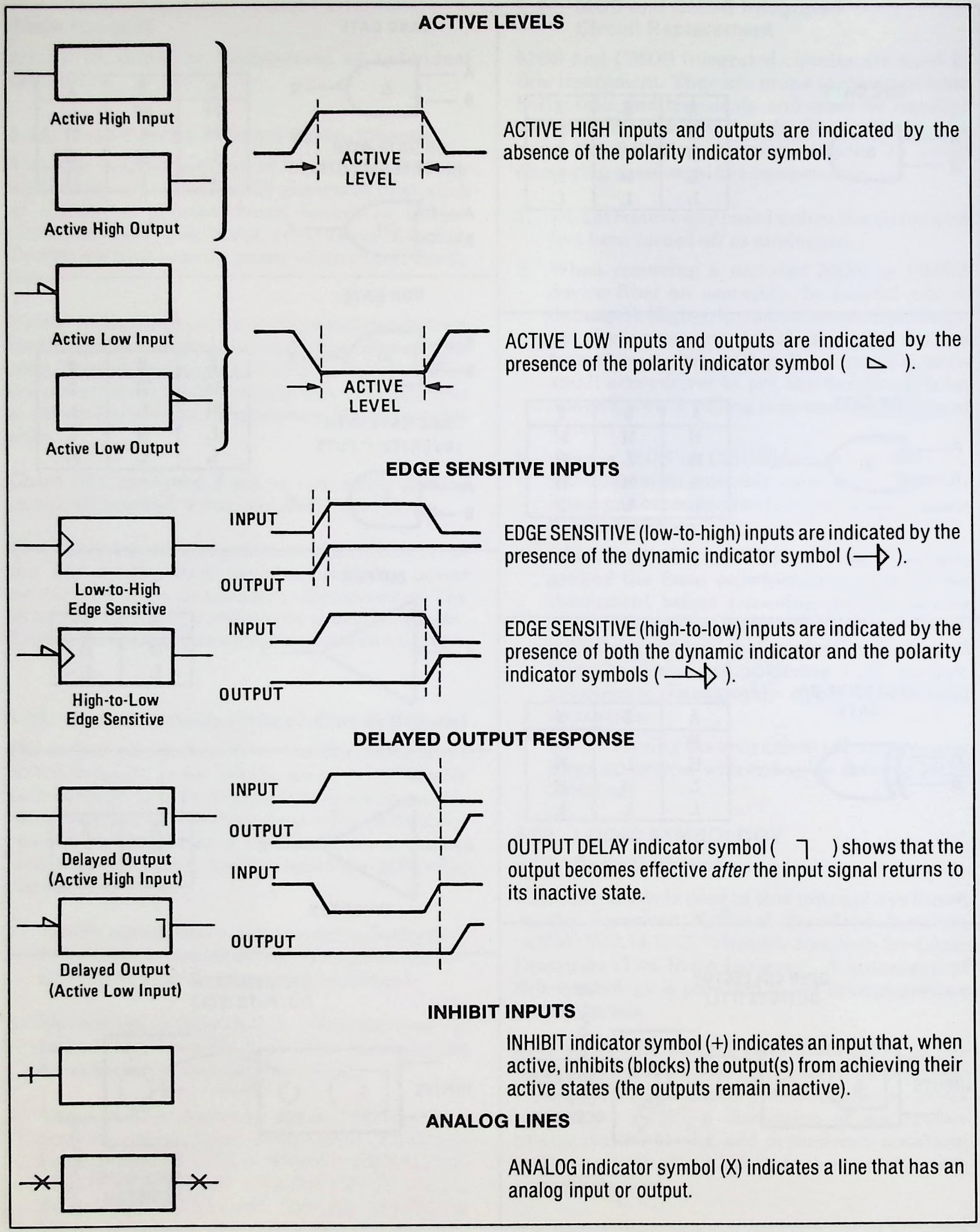


Figure 8-102. Indicator Symbols

Basic Definitions (Cont'd)

ple, "&" denotes the AND function. See Figure 8-101 for a summary of the basic logic symbols and their qualifiers.

Power supply and ground connections are not shown on the symbols. This information is tabulated on the right margins of the service sheets.

Indicator Symbols. Indicator symbols identify the active state of a device's input or output, as shown in Figure 8-102.

Contiguous Blocks. Two symbols may share a common boundary parallel or perpendicular to the direction of signal flow. Note that in the examples shown in Figure 8-103, there is generally no logic connection across a horizontal line, but there is always an implied logic connection across a vertical line. Notable exceptions to this rule are the horizontal lines beneath control blocks and between sections of shift registers and counters (dividers).

Dependency Notation. Dependency Notation simplifies symbols for complex integrated circuit elements by defining the interdependencies of inputs or outputs without actually showing all the elements and interconnections involved (see Figures 8-104

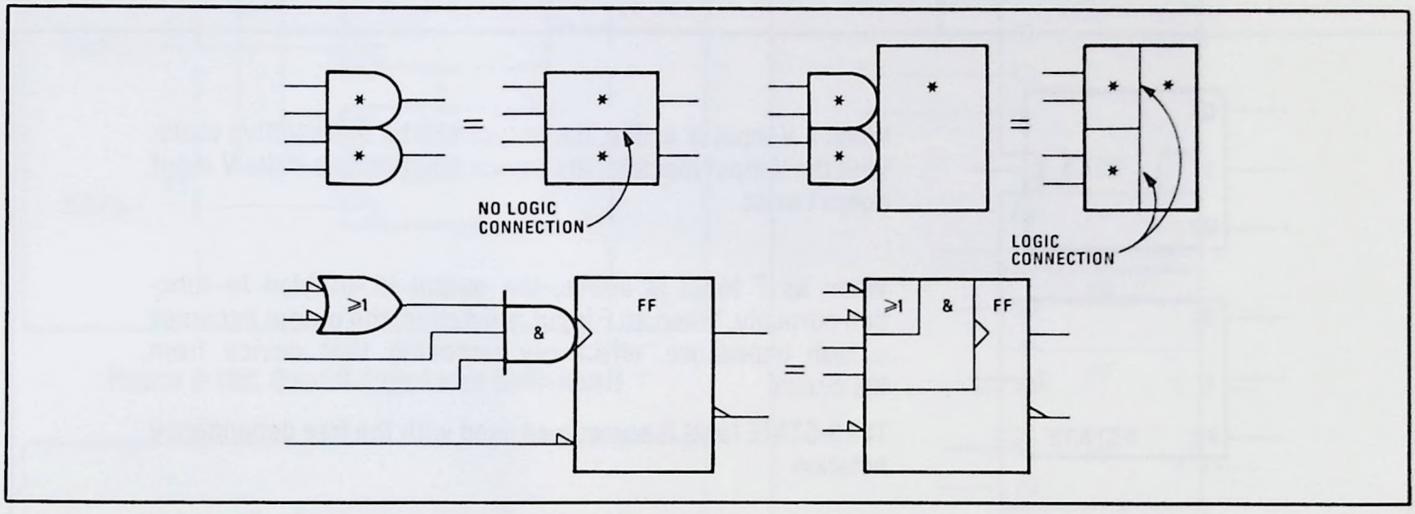


Figure 8-103. Contiguous Blocks

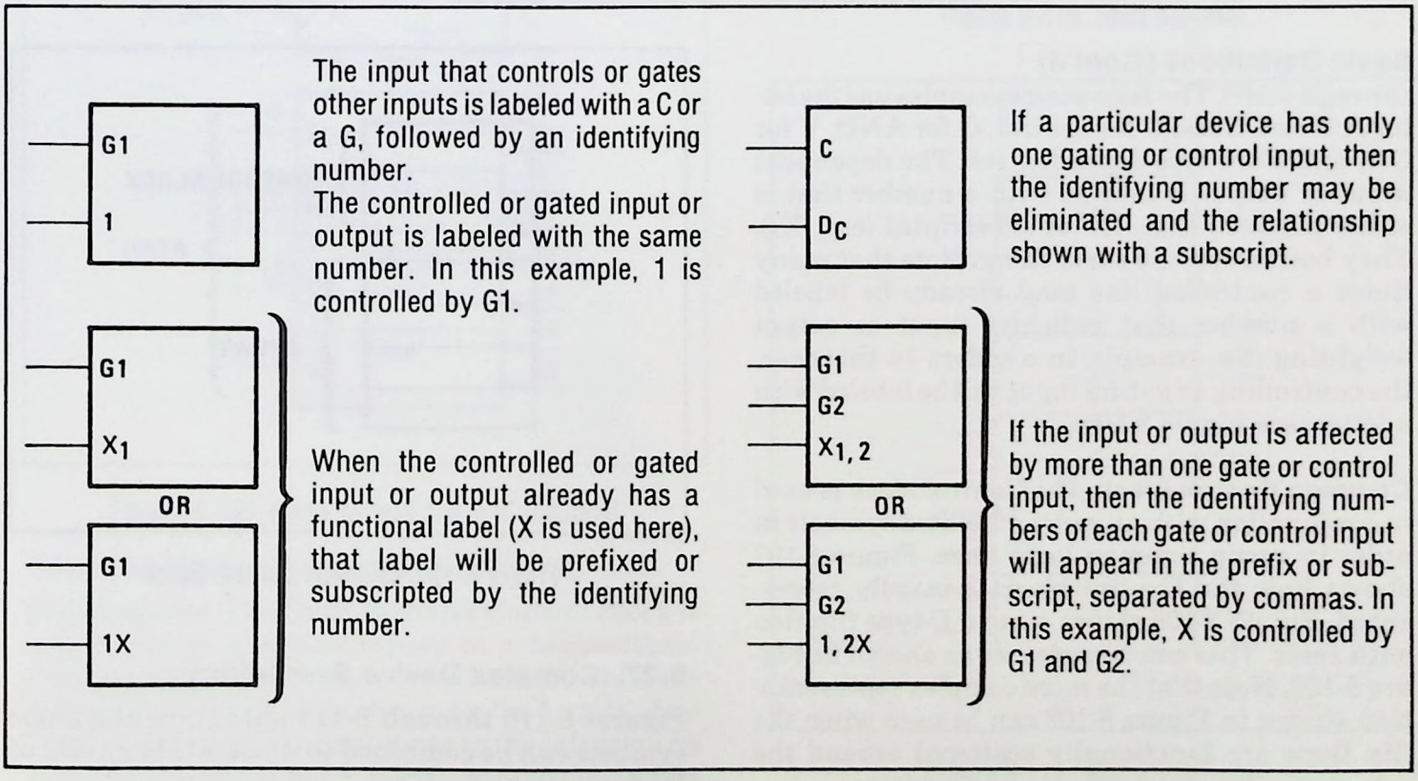


Figure 8-104. AND Dependency Notation

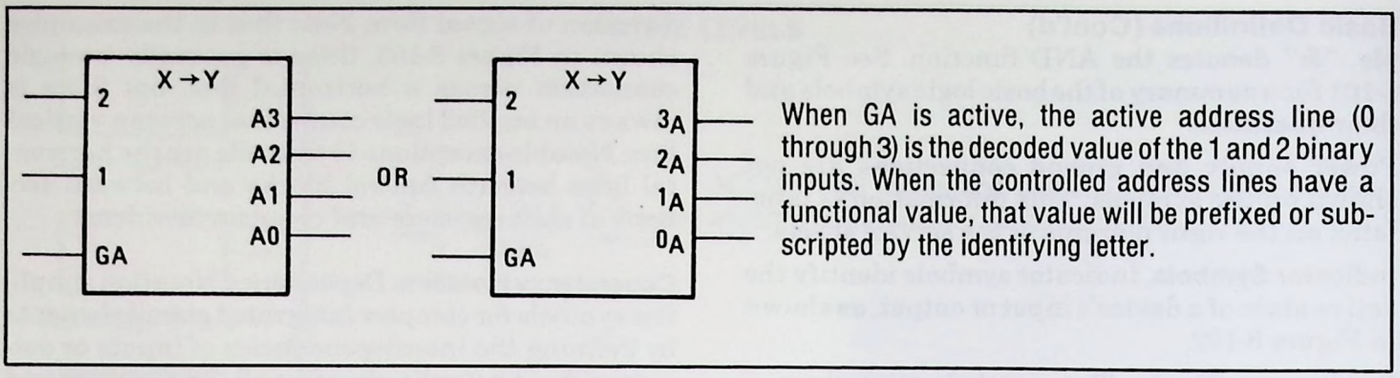


Figure 8-105. Address Dependency Notation: Coder Example Using Alpha Characters (Letters)

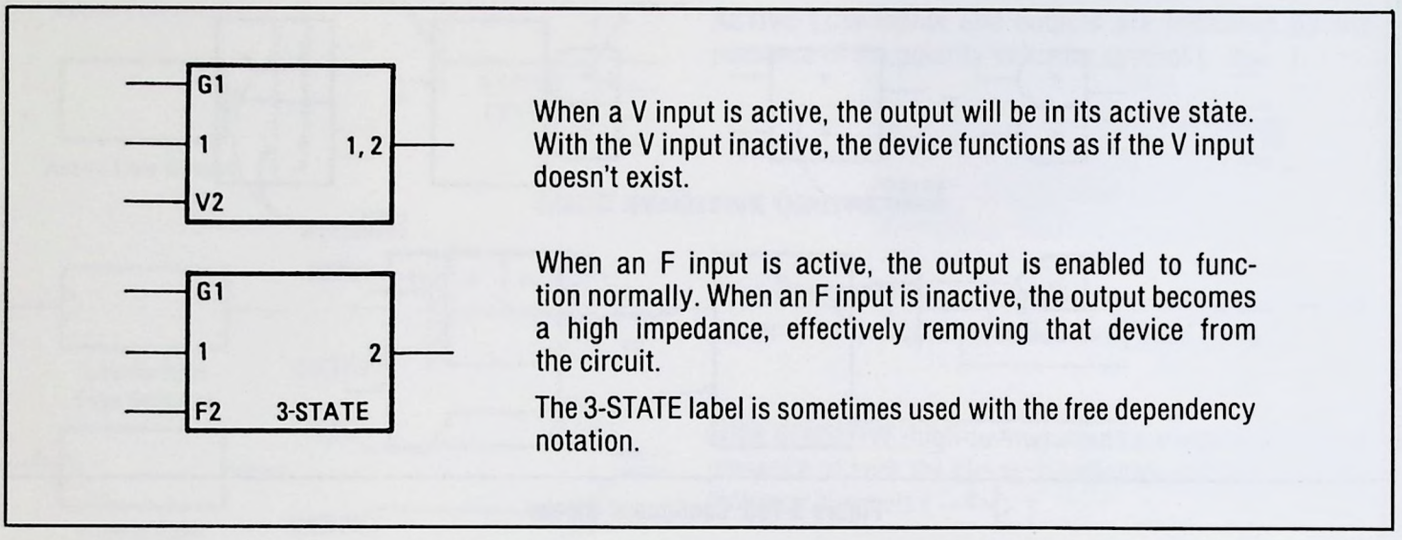


Figure 8-106. OR and Free Dependency Notation

Basic Definitions (Cont'd)

through 8-106. The following examples use the letter A for address, C for control, G for AND, V for OR, and F for free dependencies. The dependent input or output is labeled with a number that is either prefixed (e.g., 1X) or subscripted (e.g., X_1). They both mean the same thing. Note that many times a controlled line may already be labeled with a number that indicates input or output weighting (for example, in a coder). In this case, the controlling or gating input will be labeled with a letter (see Figure 8-105).

Common Control Block. The Control block is used in conjunction with an array of related symbols in order to group common logic lines. Figure 8-107 shows how the Control block is usually represented. Figure 8-108 shows a quad D-type flip flop with reset. This can be redrawn as shown in Figure 8-109. Note that the more complex representation shown in Figure 8-108 can be used when the flip flops are functionally scattered around the schematic (i.e., not used as a quad unit).

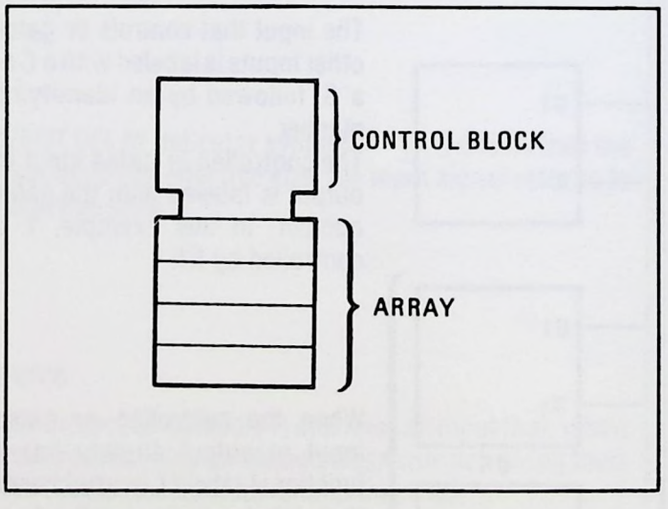


Figure 8-107. Common Control Block

8-27. Complex Device Symbology

Figures 8-110 through 8-113 show how the basic symbols can be combined to illustrate behavior of fairly complex devices.

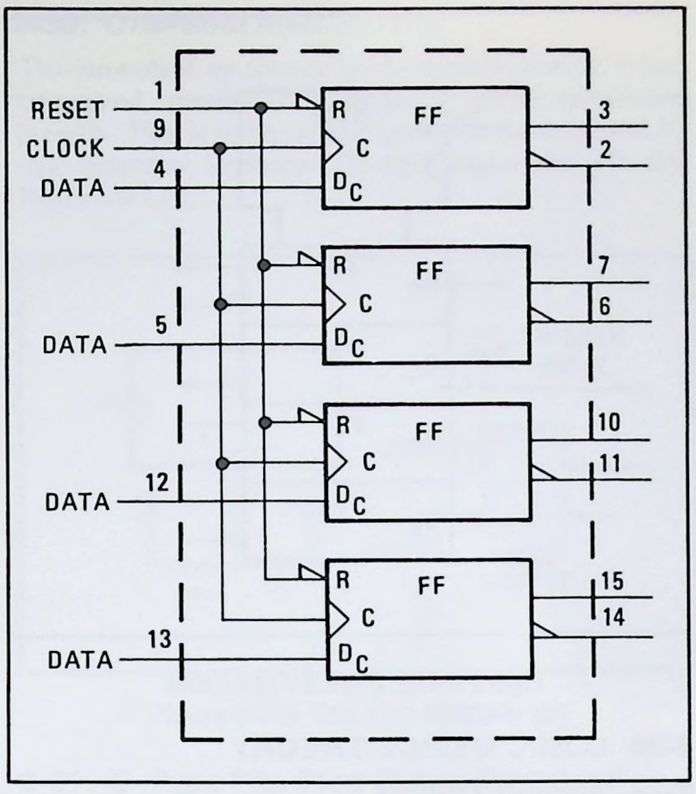


Figure 8-108. Quad D-Type Latch (Individual)

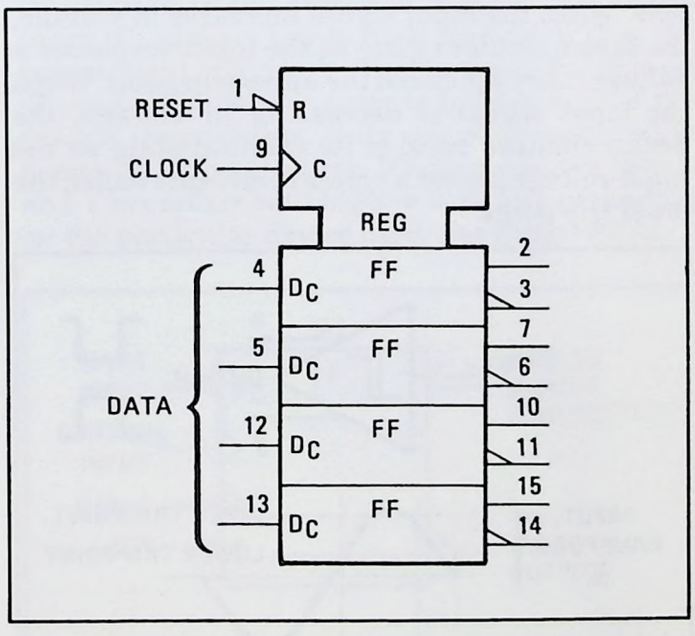


Figure 8-109. Quad D-Type Latch (Combined)

Complex Device Symbology (Cont'd)

Shift Register. The Shift Register Control Block is used to show common inputs to a bidirectional shift register. Notice that "–m" means shift the contents to the right or down by "m" units. And "–m" means shift the contents to the left or up by "m" units. Note: If m = 1, it may be omitted. Inputs "a" and "b" are each single IC pins that have two functions. Input "a" enables one of the inputs to the top D-type flip-flop (1D) and also shifts the register contents down "m" units. Input "b" enables one of the inputs to the bottom flip-flop (2D), and also shifts the register contents up "m" units. Input "c" loads all four flip-flops in parallel (3D). Input "d" is a common reset. The output delay

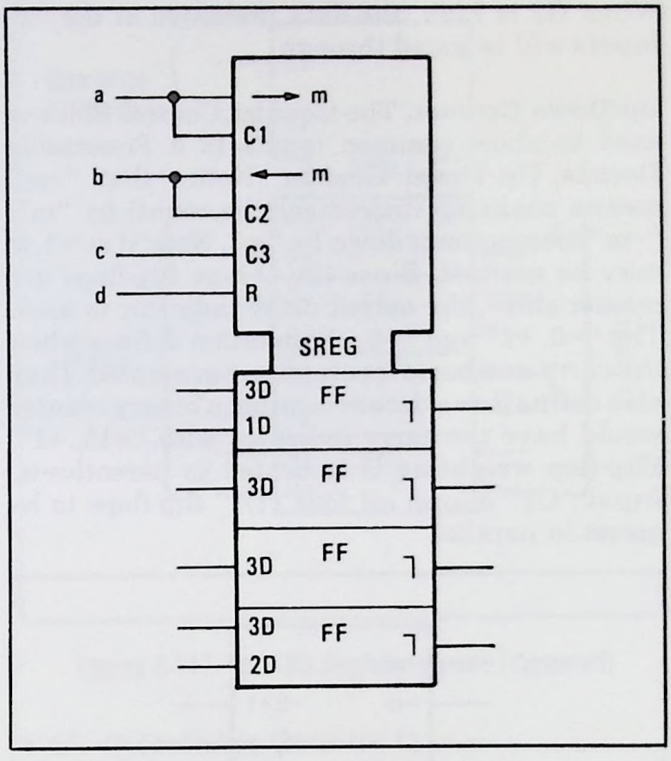


Figure 8-110. Shift Register

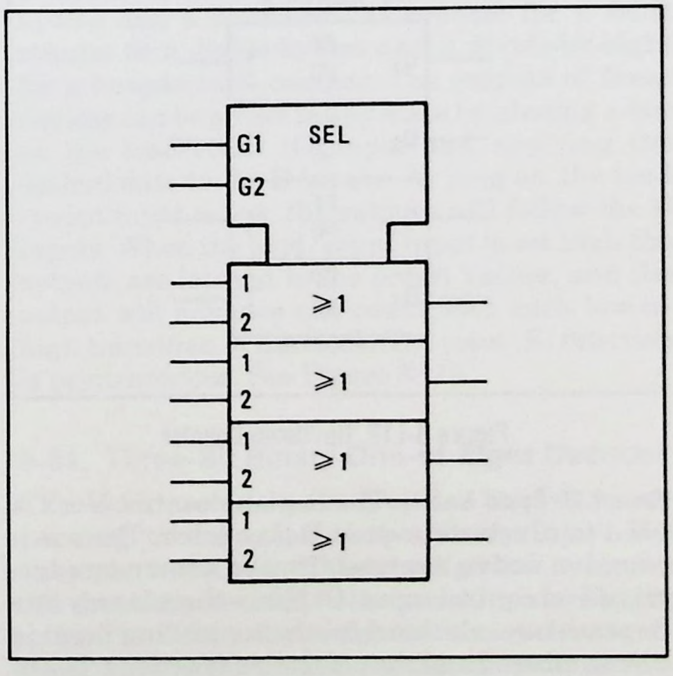


Figure 8-111. AND-OR Selector

Complex Device Symbology (Cont'd)

indicator is used because these are master slave flip-flops.

AND-OR Selector. The Selector Control Block is used to simplify the AND portion of a quad AND-OR select gate. When G1 is high, the data presented at the "1" inputs will be gated through. When G2 is high, the data presented at the "2" inputs will be gated through.

Up/Down Counter. The Counter Control Block is used to show common inputs to a Presettable Decade Up/Down Counter. Notice that "+m" means count up (increment the count) by "m"; "–m" means count down by "m". Note: if m = 1, it may be omitted. Since the D-type flip-flops are master-slave, the output delay indicator is used. The "=9, +1" and "=0, –1" notation defines when the carry and borrow outputs are generated. They also define it as a decade counter; a binary counter would have the carry indicated with "=15, +1". Flip-flop weighting is indicated in parenthesis. Input "C1" allows all four "D1" flip-flops to be preset in parallel.

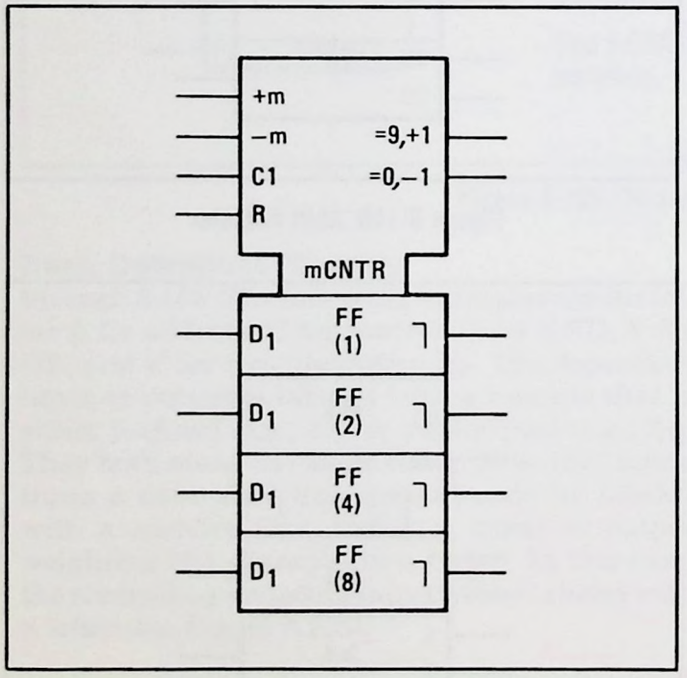


Figure 8-112. Up/Down Counter

Quad D-Type Latch. The Register control block is used to illustrate a quad D-type latch. There is a common active-low reset (R), and a common edge-triggered control input (C). Since there is only one dependency relationship, the controlling input is not numbered and the controlled functions (D) are subscripted with a C.

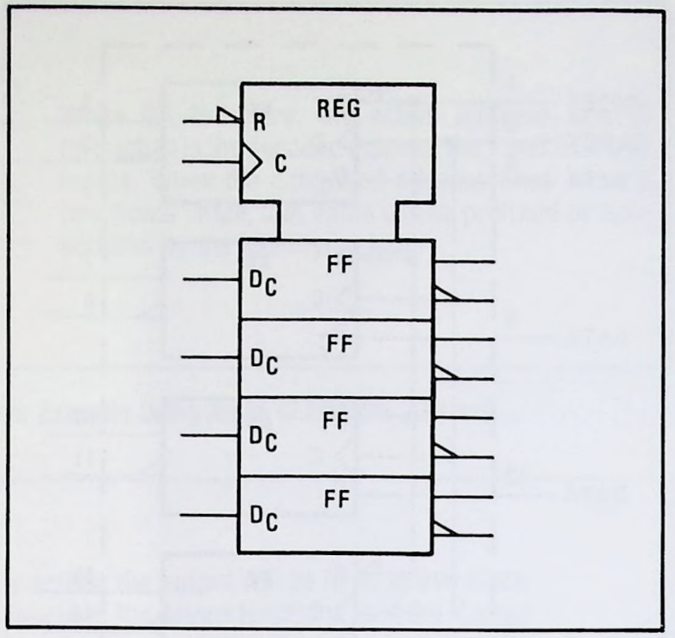


Figure 8-113. Quad D-Type Latch

8-28. LOGIC DEVICE THEORY

8-29. Schmitt Trigger

A typical Schmitt trigger is shown in Figure 8-114. Some Schmitt triggers have complimentary outputs. When the input signal increases in voltage, the device changes state as the input surpasses a voltage reference called the upper trip point. When the input signal is decreasing in voltage, the device changes back to its original state as the input voltage passes a voltage reference called the lower trip point.

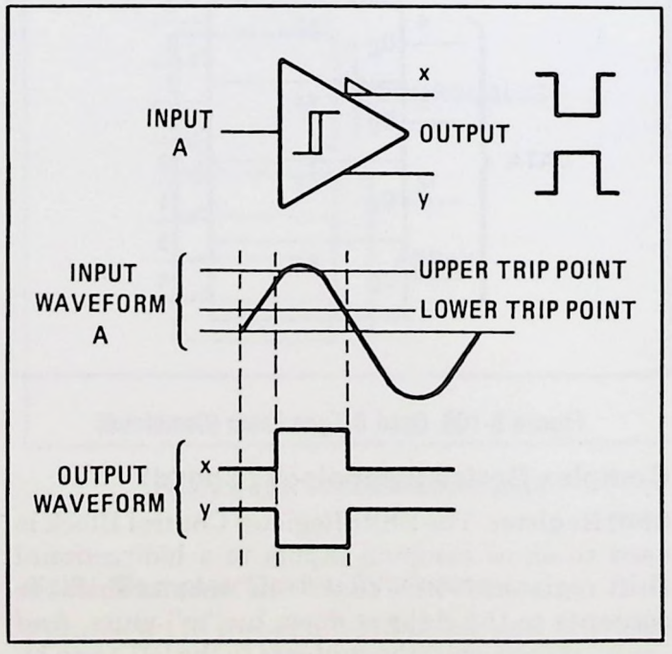


Figure 8-114. Schmitt Trigger

8-30. One-Shot Multivibrator

The one-shot or monostable multivibrator, when triggered, produces a pulse of pre-programmed length. The length of the pulse is determined by the external resistor (R) and capacitor (C). See Figure 8-115.

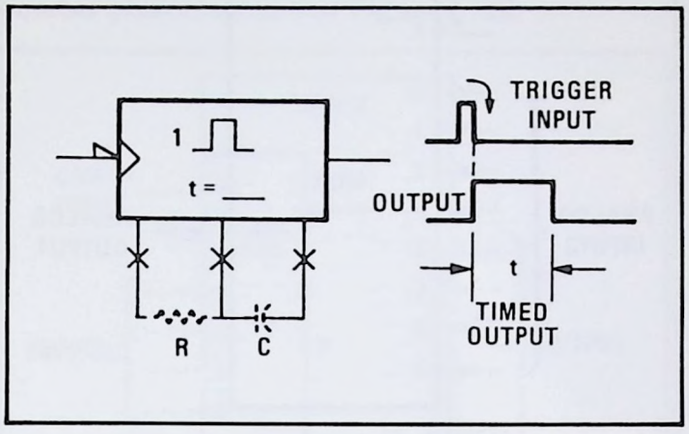


Figure 8-115. One-Shot Multivibrator

8-31. D-Type Flip-Flop (Edge-Triggered)

D-type flip-flops are used for temporary storage of one bit of binary data. The D_C input is stored and transferred to the output at X when the control input (C) gives a low-to-high transition. Y is the complement of X (i.e., Y=X). The S and R inputs set (S) and reset (R) the outputs independent of the control input status. Only one of these inputs is normally active at a time. If both are active, then X and Y are either both high or both low, depending on the particular device used. See Figure 8-116.

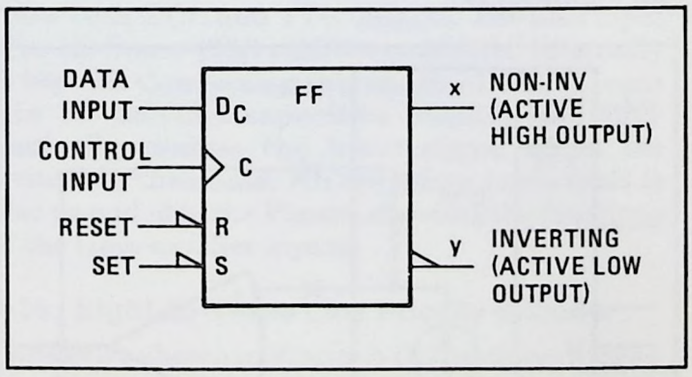


Figure 8-116. D-Type Flip-Flop (Edge-Triggered)

8-32. Four-Bit Register (Level-Triggered)

A four-bit register is used for temporarily storing four bits of binary data. Data at the D_1 inputs are stored when clocked by the C_1 control input. Data at the D_2 inputs are stored when clocked by the C_2 control input. The outputs follow the inputs as long as the control inputs remain high. When the control inputs are low, the data that was present at the D inputs (when the control inputs were low) are retained (latched) at the outputs until the control inputs go high again. See Figure 8-117.

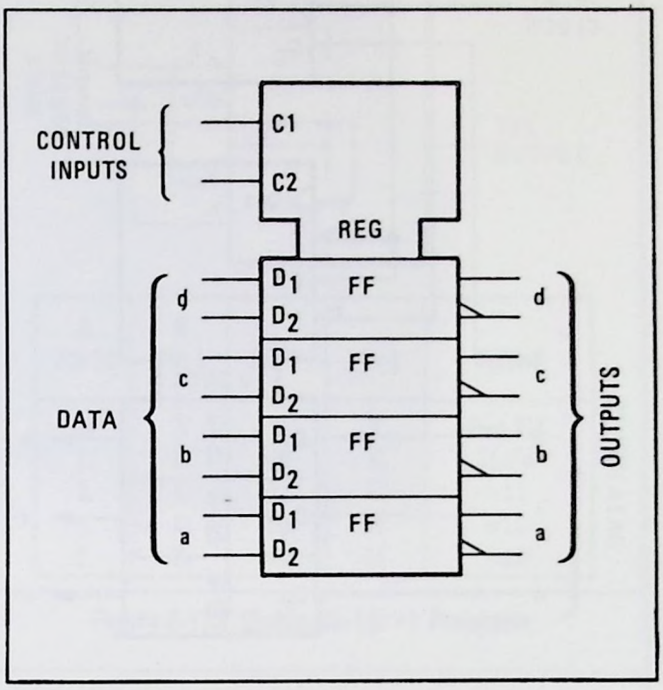


Figure 8-117. Four-Bit Register (Level-Triggered)

8-33. Presettable Counter

Presettable counters consist of four D flip-flops which are internally connected to provide a divide-by-two and a divide-by-five counter for a BCD counter or a divide-by-two and a divide-by-eight for a hexadecimal counter. The outputs of these devices can be preset to any state by placing a low on the load/count (C) input and applying the desired data to the D inputs. As long as the load /count input is low, the outputs will follow the D inputs. When the load/count input is set high the outputs are latched to the preset values, and the output will advance one count with each low-to-high transition of the clock. The reset (R) function is asynchronous. See Figure 8-118.

8-34. Three-Bit Binary One-of-Eight Decoder

This device selects an output line (1-of-8) corresponding to the value of the binary input. For example, to make the 5G output go low, a binary 101 must be presented to the select inputs. For the output to reflect the weighted binary input, all three lines to the control section must be active. See Figure 8-119.

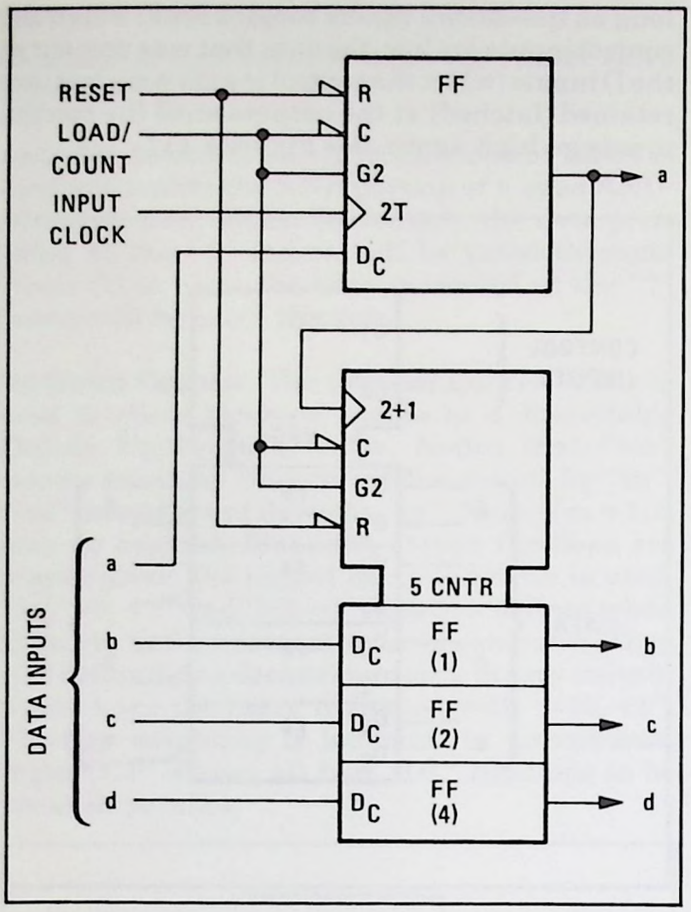


Figure 8-118. Presettable Counter

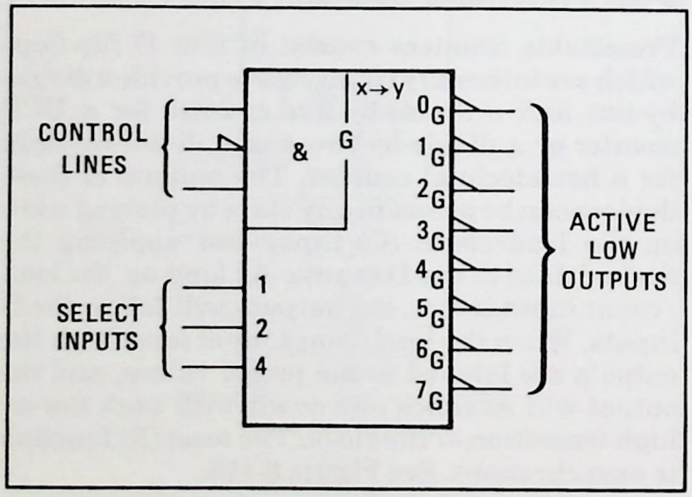


Figure 8-119. Three-Bit Binary One-of-Eight Decoder

8-35. Analog Multiplexer

This device is the electonic version of a single-pole-eight-throw (SP8T) switch. The binary code at the select inputs determines which analog input (1-of-8) will be routed to the output. The output is enabled by the F input. See Figure 8-120.

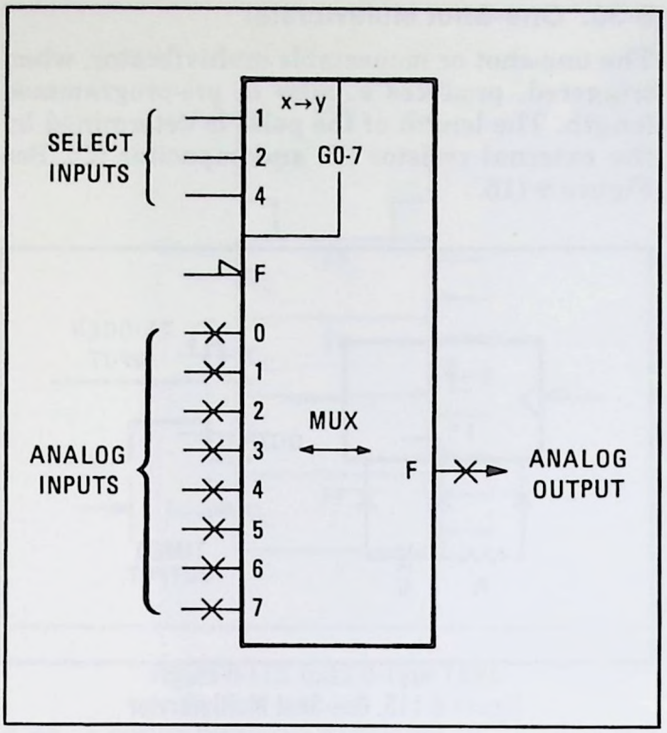


Figure 8-120. Analog Multiplexer

8-36. Digital-to-Analog Converter

The Digital-to-Analog Converter is used with an operational amplifier to provide digital control of an analog signal. The analog source (that is, V_{REF}) can be either ac or dc. The Digital-to-Analog Converter produces a variable current output where maximum current is produced when Y=1000. The output of the operational amplifier is a voltage directly proportional to V_{REF} and the value of Y. See Figure 8-121.

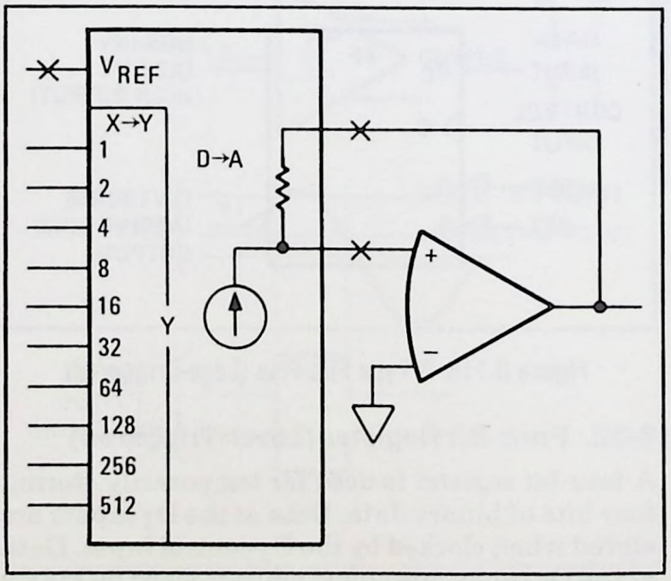


Figure 8-121. Digital-to-Analog Converter

8-37. Four-Bit BCD Summer

This device produces the BCD sum of two decimal numbers presented in the 8-4-2-1 weighted BCD format. Carry Output and Carry Input are provided for cascading. For valid BCD numbers (0 to 9) at the inputs the BCD sum is formed at the outputs. Input numbers 10 to 15 yield a valid BCD number plus a carry. See Figure 8-122.

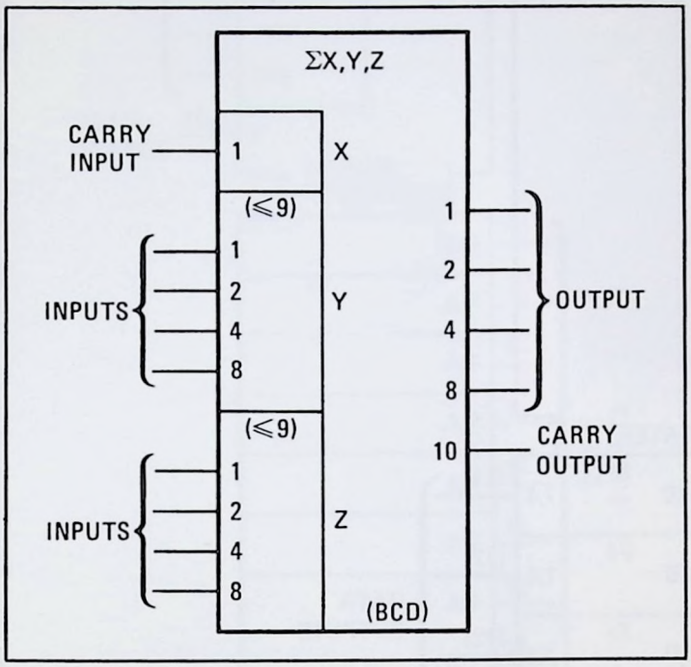
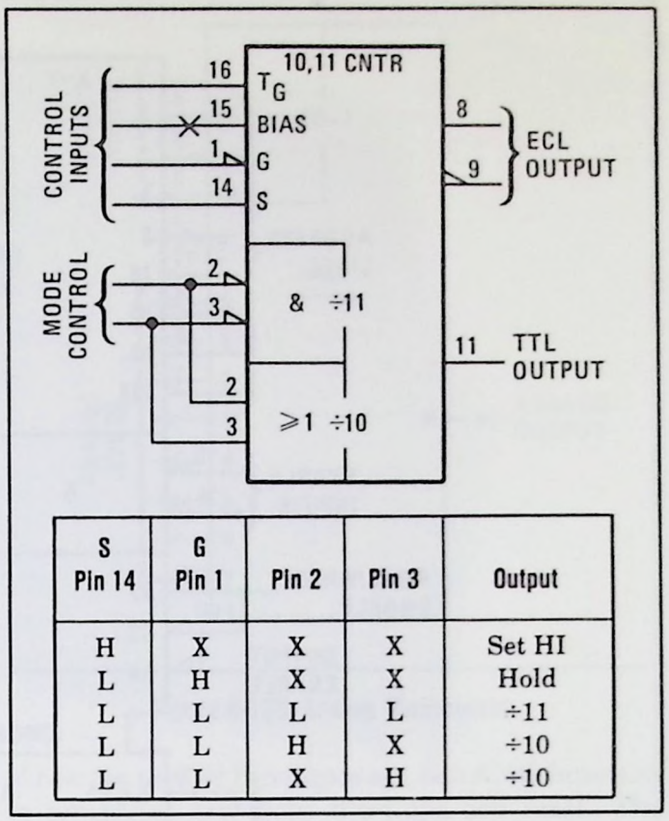


Figure 8-122. Four-Bit BCD Summer

8-38. Divide-by-10/11 Prescaler

The ÷10/11 Prescaler will divide by 10 or 11 (see Figure 8-123). The mode control inputs (pins 2 and 3) control the division ratio. The Prescaler provides both ECL and TTL outputs. The bias input (Pin 15) has a 400Ω resistor connected internally to the V_{BB}. Connecting this resistor to the T_G input (pin 16) provides capacitive coupling and automatically centers the input signal about the switching threshold. An operating mode table is also provided in the Figure, showing the functions of the Gate and Set inputs.



S Pin 14	G Pin 1	Pin 2	Pin 3	Output
H	X	X	X	Set HI
L	H	X	X	Hold
L	L	L	L	÷11
L	L	H	X	÷10
L	L	X	H	÷10

Figure 8-123. Divide-By-10/11 Prescaler

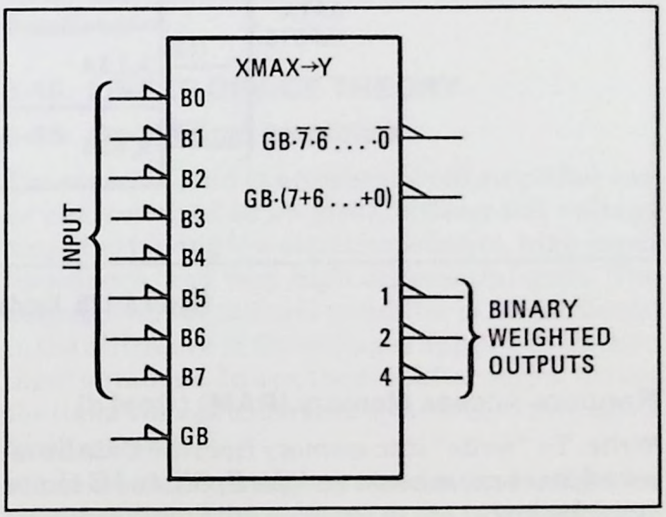


Figure 8-124. Eight-to-Three Line Priority Encoder

8-39. Eight-to-Three Line Priority Encoder

The device shown in Figure 8-124 produces a three-line binary weighted output as a result of one active input. If more than one input line is active, the output will be the binary equivalent of the highest valued input (for example, if the input lines B4 and B6 are both active, the output would be 110 or binary 6). Two additional outputs are provided: one is active when any data line and GB are active; the other output is active when only GB is active. All lines are active-low.

8-40. Random Access Memory (RAM)

The device shown in Figure 8-125 is a 256 by 4-bit static memory. Each of the 4-bit memory locations are addressed by the eight address lines. Both F inputs must be low to enable either memory mode (that is, "write" or "read"). When either F input is high the Data lines are in the three-state condition (that is, high impedance). The Data Inputs and Outputs are shown functionally as separate lines. However, each Input-Output function occurs physically on one pin.

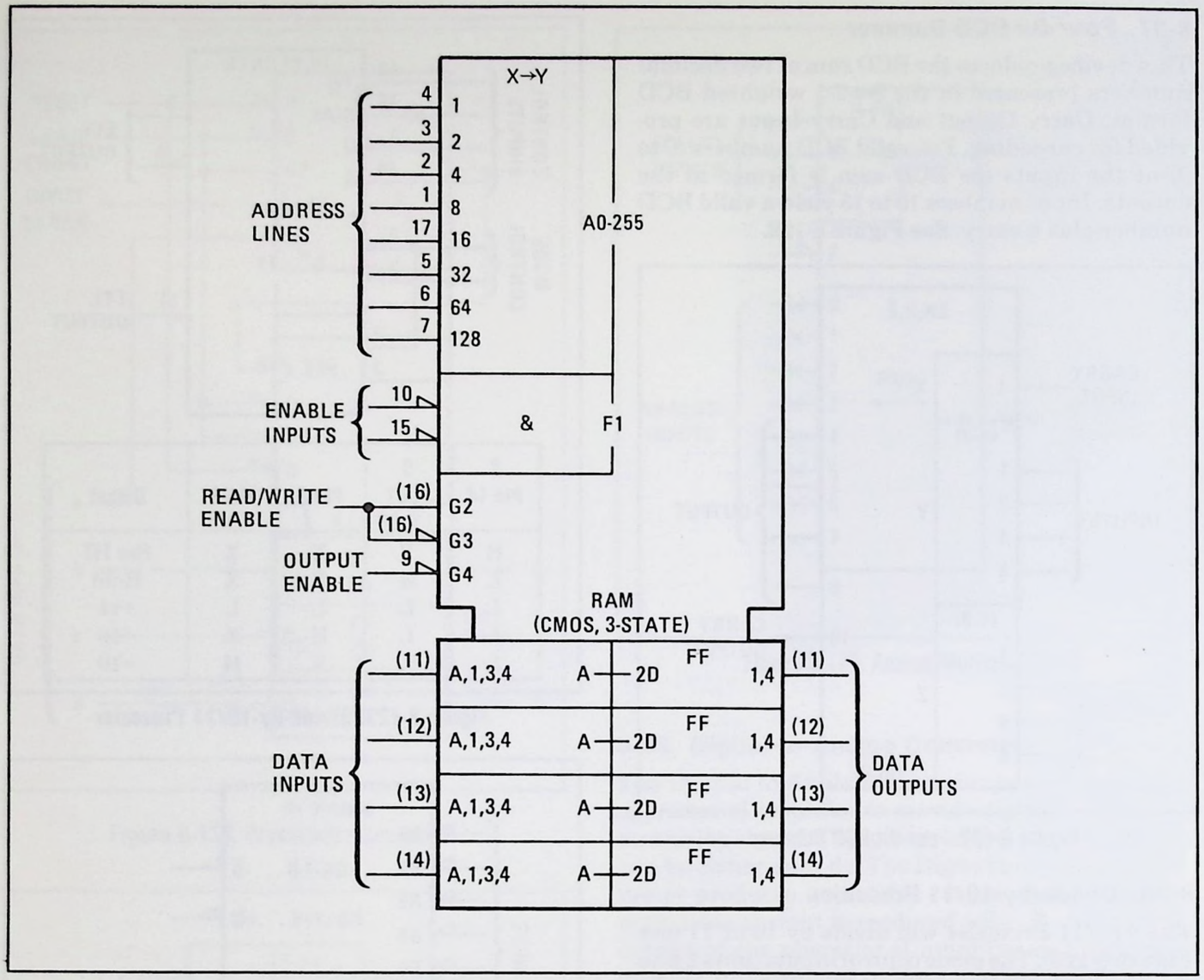


Figure 8-125. Random Access Memory (RAM)

Random Access Memory (RAM) (Cont'd)

Write. To "write" into memory from the Data lines, an address must be set and the F, G3, and G4 lines must be low.

Read. To "read" from memory to the output latches (FF) and then to the Data lines, an address must be set, G2 must be high, and the F and G4 lines must be low.

8-41. Read-Only Memory (ROM)

The device shown in Figure 8-126 has 512 preprogrammed 8-bit memory locations. The memory locations are addressed by the nine binary address lines. The F input must be low to enable the Data Outputs. Otherwise, the outputs are in the three-state conditon (that is, high impedance).

8-42. Analog Switch

The analog switch is a bi-directional device, as is indicated by the double-ended arrow. The F1 input is the gate. F1 indicates the input and output (labeled with "1's") are dependent on this input. See Figure 8-127.

8-43. Analog Multiplexer

The device shown in Figure 8-128 is an electronic version of a Single-Pole-Eight-Throw switch (SP8T). The binary code at the Select Inputs determines which analog signal, 0 through 7, will be routed to the output. The F input must be low to enable the output. Otherwise, the output will be in the three-state condition (that is, high impedance).

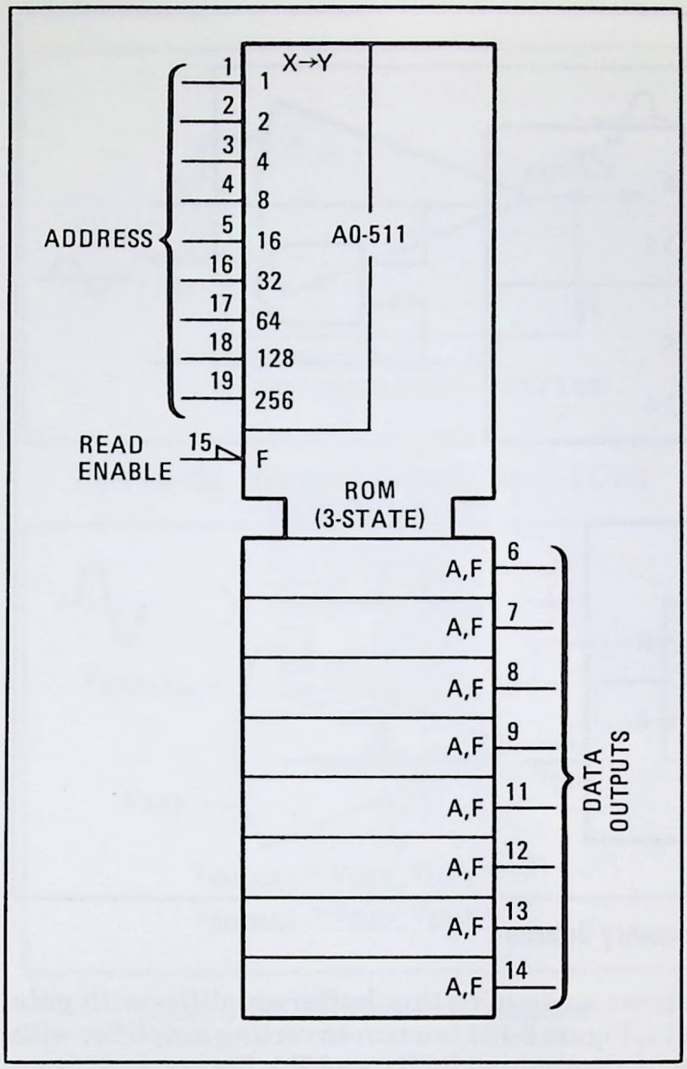


Figure 8-126. Read-Only Memory (ROM)

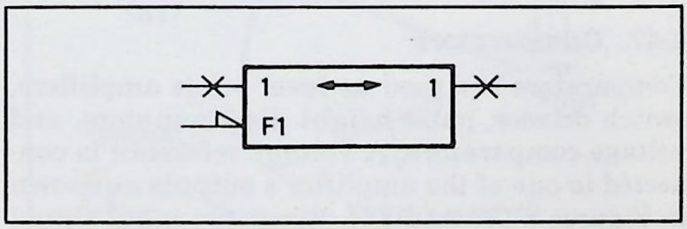


Figure 8-127. Analog Switch

8-44. Phase-Frequency Detector

The device shown on the left side of Figure 8-129 can also be shown as it is on the right. It contains two RS flip-flops. The reference and variable signals drive the Set inputs. The latched outputs are AND'ed to reset the flip-flops.

The output signal for two out-of-phase input signals (or two signals of different frequency) would be a pulse on one line due to the first flip-flop being set. The pulse width would be equal to the time difference between the two active Set inputs.

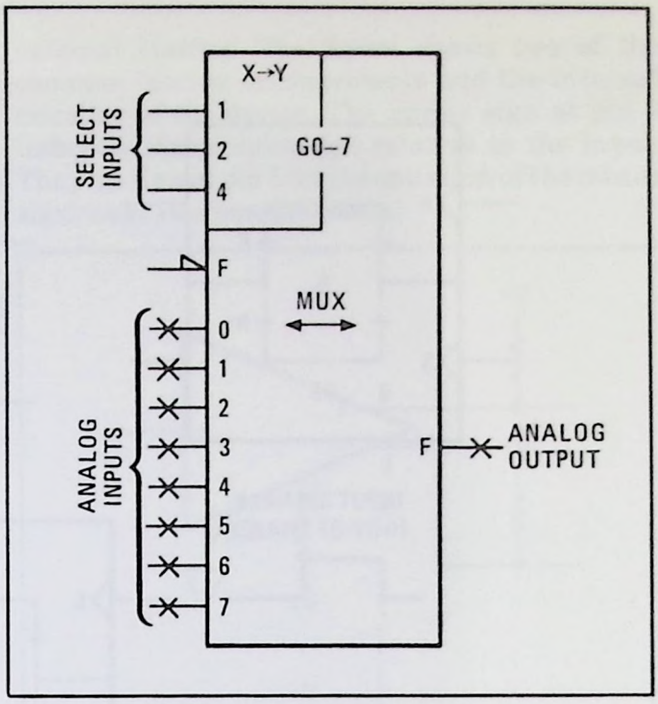


Figure 8-128. Analog Multiplexer

When the second flip-flop is set, the AND function is completed and both flip-flops are reset. The second output would have a fast spike due to the small propagation delay of the AND and Reset functions.

8-45. LINEAR DEVICE THEORY

8-46. Operational Amplifiers

The source of gain in an operational amplifier can be characterized as an ideal, differential voltage amplifier having low ouput impedance, high input impedance, and very high differential gain. The output of an operational amplifier is proportional to the difference in the voltages applied to the two input terminals. In use, the amplifier output drives the input voltage difference close to zero through a feedback path.

When troubleshooting an operational amplifier circuit, measure the voltages at the two inputs; the difference between these voltages should be less than 10 mV. (Note: this troubleshooting procedure will not work for operational amplifiers which are configured as comparators.) A difference voltage much greater than 10 mV indicates trouble in the amplifier or its external circuitry. Usually, this difference will be several volts and one of the inputs will be very close to one of the supply voltages (e.g., +15V or −15V).

Next, check the amplifier's output voltage. It will probably also be close to one of the supply voltages (e.g., ground, +15V or −15V). Check to see that the output conforms to the inputs. For example, if the

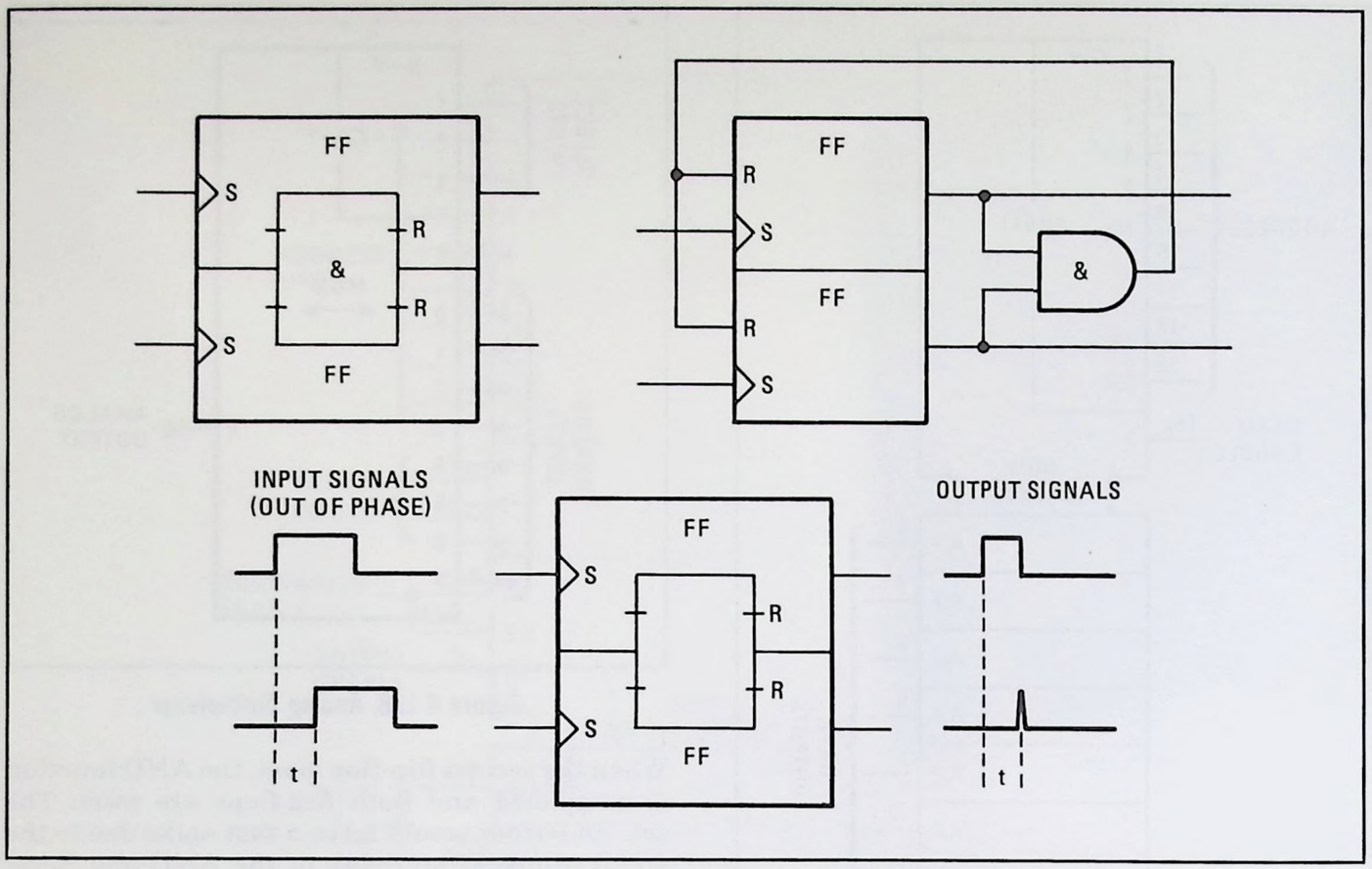


Figure 8-129. Phase-Frequency Detector

Operational Amplifiers (Cont'd)

inverting input is more positive than the non-inverting input, the output should be negative; if the non-inverting input is more positive than the inverting input, the output should be positive. If the output conforms to the inputs, check the amplifier's external circuitry. If the amplifier's output does not conform to its inputs, it is probably defective.

Figures 8-130, 131, and 132 show typical operational amplifier configurations. Figure 8-130 shows a non-inverting buffer amplifier with gain of 1. Figure 8-131 is a non-inverting amplifier with gain determined by R1 and R2. Figure 8-132 is an inverting amplifier with a gain determined by R1 and R2.

8-47. Comparators

Comparators are used as level sense amplifiers, switch drivers, pulse height discriminators, and voltage comparators. A voltage reference is connected to one of the amplifier's outputs as shown in Figures 8-133 and 134. When the input signal

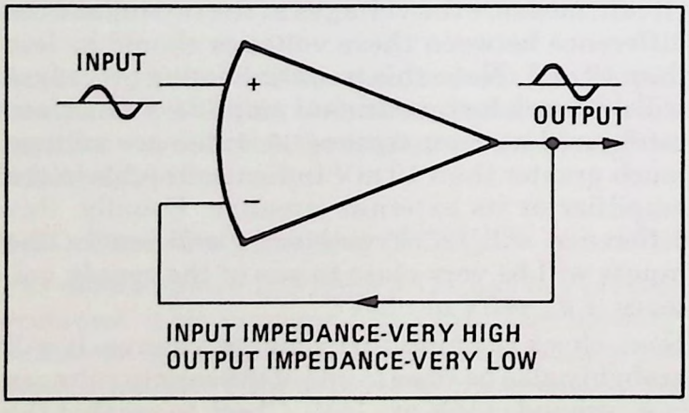


Figure 8-130. Non-Inverting Amplifier (Gain = 1)

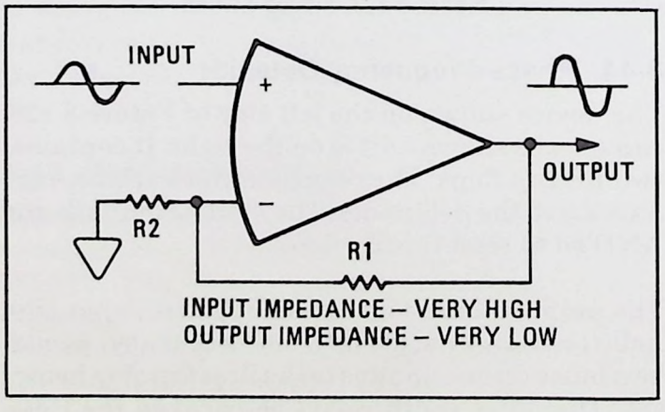


Figure 8-131. Non-Inverting Amplifier (Gain = 1 + R1/R2)

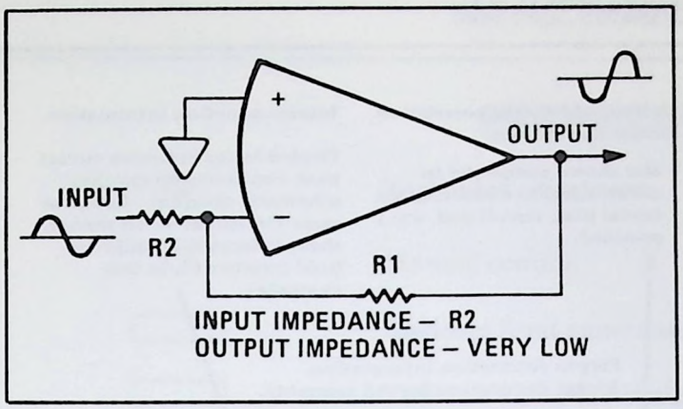


Figure 8-132. Inverting Amplifier (Gain = –R1/R2)

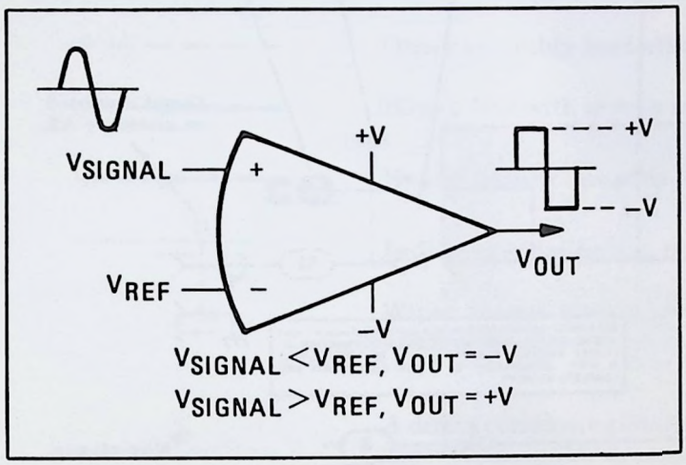


Figure 8-133. Non-Inverting Comparator

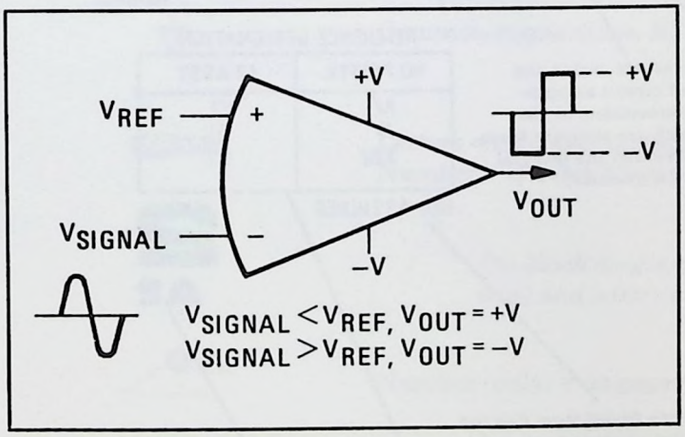


Figure 8-134. Inverting Comparator

Comparators (Cont'd)

voltage crosses the reference, the output goes positive; the output remains positive until the signal re-crosses the reference.

8-48. Limiter (Transistor Array)

The limiter shown in Figure 8-135 is simply a transistor array in a differential amplifier configuration. Its limiting characteristic is a function of its external biasing. The figure shows two of the common biasing arrangements and the internal circuitry of the device. The minus sign at pin 8 indicates signal inversion relative to the input. The plus sign at pin 5 (or the omission of the minus sign) indicates non-inversion.

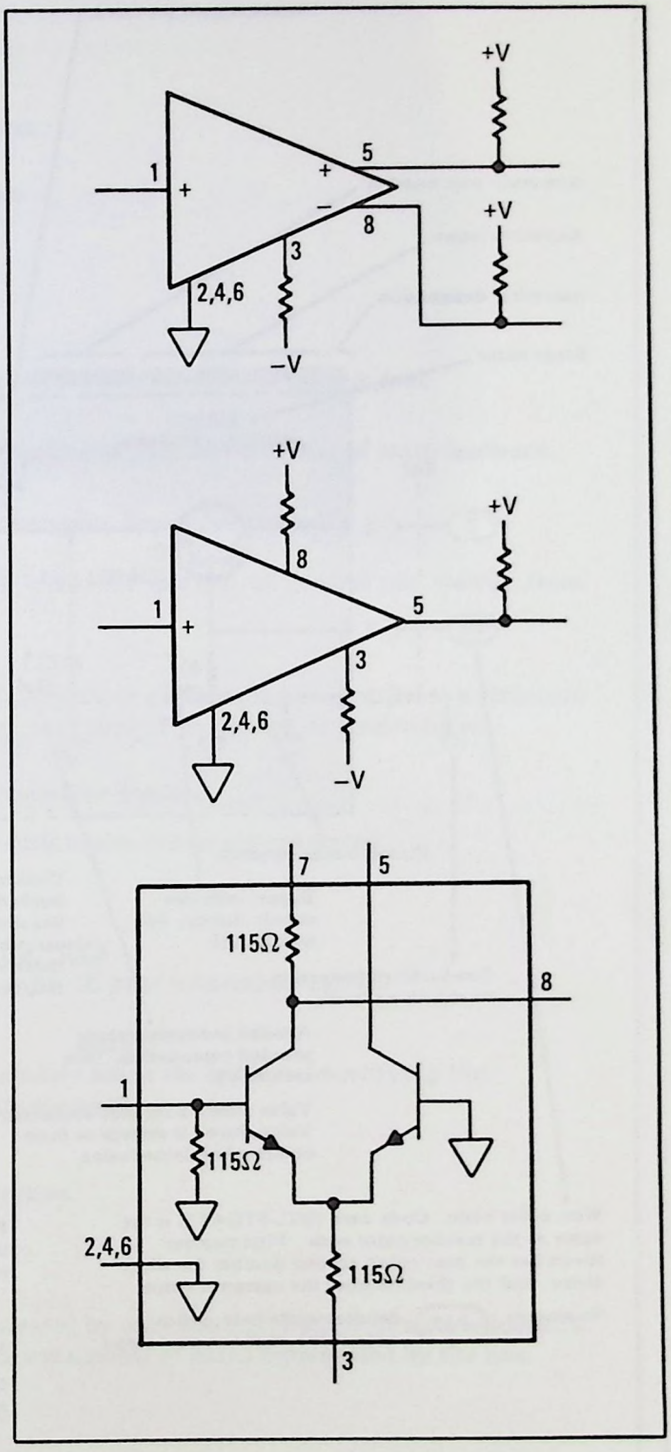


Figure 8-135. Limiter (Transistor Array)

8-49. SCHEMATIC DIAGRAM NOTES

Table 8-102 summarizes the symbology used in presenting many of the devices on the schematics.

Table 8-102. Schematic Diagram Notes (1 of 7)

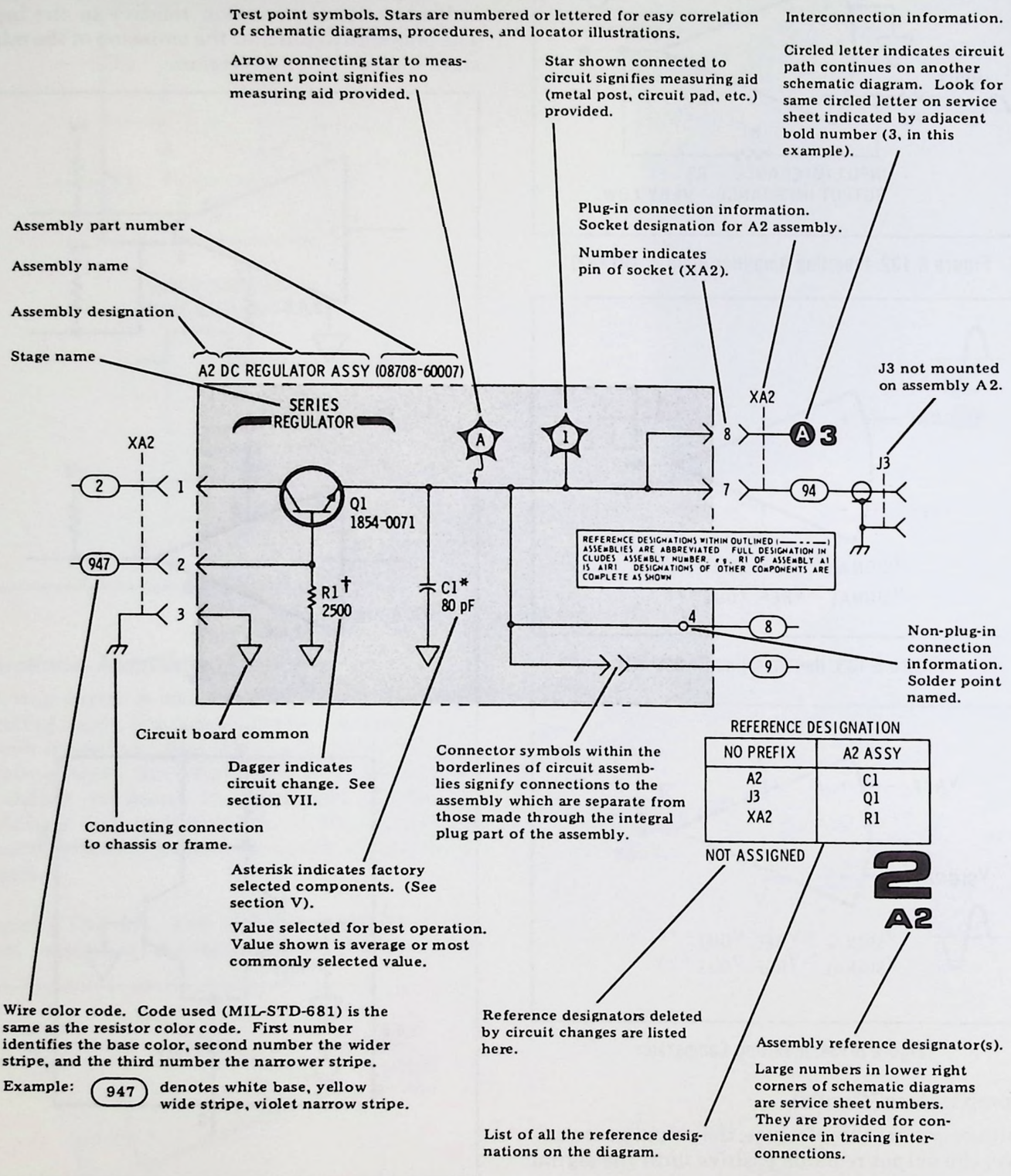


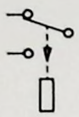
Table 8-102. Schematic Diagram Notes (2 of 7)

SCHEMATIC DIAGRAM NOTES

	Tool-aided adjustment.
	Manual control.
	Encloses front-panel designation.
	Encloses rear-panel designation.
	Circuit assembly borderline.
	Other assembly borderline.
	Heavy line with arrows indicates path and direction of main signal.
	Heavy dashed line with arrows indicates path and direction of main feedback.
	Indicates stripline (i.e., RF transmission line above ground).
CW	Wiper moves toward cw with clockwise rotation of control (as viewed from shaft or knob).
	A direct conducting connection to earth, or a conducting connection to a structure that has a similar function (e.g., the frame of an air, sea, or land vehicle).
	A conducting connection to a chassis or frame.
	Common connections. All like-designation points are connected.
AK 12	Letters = off-page connection, e.g., AK . Number = Service Sheet number for off-page connection, e.g., **12**.
	NOTE *On block diagrams, numbers are in the bubbles (identifying the line) and letters identify the page.*
1 THIS PAGE	Number (only) = on-page connection.
A B C A B 3 2 2	Indicates multiple paths represented by only one line. Letters or names identify individual paths. Numbers indicate number of paths represented by the line.
	Coaxial or shielded cable.

Table 8-102. Schematic Diagram Notes (3 of 7)

SCHEMATIC DIAGRAM NOTES



Relay. Contact moves in direction of arrow when energized.



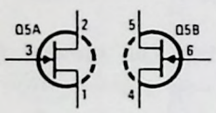
Indicates a PIN diode.



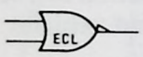
Indicates a Varactor diode.



Indicates a Schottky (hot-carrier) diode.



Multiple transistors in a single package—physical location of the pins is shown in package outline on schematic.



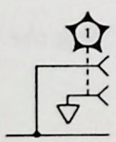
Identification of logic families as shown (in this case, ECL).



Numbered Test Point.
Measurement aid provided.



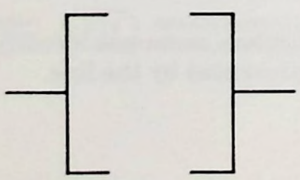
Lettered Test Point.
No measurement aid provided.



Numbered RF Test Point. Requires ac-coupling adapter from service kit.

DIGITAL SYMBOLOGY REFERENCE INFORMATION

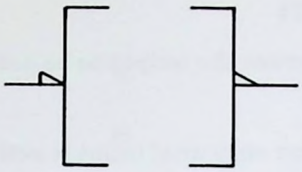
Input and Output Indicators



Implied Indicator—Absence of polarity indicator (see below) implies that the active state is a relative high voltage level. Absence of negation indicator (see below) implies that the active state is a relative high voltage level at the input or output.

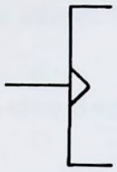
Table 8-102. Schematic Diagram Notes (4 of 7)

DIGITAL SYMBOLOGY REFERENCE INFORMATION

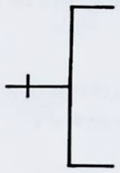


Input and Output Indicators (Cont'd)

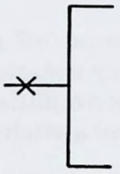
Polarity Indicator—The active state is a relatively low voltage level.



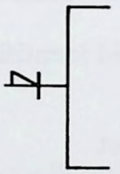
Dynamic Indicator—The active state is a transition from a relative low to a relative high voltage level.



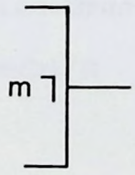
Inhibit Input—Input that, when active, inhibits (blocks) the active state outputs of a digital device.



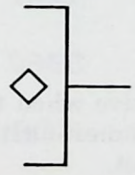
Analog Input—Input that is a continuous signal function (e.g., a sine wave).



Polarity Indicator used with Inhibit Indicator—Indicates that the relatively low level signal inhibits (blocks) the active state outputs of a digital device.



Output Delay—Binary output changes state only after the referenced input (m) returns to its inactive state (m should be replaced by appropriate dependency or function symbols).



Open Collector or Open Emitter output.

3-STATE

Three-state Output—Indicates outputs that can have a high impedance (disconnect) state in addition to the normal binary logic states.

Combinational Logic Symbols and Functions

&

AND—All inputs must be active for the output to be active.

≥1

OR—One or more inputs being active will cause the output to be active.

Table 8-102. Schematic Diagram Notes (5 of 7)

DIGITAL SYMBOLOGY REFERENCE INFORMATION

Combinational Logic Symbols and Functions (Cont')

≥m	Logic Threshold—m or more inputs being active will cause the output to be active (replace m with a number).
=1	EXCLUSIVE OR—Output will be active when one (and only one) input is active.
=m	m and only m—Output will be active when m (and only m) inputs are active (replace m with a number).
=	Logic Identity—Output will be active only when all or none of the inputs are active (i.e., when all inputs are identical, output will be active).
Σm	Arithmetic Summer—Performs arithmetic sum and difference, etc. per m and other internal notation.
	Amplifier—The output will be active only when the input is active (can be used with polarity or logic indicator at input or output to signify inversion).
X/Y	Signal Level Converter—Input level(s) are different than output level(s).
	Bilateral Switch—Binary controlled switch which acts as an on/off switch to analog or binary signals flowing in both directions. Dependency notation should be used to indicate affecting/affected inputs and outputs. Note: amplifier symbol (with dependency notation) should be read to indicate unilateral switching.
X→Y	Coder—Input code (X) is converted to output code (Y) per weighted values or a table.
(Functional Labels)	The following labels are to be used as necessary to ensure rapid identification of device function.
MUX	Multiplexer—The output is dependent only on the selected input.
DEMUX	Demultiplexer—Only the selected output is a function of the input.
CPU	Central Processing Unit
PIO	Peripheral Input/Output
SMI	Static Memory Interface

Sequential Logic Functions

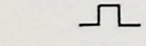
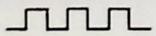
1 	Monostable—Single shot multivibrator. Output becomes active when the input becomes active. Output remains active (even if the input becomes inactive) for a period of time that is characteristic of the device and/or circuit.
G 	Oscillator—The output is a uniform repetitive signal which alternates between the high and low state values. If an input is shown, then the output will be active if and only if the input is in the active state.
FF	Flip-Flop—Binary element with two stable states, set and reset. When the flip-flop is set, its outputs will be in their active states. When the flip-flop is reset, its outputs will be in their inactive states.
T	Toggle Input—When active, causes the flip-flop to change states.

Table 8-102. Schematic Diagram Notes (6 of 7)

DIGITAL SYMBOLOGY REFERENCE INFORMATION

Sequential Logic Functions (Cont'd)

S	Set Input—When active, causes the flip-flop to set.
R	Reset Input—When active, causes the flip-flop to reset.
J	J Input—Analogous to set input.
K	K Input—Analogous to reset input.
D	Data Input—Always enabled by another input (generally a C input—see Dependency Notation). When the D input is dependency-enabled, a high level at D will set the flip-flop; a low level will reset the flip-flop. Note: strictly speaking, D inputs have no active or inactive states—they are just enabled or disabled.
+m	Count-Up Input—When active, increments the contents (count) of a counter by "m" counts (m is replaced with a number).
−m	Count-Down Input—When active, decrements the contents (count) of a counter by "m" counts (m is replaced with a number).
→m	Shift Right (Down) Input—When active, causes the contents of a shift register to shift to the right or down "m" places (m is replaced with a number).
←m	Shift Left (Up) Input—When active, causes the contents of a shift register to shift to the left or up "m" places (m is replaced with a number).

NOTE

For the four functions shown above, if m is one, it is omitted.

(Functional Labels)	The following functional labels are to be used as necessary in symbol build-ups to ensure rapid identification of device function.
mCNTR	Counter—Array of flip-flops connected to form a counter with modules m (m is replaced with a number that indicates the number of states: 5 CNTR, 10 CNTR, etc.).
REG	Register—Array of unconnected flip-flops that form a simple register or latch.
SREG	Shift Register—Array of flip-flops that form a register with internal connections that permit shifting the contents from flip-flop to flip-flop.
ROM	Read Only Memory—Addressable memory with read-out capability only.
RAM	Random Access Memory—Addressable memory with read-in and read-out capability.

Dependency Notation

mAm	Address Dependency—Binary affecting inputs of affected outputs. The m prefix is replaced with a number that differentiates between several address inputs, indicates dependency, or indicates demultiplexing and multiplexing of address inputs and outputs. The m suffix indicates the number of cells that can be addressed.

Table 8-102. Schematic Diagram Notes (7 of 7)

DIGITAL SYMBOLOGY REFERENCE INFORMATION

Dependency Notation (Cont'd)

Gm	Gate (AND) Dependency—Binary affecting input with an AND relationship to those inputs or outputs labeled with the same identifier. The m is replaced with a number or letter (the identifier).
Cm	Control Dependency—Binary affecting input used where more than a simple AND relationship exists between the C input and the affected inputs and outputs (used only with D-type flip-flops).
Vm	OR Dependency—Binary affecting input with an OR relationship to those inputs or outputs labeled with the same identifier. The m is replaced with a number or the letter (the identifier).
Fm	Free Dependency—Binary affecting input acting as a connect switch when active and a disconnect when inactive. Used to control the 3-state behavior of a 3-state device.

NOTE

The identifier (m) is omitted if it is one—that is, when there is only one dependency relationship of that kind in a particular device. When this is done, the dependency indicator itself (G, C, F, or V) is used to prefix or suffix the affected (dependent) input or output.

Miscellaneous

	Schmitt Trigger—Input characterized by hysterisis; one threshold for positive going signals and a second threshold for negative going signals.
Active	Active State—A binary physical or logical state that corresponds to the true state of an input, an output, or a function. The opposite of the inactive state.
Enable	Enabled Condition—A logical state that occurs when dependency conditions are satisfied. Although not explicitly stated in the definitions listed above, functions are assumed to be enabled when their behavior is described. A convenient way to think of it is as follows: A function becomes active when: • it is enabled (dependency conditions—if any—are satisfied) • and its external stimulus (e.g., voltage level) enters the active state.

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SERVICE MANUAL

8662A Synthesized Signal Generator

10 kHz — 1280 MHz



P/O Section VIII
Service Sheets

A-1

Block Diagrams

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HEWLETT PACKARD

SERVICE SHEET A

OVERALL BLOCK DIAGRAM

TROUBLESHOOTING HELP

Simplified Operation (Section III)
Operator's Checks (Functional, Memory, HP-IB — Section III)
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

The basic frequency generating circuitry is composed of the Reference Section, phase lock loops and Output Section (in the upper-left, center and right hand portions of the block diagram respectively). All of the reference frequencies used within the instrument are obtained from the Reference Section. A total of seven phase lock loops work together to produce the fundamental frequency band of 320 to 640 MHz with a step resolution of 0.1 Hz. This fundamental (or basic) band is sent to the Output Section where it is doubled, passed straight through or down-converted to produce the entire frequency range at the RF output (.01 to 1280 MHz).

The Digital Control Unit (DCU) controls the operation of the unit. It accepts keyboard or remote inputs and generates internal data and control signals to control the signal at the RF output. Power for the instrument is supplied by a switching-regulated power supply.

Reference Section

All of the reference frequencies used within the instrument are obtained from the Reference Section. This block is composed of doublers, dividers, and mixers, all of which are driven by a single temperature-stabilized 10 MHz crystal oscillator. Outputs from the Reference Section are 10, 20, 120, 520, and 320—640 MHz (in 20 MHz steps). Signal levels vary depending on which section they are being sent to.

Phase Lock Loops. The Generator uses the indirect synthesis method for generating output frequencies. Phase lock loop (PLL) circuits are locked to signals from the Reference Section and generate signals which are combined to give the desired output frequency. All output frequencies retain the same accuracy and stability as the 10 MHz reference signal. PLL's are found in the High Frequency, Low Frequency, Fractional-N, and Modulation Sections.

High Frequency Loops. The Reference Sum Loop and the Output Sum Loop are two nearly identical circuits. The Reference Sum Loop starts with 320—640 MHz and 10 or 20 MHz signals from the Reference Section. Together, these signals are related to digits D_9 and D_8 in the FREQUENCY readout (that is, in the basic band only). These signals are combined in the Output Sum Loop with the low frequency loops output that has a 0.1 Hz resolution.

Low Frequency Loops. The Low Frequency section consolidates several signals and produces an output signal having the characteristics of all of the inputs. This section has three phase lock loops: the N-Loop, the Low Frequency Sum Loop, and the FM Sum Loop.

The N-Loop generates a signal related to the D_7 and D_6 digits of the FREQUENCY readout (in the basic band). The other two loops combine this signal with outputs from the Fractional-N Loop and a 20 MHz reference signal from the Modulation or Reference Section. When the FM mode is selected, the 20 MHz signal is frequency modulated at the level needed to provide the desired amount of deviation at the front panel RF output.

Fractional-N-Loop. The Fractional-N Loop uses the 10 MHz reference signal to produce an output that is related to digits D_5,D_4,D_3,D_2,D_1, and D_0 of the FREQUENCY readout (in the basic band). The phase lock loop is called "Fractional-N" because the divider in the feedback circuit can divide by both integer and fractional values. This is accomplished by using digital dividers that by themselves only divide by integer values, but with extra control circuitry can switch the "divide-by" integer (N) between two values so that the average value of N contains a fractional part.

For example, to divide by 1300.455, the divider, would divide by 1301 for 455 cycles and by 1300 for 545 cycles. Over 1000 cycles, the effective division is by 1300.455. The Fractional-N Loop provides high resolution, faster switching, and lower noise.

Modulation Section and FM Loop. The Modulation Section produces 400 and 1000 Hz signals by dividing a signal from the Reference Section. Externally applied signals can be ac or dc coupled as shown on the block diagram.

The FM Loop produces one of the reference signals for the FM Sum Loop. The signal is 20 MHz with

SERVICE SHEET A (Cont'd)

FM. The phase lock loop is unlocked when a dc-coupled signal from the front panel's MODLATION INPUT is selected. Thus, the 140 MHz Oscillator operates in a free run condition without any correction.

Output Section

The output section converts the basic band (320 to 640 MHz) from the High Frequency Section to all other frequencies by multiplying it, passing it through, or dividing it. This section also controls the RF level of the signal. It does this with a group of electromechanical attenuators. These attenuators reduce the amplitude in 5 dB increments from 5 dB through 140 dB. Electronic leveling keeps the output level constant and provides finer output step resolution.

The Reverse Power Protection circuit, if triggered, opens a relay in series with the output. The trigger level is set to 10 volts peak RF. Limiting diodes provide initial protection until the relay opens. AM is applied to the output signal at each of the three separate Automatic Gain Control (AGC) modulators.

Digital Control Unit

The Digital Control Unit (DCU) is a microprocessor based controller that is responsible for directing the operation of the instrument. It takes information from the keyboard, HP-IB interface or AUX connector. It stores the data, calculates the required oscillator frequencies, determines internal switch settings, and provides basic control over the instrument. Although not shown on this block diagram, the DCU is a transfer point for digital data to all the sections.

Power Supply

This instrument uses a switching-regulated power supply that provides high efficiency and low heat dissipation.

TROUBLESHOOTING

Introduction

Troubleshooting is structured into three levels:

1. Instrument (to identify a defective section)
2. Section (to identify a defective assembly)
3. Assembly (to identify a defective component)

The general procedure is to begin at the instrument level to isolate the problem to a section (Block Diagram A), then to an assembly within the section (Block Diagrams B-I), and finally to a component on the assembly (detailed schematics). There is troubleshooting information on the block diagrams which can be used by someone who understands the theory of operation to isolate the problem to the next lower level. There is a troubleshooting procedure with each block diagram. These procedures are the recommended troubleshooting approach for someone who is inexperienced with servicing the Generator. To effectively use these procedures you need a basic understanding of the principles of operation. Read the theory before using the procedure so the procedure becomes a guide. Many short cuts are possible as more experience is gained.

WARNING

When working on the power supply, remember that high voltage is present at all times when the line cord is plugged in (that is, plus and minus 160 Vdc and line voltage). Unplug the line cord before doing anything to the power supply. The line switch has no effect on the high voltage.

When working near the rear panel, be careful to keep long hair from being drawn into the fan. This could cause personal injury.

CAUTION

DO NOT plug in or unplug any board assembly with the instrument line switch turned on. Always turn the line switch to STANDBY when removing or inserting a board. There are some components that could be damaged by transients generated this way.

The "LINE" fuse should not be replaced until the cause of its failure is determined. Replacing this fuse in a damaged Generator might cause additional damage. A qualified service person should first determine the cause of its failure, specifically with resistance checks in the power supply (see Service Sheet 55); repair the failure and then replace the fuse.

When measuring frequency, connect a cable from the Generator's 10 MHz Reference output (rear panel) to the counter's reference input and set the

SERVICE SHEET A (Cont'd)

counter Reference switch to EXT. All time bases will be a little different so this will ensure that all correct frequency readings will be off only by the resolution error of the counter.

When measuring frequency or power level at an output connector, disconnect any cable that is normally connected so the measuring instrument is the only load on the output. If the cable must remain connected to make a valid measurement, this will be specifically stated.

All power level values given are as measured on a spectrum analyzer. Measurements made with a power meter might give a slightly higher reading. ECL signals will read approximately 2 dB higher with a power meter because the harmonics are high and add to the power meter reading.

Instrument Level Troubleshooting

The following procedure can be used to isolate an instrument malfunction to one of the sections.

1. Check power supply voltages. Remove the top cover of the instrument. The power supply is in the left-rear corner. Test points to check each of the voltages are accessible through openings in the power supply top cover. Silkscreening on the cover identifies the test points. Measure each of the voltages and compare to the tolerance in Table 8-201.

Table 8-201. Power Supply Voltages

Supply Voltage	Tolerance
+5.2V	±.02V
+20V	±0.1V
−10V	±.04V
−40V	±0.2V

If a voltage is out of tolerance, adjust it. The voltage should be adjustable above and below the nominal value within the tolerance limits. If a voltage cannot be adjusted to within limits, there is a problem with the power supply, so continue troubleshooting on Service Sheet I.

If the Generator fails to turn on, check the power supply voltages first. If they are incorrect, continue on Service Sheet I. If the power supply voltages are correct, continue on Service Sheet B (the Digital Control Unit).

2. STATUS light flashes. All sections contain self-check circuitry which can detect some malfunctions. When a malfunction is detected, the STATUS light flashes. Press the STATUS key and hold it down and the status code will be displayed on the frequency display (on the right). If 99 is displayed, press the Blue Key and then the STATUS key. The actual status code will be displayed. Table 8-203 defines the status codes and where to continue troubleshooting if one occurs. Many codes do not indicate an "error" so no further troubleshooting is necessary. The codes in Table 8-203 that are followed by an asterisk (*) indicate errors which could be caused by an external means (operator setting, external reference, etc.). Check this possibility before troubleshooting the Generator. Table 8-204 is a list of special function codes that would be displayed on the left when the STATUS key is pressed.

There are many errors which cannot be detected by the self-check circuitry and it's also possible for the self-check circuitry to malfunction. Therefore, use the status code only as a guide. Confirm that the problem indicated by the status code really exists.

NOTE

Under certain conditions, it is possible for Status code 10, "Amplitude out of specification", to turn on when no amplitude error exists. This can happen during fast repetitive sweeps (for example, Auto Sweep or Remote Stepped Sweep, with the time/step less than 1 ms). Corrective action is not required unless code 10 persists in conditions other than the fast repetitive sweep.

If no status code is present, continue with Step 3.

3. All malfunctions can be divided into six general classifications.

a) Front Panel, HP-IB and AUX malfunctions. This includes all improper operation of keys, display and indicators. Begin troubleshooting with Service Sheet B.

b) RF output frequency not correct. Begin troubleshooting with Step 4.

c) RF output power level not correct. Begin troubleshooting with Step 5.

d) Modulation problems. Begin troubleshooting with Service Sheet F.

SERVICE SHEET A (Cont'd)

e) High spurs or phase noise. Begin troubleshooting with Step 6, below.

f) Problems associated with front and rear panel connectors (except RF output). Table 8-202, shows where to start troubleshooting when the signal from an output connector is not normal or the signal applied to an input connector does not produce the desired effect.

Table 8-202. Failures Associated with External Connectors

Connector	Troubleshoot Assembly (Service Sheet)
SWEEP OUTPUT	A2A2 (16)
MODULATION INPUT	A4A9 (40)
AUX (Inputs)	A2A2 (3)
AUX (Outputs)	A2A2 (17)
PEN LIFT	A2A2 (17)
Z AXIS BLANKING/MARKER	A2A2 (16)
AM MARKER	A2A2 (16)
MODULATION OUTPUT	A4A9 (40)
AUX FM INPUT	A4A6 (39)
(10 MHz Reference) OUTPUT	A8A4 (18)
(5 or 10 MHz Reference) INPUT	A8A4 (18)

4. RF Output Frequency Not Correct.

a) Measure the RF output frequency with a counter. Run a cable from the Generator's 10 MHz reference output to the counter external time base input and move the counter time base switch to external.

b) If the frequency is not stable (that is, it varies more than ±1 count), there is a phase lock loop unlocked. Measure the output of each section containing phase lock loops shown on the block diagram until the bad section is found. Start at the bottom of the block diagram and move up. Then continue troubleshooting on the service sheet for the bad section.

c) If the frequency is stable, measure the High Frequency Loops Section output frequency. If this frequency is normal, the problem is in the Output Section. Otherwise, measure the output of each section starting at the bottom of the block diagram until the bad section is found. Then continue troubleshooting on the service sheet for the bad section.

5. RF Power Level Not Correct. Measure the power level of the output signal from the High Frequency Loops Section. If this power level is not within the limits given on the block diagram, there is a problem in the High Frequency Loops Section so continue troubleshooting on Service Sheet D. If this power level is normal, the problem is in the Output Section, so continue troubleshooting on Service Sheet E.

6. High Spurs or Phase Noise. This is the most difficult type of problem to troubleshoot. Some troubleshooting experience and a thorough understanding of the theory of operation of the instrument are needed to be successful. The general procedure to follow is:

a) Locate the section of the instrument in which the problem is originating.

b) Search for the cause. In the case of high phase noise it is now a matter of trying different things to narrow the cause. This is where experience helps. If the problem is spurs, identify the source of the spur. The location of the spur and how it moves in relation to the center frequency can provide a lot of information when the theory of operation of the Generator is well understood. Removing cables or substituting signals from an external source are also useful techniques.

c) Once the source of the spur is known look for the coupling mechanism. This often requires a lot of trial and error work.

Table 8-203. Status Code Descriptions (1 of 2)

Status Code	Description	Continue Troubleshooting on Service Sheet
00	No error	—
01*	No signal level or no reference oscillator. Check INT-EXT switches on rear panel	18
02	Fractional-N Loop unlocked	G
03	N-Loop unlocked (Low Frequency Section)	H
04	Sum Loop unlocked (Low Frequency Section)	H
05	FM Sum Loop unlocked (Low Frequency Section)	H
06	Reference Sum Loop unlocked (High Frequency Section)	D
07	Output Sum Loop unlocked (High Frequency Section)	D
08	FM Loop unlocked	F
09*	Reverse power protection triggered. If reverse power was applied, press AMPLITUDE key to reset the Generator's output. If no reverse power was applied, continue troubleshooting.	36
10*	Amplitude error in Output Section (see also Troubleshooting step 2).	E
11*	Over modulation (FM). Compare deviation and rate to specifications. Reduce input level,or if within specification, continue troubleshooting.	F
12	Reference oscillator not heat stabilized. This condition should not exist for more than 1 hour after the line cord is plugged in.	18
13	External reference selected.	18
14*	Frequency of reference signal out of tolerance.	19
15*	AM overmodulation in AM +FM mode. Reduce input level.	40
	NOTE *Errors 16-31 are triggered by self-check circuitry in the Digital Control Unit (DCU). The frequency, level and modulation data sent to the other sections is also read back from the DCU's output. Thus when an error occurs, it could be that the data is bad or that the read-back circuitry is bad.*	
16	DF0 or DF1	
17	DF2 or DF3	
18	DF4 or DF5	
19	DF6	
	Fault in frequency output data	B
20	Binary	
21	Frequency range data	
22	DF9	
	Fault in frequency output data	B
23—25	Not used	
26	MA0 to MA7	
27	MA8 to MA10	
28	MS0 to MS7	
	Fault in modulation output data	B
29	Step attenuator data	
30	LV1—0 through LV2—3	
31	LV2—4 through LV2—11	
	Fault in level output data	B
32	Frequency selection out of range (1 kHz to 1.28 GHz).	—
33	Amplitude selection > +16 dBm. Entry ignored.	—
34	Amplitude selection <—139.9 dBm. Entry ignored.	—

*These errors could have an external cause. Check before troubleshooting the Generator.

Table 8-203. Status Code Descriptions (2 of 2)

Status Code	Description	Continue Troubleshooting on Service Sheet
35	Amplitude >+10 dBm or 710 mV. AM not specified.	—
36	Amplitude selection >999 mV or <0 µV. Entry ignored.	—
37	AM selection >95% or <0%. Entry ignored.	—
38	Frequency >150 kHz. AM invalid.	—
39	FM <200 kHz or >0.0 kHz invalid.	—
40	FM >100 kHz invalid for frequencies between 320 and 640 MHz, or 1 kHz and 120 MHz.	—
41	FM >50 kHz invalid for frequencies between 160 and 320 MHz.	—
42	FM >25 kHz invalid for frequencies between 120 and 160 MHz.	—
43	Wrong entry protocol. Entry ignored.	—
44	Too many significant digits prior to decimal point.	—
45	Start and stop frequencies equal.	—
46	Parameter underflow. Defaulted to zero.	—
47	Marker out of limits (start-stop).	—
48	Marker out of limits (span)	—
49	Sweep step size is greater than start/stop frequency difference	—
50	Store/Recall error. Register failed or non-existent.	—
51	Recall 0 invalid (1—9 only).	—
52	RAM data altered; first good register recalled; special functions cleared. Re-enter data for Store-Recall registers.	—
53	RAM faulty. Generator initialized to 100 MHz and –30 dBm. Re-enter data for all registers.	—
54	No amplitude correction above +13 dBm.	—
55	Sweep steps >10,000. Staircase ramp disabled (SWEEP OUTPUT = 0V).	—
56	Special Function code invalid.	—
57	Amplitude reference volts invalid.	—
58	Key invalid in mixed modulation mode.	—
59	Sweep span out of limits.	—
95 96 97 98	} Memory error (ROM or RAM).	B
99	General code for internal hardware malfunction. Press blue key and status key to get one of the above codes which is the actual cause of the malfunction.	

Table 8-204. Special Function Status Codes

Code	Description
11	+Freq Offset
12	–Freq Offset
31	Amplitude reference
41	FM INT +AM EXT AC
42	FM INT +AM EXT DC
51	AUX FM (rear panel input)
61	Parameter shift keying increment (two-key format)
62	Parameter shift keying increment (one-key format)
85	Amplitude Correction Off
88	Automatic Sequence
89	Factory testing only

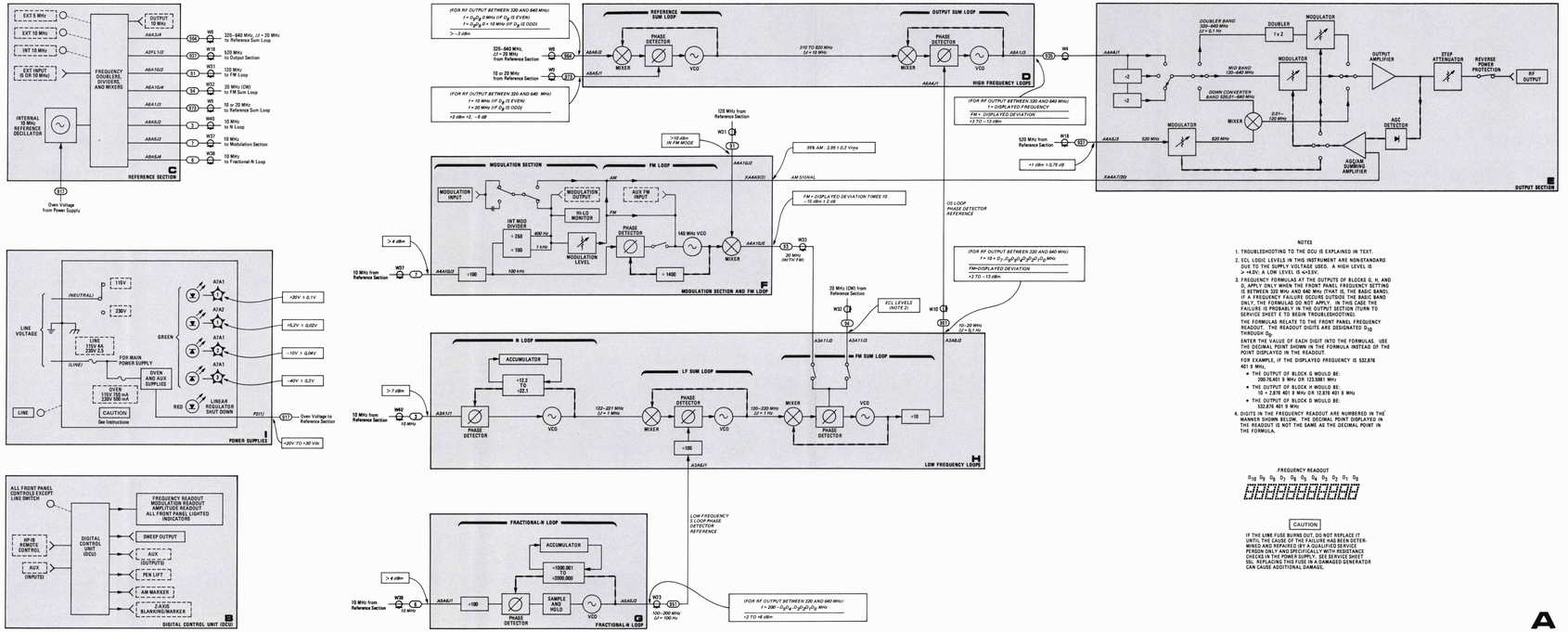


Figure 8-201. Overall Block Diagram

SERVICE SHEET B

DIGITAL CONTROL UNIT (DCU) BLOCK DIAGRAM

TROUBLESHOOTING HELP

Block Diagram A
HP-IB Address Selection (Section II)
HP-IB Connector (Section II)
Memory and HP-IB I/O Checks (Section III)
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post Repair Adjustment Procedures

PRINCIPLES OF OPERATION

The main function of the Digital Control Unit (DCU) is to control the operation of the Signal Generator in response to data and instructions received from the front panel keyboard, AUX connector or Hewlett-Packard Interface Bus (HP-IB).
The Microprocessor/Decoder Board maintains control of the system by implementing a master program stored permanently in read-only memory (ROM). Temporary storage of keyboard and display information and numerous intermediate data calculations is located in random-access memory (RAM). The RAM is provided with battery backup to keep stored data intact during power-down conditions. ROM and RAM are addressed by the Microprocessor/Decoder Board, as is the Control ROM on the HP-IB Board.

The HP-IB Board functions as the instrument interface to the IEEE Standard 488 interface bus (HP-IB) which enables the instrument to be operated by an automated controller. The ROM on this board contains all of the software routines for interfacing the Signal Generator to HP-IB.

The DCU uses a bi-directional data bus for transferring information between the Microprocessor Board and peripheral boards. The HP-IB Board's bi-directional bus arrangement allows data to be sent between the Signal Generator and the automated controller. All but three DCU boards read and write information from the data bus. The Readout and Sweep boards only read information off the data bus; the ROM Board only writes onto the bus. The Level/Modulation and Frequency Output boards have monitor circuits which return data to the processor. The processor can then verify that control information sent to the signal generating portion of the circuit is correct. The Keycode Board provides an interface between the Keyboards, status circuits, and the microprocessor.

Signals on the DCU control bus coordinate data-transmission timing within the DCU. The control bus consists of enable/disable, read/write, interrupt request, reset, and clock signal lines. Only two boards can interrupt the microprocessor by way of the control bus. They are the HP-IB and Keycode boards. In the process of transmitting and receiving data, these boards use a "handshake" routine that ensures information is acknowledged, read, and verified in proper sequence.

Overall Block Diagram SERVICE SHEET A

SERVICE SHEET B (Cont'd)

TROUBLESHOOTING

If a problem has been traced to the DCU, the troubleshooting procedures in this section will narrow down the problem to an assembly. There are four separate procedures. Use the Procedure that matches the failure symptoms:

1. Instrument dead or failure doesn't fit into one of the other categories. This is a general troubleshooting procedure which should find most problems. Use the procedure 1 below.

2. Front panel STATUS light flashed and error code indicates DCU failure. Use procedure 2 below.

3. HP-IB programming problems. Use the troubleshooting procedure with Service Sheet 5.

4. Keyboard related problems and problems related to the malfunction signals coming from the rest of the instrument. Use the troubleshooting procedure with Service Sheet 3.

Procedure

1. General Troubleshooting Procedure.

a. Remove all the boards from the DCU except the A2A6 processor board.

b. Turn the Generator so it is resting on its right side and remove the bottom cover.

c. Follow the instructions on Service Sheet B2 to connect the signature analyzer and put the Generator in free run mode.

d. Take signatures on the bottom of the DCU mother board at the XA2A6 connectors. If the +5V signature (at XA2A6A pin 1 or 19) is not correct there is a problem with the set-up or the processor is bad. Start troubleshooting the A2A6 (Service Sheets 6 and 7) if this signature cannot be obtained.

e. If any signatures on the XA2A6 connectors are not normal, troubleshoot the A2A6 assembly to find the cause of the problem. Measure the signatures on the top connector of A2A6 shown in Table 8-212 on Service Sheet B2 (free run mode).

†f. Plug in the memory boards (that is A2A7 and A2A9) and A2A2, and perform the memory tests (RAM and ROM). Follow the instructions on Service Sheet B3. Troubleshoot any errors that are found.

g. Plug-in the data output boards (A2A3 and A2A4) and follow the instructions on Service Sheet B2 to use the signature analysis stimulus mode. Take signatures on the bottom of the DCU mother board on connectors XA2A3 and XA2A4 as shown on the service sheet. Most of A2A2 is checked during the RAM memory test when the keyboard LEDs come on and off.

h. This checks all DCU boards except the A2A1 keycode board and the A2A5 HP-IB board. The A2A5 HP-IB board should have no effect on operation of the instrument from the front panel and if it does, there is most likely a problem with the A2A5 assembly. Troubleshooting the HP-IB assembly is covered by the procedures with Service Sheet 5.

i. The Keycode board is the interface between the keyboards and the microprocessor. If there are problems relating to the keys or AUX connector troubleshoot the A2A1 board starting on Service Sheet 3.

2. DCU Error Code Displayed.

a. Memory must be checked first. Execute the ROM and RAM tests by using special functions 83 (ROM) and 84 (RAM). These tests are described in Section III. If either of these tests fail, perform diagnostics described on Service Sheet B3.

NOTE

The special function 84 RAM diagnostic does not perform a comprehensive RAM check. If there is any reason to suspect that there may be RAM problems, perform the RAM memory diagnostic described on Service Sheet B3.

b. When the error code indicates a data output error (error codes 16 through 31), use signature analysis to verify the failure. Follow the instructions on Service Sheet B2 (data output boards signature analysis stimulus) to set-up the signature analysis mode. Table 8-205 identifies the signal lines that originate each of the status codes. Take signatures at the DCU mother board connectors for the data lines where the error was detected.

c. If the signatures indicate a failure, then extend the board and troublehsoot to find the cause. If the signatures at the data output lines are normal, there is likely a problem in the monitor circuitry. To troubleshoot the monitor circuitry, extend the board where the readback error was detected and use signature analysis to find the bad component.

Table 8-205. Error Code

Error Code	Signal Line	Assembly (Service Sheet)
16	DF0, DF1	A2A4 (12)
17	DF2, DF3	A2A4 (12)
18	DF4, DF5	A2A4 (13)
19	DF6	A2A4 (13)
20	DB7, DB8	A2A4 (13)
21	R0, R6	A2A4 (12)
22	DF9	A2A4 (13)
26	MA0, MA7	A2A3 (15)
27	MA8, MA10	A2A3 (15)
28	MS0, MS7	A2A3 (15)
29	step attenuator data	A2A3 (14)
30	LV1-0 — LV2-3	A2A3 (14)
31	LV2-4 — LV2-11	A2A3 (14)

Diagnostic Programs

The DCU has several internal diagnostic programs. These programs are stored in a ROM and need only the A2A6 board in the DCU to run. Table 8-206 summarizes these programs. Operating instructions are contained in the foldout service sheet listed in Table 8-206.

Table 8-206. Diagnostic Program Summary

Diagnostic	Service Sheet	A2A6 Switch Setting
HP-IB Talk-Only	B1	2
Mainframe Stimulus	B1	A
Signature Analysis Stimulus:		
Sweep Board	B2	3
Mod/Level Frequency Output Boards	B2	4
Free Run Mode	B2	N/A
Memory and Indicators		
ROM, Continuous Run	B3	6
ROM, Stop on Error	B3	7
RAM and Indicators		
Single Run	B3	8
Continuous Run	B3	9

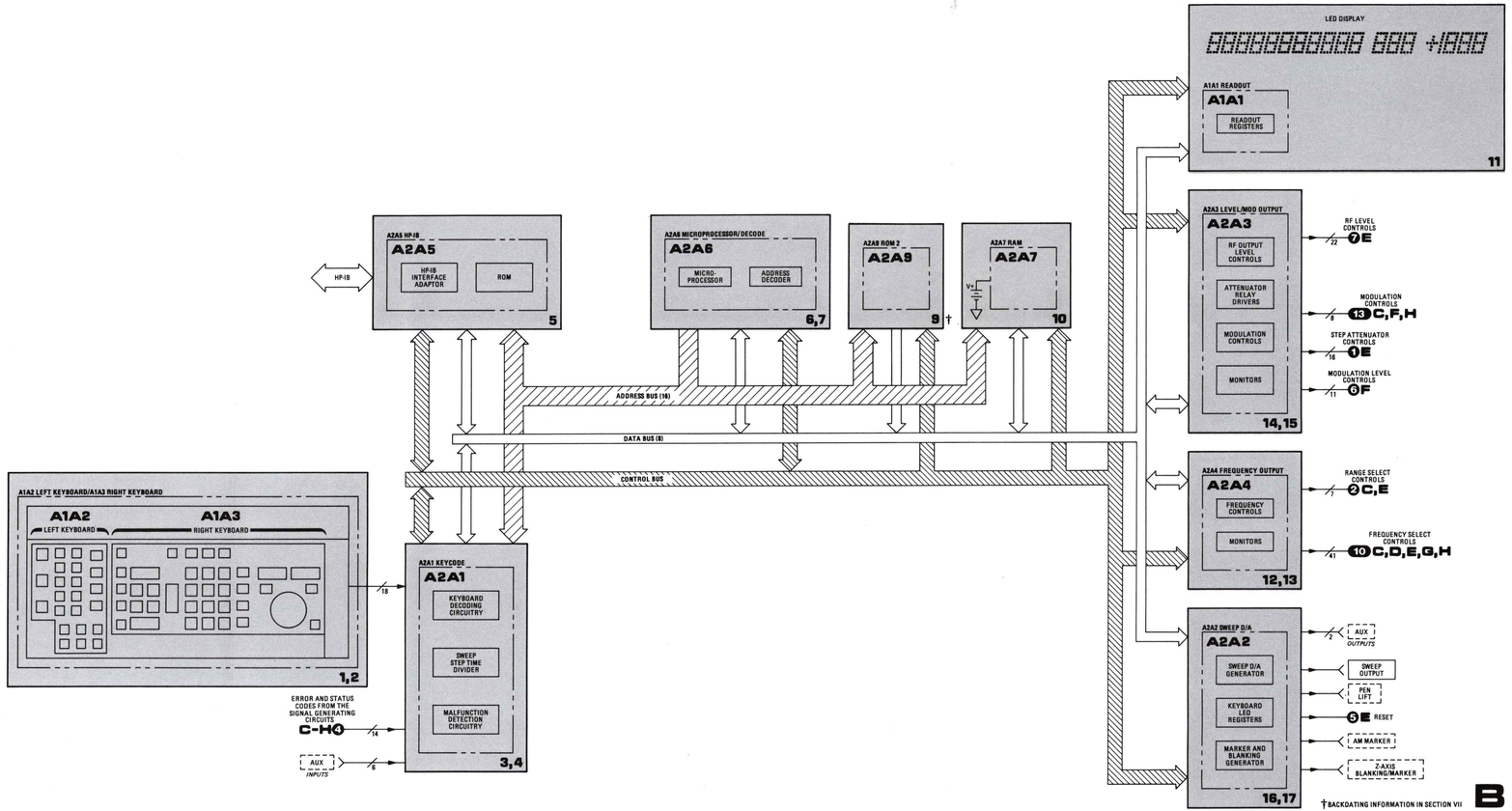


Figure 8-202. Digital Control Unit (DCU) Block Diagram

HP-IB TALK-ONLY DIAGNOSTIC

DESCRIPTION

This diagnostic does the following:

1. Reads the HP-IB address switch on top of the A2A5 assembly and displays the switch setting in the front panel frequency display.
2. Puts the Generator into a talk only mode and transmits on the bus. All 8 bit values from 0 to 255 are sent continuously. This data can be read and analyzed by a controller.
3. Stimulates the A2A5 assembly so signature analysis can be used to troubleshoot parts of the HP-IB circuitry (see Service Sheet 5).

SET UP

1. Set the rotary switch on the A2A6 Microprocessor Assembly to position 2.
2. Insert a shorting pc edge connector on the top connector of the A2A6 assembly.
3. Connect a jumper from TP6 (ground) to TP4 (R) on A2A6.
4. Momentarily short TP3 (RES) to ground or turn the line switch to ON.

OPERATING INSTRUCTIONS

1. Remove the jumper from TP4(R). The contents of the front panel frequency display should be the HP-IB address switch setting. Change the address switch to all of its positions and check that each setting appears in the frequency display as it is changed.
2. Figure 8-203 is a sample program for the HP 9825A, HP 9835, or HP 9845 computing controllers to read the data the Generator is sending on the HP-IB and check that it is correct. Connect the HP-IB cable to the Generator and run the program. If operation is normal, the controller display will contain "PASSED". This should occur within 5 seconds after the RUN key is pressed. If the program is running for more than about 5 seconds, it is likely that the program is not reading data but is waiting because the Generator is not "handshaking" properly. In this case the program will stay hung-up and the problem is most likely the PIA(U7) or HP-IB transceivers (U6 or U9) on A2A5. Check the "handshaking" lines to find the cause.
3. If the data is read but is not correct, an error printout will occur. A sample error printout is shown in Figure 8-204. The 8 bit data bytes received are on the left and their decimal equivalent on the right. The data goes from 0 to 255 and repeats. The calculator starts reading anywhere in the cycle and reads 256 values. After reading all the values, the data is analyzed and data values near where the error was detected are printed. Analyzing the printout can often detect a bit stuck high or low. The printout in Figure 8-204 shows the DIO7 line stuck in the one state.

DESCRIPTION	SAMPLE PROGRAMS	
	HP 9825A	HP 9835A/B or HP 9845A
Reserve space in memory for arrays A and A$. Sets format of all data as having no digits after decimal point.	0: dim A[300],A$[8];fxd 0	10 OPTION BASE 1 20 DIM A(300),A$[8] 30 FIXED 0
Reads 300 values from the HP-IB into array A.	1: for I=1 to 300 2: rdb(700)→A[I] 3: next I	40 FOR I=1 TO 300 50 A(I)=READBIN(700) 60 NEXT I
Check that each reading increases by 1. When the reading is 0, the sequence starts over.	4: for J=1 to 256 5: if A[J+1]=0;gto +2 6: if A[J]+1≠A[J+1];gto "error" 7: next J	70 FOR J=1 TO 256 80 IF A(J+1)=0 THEN 100 90 IF A(J)+1<>A(J+1) THEN Error 100 NEXT J
Print or display "Passed" or "Error."	8: prt "PASSED";stp 9: "error": 10: prt "ERROR"	110 DISP "PASSED" 120 STOP 130 Error: PRINT "ERROR"
If an error was detected, start printing 5 readings before the error occured.	11: J-5→K 12: if K<1;1→K	140 K=J-5 150 IF K<1 THEN K=1
Print 20 readings.	13: for L=K to K+20	160 FOR L=K TO K+20
Convert the numeric value of the reading to binary and store in string array A$.	14: A[L]→V 15: for M=1 to 8 16: 2^(8-M)→B 17: "0"→A$[M,M] 18: if V>=B;"1"→A$[M,M];V-B→V 19: next M	170 V=A(L) 180 FOR M=1 TO 8 190 B=2^(8-M) 200 A$[M,M]="0" 210 IF V<B THEN 240 220 A$[M,M]="1" 230 V=V-B 240 NEXT M
Print the reading in binary (Array A$) and decimal form.	20: prt A$,A[L] 21: next L	250 PRINT A$,A(L) 260 NEXT L
	22: stp	270 END

Figure 8-203. HP 9825A, HP 9835A/B and HP 9845A Sample Program Listing

ERROR		ERROR	
BINARY	DECIMAL	BINARY	DECIMAL
11111010	250	(Cont'd)	(Cont'd)
11111011	251	01000101	69
11111100	252	01000110	70
11111101	253	01000111	71
11111110	254	01001000	72
11111111	255	01001001	73
01000000	64	01001010	74
01000001	65	01001011	75
01000010	66	01001100	75
01000011	67	01001101	77
01000100	68	01001110	78

Figure 8-204. Sample Error Printout

MAINFRAME STIMULUS DIAGNOSTIC

DESCRIPTION

This diagnostic stimulates the frequency data (DB7-1 to DF9-2) going to the High Frequency Loops Section and the level data (LV2-0 to LV2-9) going to the Output Section. Both data values start at all zeros and are increased by ones to all ones. A delayed signature analysis clock is generated because the frequency data lines going to the High Frequency Loops Section are heavily filtered and have long rise and fall times. The delayed clock assures stable signatures. The functions of this diagnostic are:

1. Allows signature analysis verification of the high frequency data.
2. Allows signature analysis verification of the ROMs on the A6A9 assembly.
3. Allows checking of the D/A converter (DAC) on the A4A7 assembly (Service Sheet 37). The output of the DAC is a voltage ramp from zero to full scale.

SET-UP

1. Set the rotary switch on the A2A6 assembly to position A.
2. Insert a shorting pc edge connector on the top connector of the A2A6 assembly.
3. Connect a jumper from TP6 (ground) to TP4 (R) on A2A6.
4. Momentarily short TP3 (RES) to ground or turn the front panel switch to ON.
5. † If the signature analysis portion of this diagnostic is to be used, connect the signature analyzer to the A2A6 assembly as follows:

Analyzer	A2A6
START	ST(TP2)
STOP	ST(TP2)
CLOCK	TP7
GND	GND(TP6)

6. Set the analyzer pushbutton switches as follows:

START	⌿(OUT)
STOP	⍀(IN
CLOCK	⍀(IN)
HOLD	OFF (OUT)
SELF TEST	OFF (OUT)
+5V signature should be 2H98.	

OPERATING INSTRUCTIONS

1. A4A7 Reference Circuitry Check. Mount the A4A7 board on an extender. View the signal at A4A7TP3 on an oscilloscope. The waveform should be as shown in Figure 8-205.
2. A6A9 High Frequency Loops Controller ROM check. Mount the A6A9 board on an extender. Correct signatures are given in table 8-207.
3. A2A4 Frequency Output Assembly High Frequency Digit check. Signatures can be taken with the A2A4 assembly on an extender board or on the bottom of the DCU motherboard. Correct signatures are given in Table 8-208.

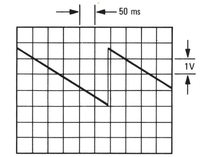


Figure 8-205. Waveform at A4A7TP3

Table 8-207. A6A9 ROM Signatures

OUTPUT SIGNATURES				INPUT SIGNATURES	
PIN	A6A9 U1	A6A9 U2	A6A9 U3	U1, U2, U3 PIN	
6	H353	70C1	48A4	1	F910
7	9HH6	F22A	P3HC	2	4FPP
8	P998	8AHA	4C3A	3	P64F
9	295A	CP86	5537	4	F77A
11	85H7	58U1*	UC64	5	OA37
12	7991	H932*	H504	16	OC29
13	14FO	82A7*	7703	17	0654
14	U3CF	A420	F101	18	9340
				19	UA70

*To obtain these signatures lift one lead of VR1, VR2 and VR3.

Table 8-208. A2A4 Output Signatures

MNEMONIC	XA2A4B PIN	SIGNATURE
DB7-1	19	F910
DB7-2	20	4FPP
DB7-4	21	P64F
DB7-8	22	F77A
DB8-1	23	OA37
DB8-2	24	OC29
DB8-4	25	0654
DB9-1	26	9340
DB9-2	27	UA70

SIGNATURE ANALYSIS STIMULUS DIAGNOSTIC

DESCRIPTION

This diagnostic stimulates much of the circuitry within the DCU for testing purposes. Lists of normal signatures are contained with the troubleshooting information for each assembly where this technique is used. Switch setting 3 stimulates the A2A2 sweep board. Switch setting 4 stimulates the data output boards.

SET-UP

1. Connect a jumper from GND (TP6) to R (TP4) on A2A6.

2. Connect a shorting connector on the top edge connector of A2A6. Turn the rotary switch on A2A6 to position 3 or 4 (as indicated by the notes in the signature tables).

3. Connect the signature analyzer to the A2A6 assembly as follows:

Analyzer	A2A6
START	ST (TP2)
STOP	ST (TP2)
CLOCK	SA CK (TP1)
GND	GND(TP6)

4. Set the analyzer pushbutton switches as follows:

START	⌜ (OUT)
STOP	⌞ (IN)
CLOCK	(See Table Notes)
HOLD	OFF (OUT)
SELF TEST	OFF (OUT)

5. Momentarily ground RES (TP3) on A2A6. This should cause the signature analysis stimulus diagnostic to run. Touch the signature analysis probe to +5V. The signature should be PP02 for switch position 4; or 6F90 for position 3.

6. All output lines are loaded by the cables attached to them. Sometimes, this loading can affect the signatures. So, if an incorrect signature is obtained, remove the associated connector on the DCU motherboard and recheck the signature (the associated connector is shown in the Table notes).

† Table 8-209. A2A2 Sweep Board Signatures (see Notes)

MNEMONIC	SIGNATURE				MNEMONIC	SIGNATURE
GND	0000	18	36		0000	GND
PRW	391U	17	35			
D3-7	867F	16	34			
D3-4	7U1P	15	33			
SWEEPEND	1P56	14	32			
D3-6	3HH4	13	31			
D3-0	9CU5	12	30	XA2A2B		
D3-1	7U17	11	29			
D3-3	A615	10	28			
D3-2	0984	9	27			
D4-5	8UH6	8	26		95CF	D4-4
D4-7	3C97	7	25		0145	D4-6
D4-2	58UH	6	24		7756	D4-3
D4-0	U11U	5	23		5U82	D4-1
D5-5	C60F	4	22		8359	D5-4
D5-7	H628	3	21		F293	D5-6
D5-2	8H33	2	20		044P	D5-3
D5-0	707F	1	19		1H08	D5-1
		18	36			
		17	35			
DAL	6F90	16	34		H9A6	D6-4
D6-3	HP80	15	33		P20D	D6-2
D6-0	43UU	14	32		H2H2	D6-1
SME		13	31			
D7-4	CUC9	12	30		833A	
D7-3	0569	11	29	XA2A2A	89HH	D7-2
D7-0	A307	10	28		PAF1	D7-1
STATUS	06A4	9	27			
		8	26			
DAH	6F90	7	25		----	A0
		6	24		----	A1
	H02U	5	23		----	A2
		4	22		----	SC0
	P044	3	21		391U	CLOCK
A2	PFUA	2	20		798A	SB4
+5V	6F90	1	19		6F90	+5V

Notes.
1. On the analyzer, CLOCK = ⌞ (IN).
2. On A2A6, use switch position 3.

Table 8-210. A2A3 Mod/Level Output Board Signatures (see Notes)

MNEMONIC	SIGNATURE				MNEMONIC	SIGNATURE
GND	0000	18	36		0000	GND
MA9	6CPH	17	35		5AF2	MA10
MA7	F504	16	34		7455	MA8
MA5	5730	15	33		FA71	MA6
MA3	HF61	14	32		26U4	MA4
MA1	2P6U	13	31		2H4A	MA2
MS6	1H9P	12	30	XA2A3B	U154	MA0
MS4	PF76	11	29		291A	MS5
MS2	2030	10	28		5447	MS3
MS0	7A2F	9	27		45UH	MS1
LV2-10	29PA	8	26		0428	LV2-11
LV2-8	7HP8	7	25		C4A0	LV2-9
LV2-6	3A07	6	24		84CP	LV2-7
LV2-4	A0F7	5	23		A886	LV2-5
LV2-2	U14H	4	22		7400	LV2-3
LV2-0	71U8	3	21		P676	LV2-1
LV1-4	4642	2	20		9HU6	LV1-8
LV1-1	4C3F	1	19		60U7	LV1-2
MS7	HFH1	18	36			
MON	FF38	17	35			
		16	34			
		15	33			
		14	32			
		13	31			
		12	30	XA2A3A		
		11	29			
		10	28			
		9	27			
		8	26			
		7	25			
MAH	PP02	6	24			
LTE	PP02	5	23			
MAL	PP02	4	22		PP02	LEH
		3	21		PP02	LEL
MSE	PP02	2	20		PP02	LME
+5V	PP02	1	19		PP02	+5V

Notes:
1. On the analyzer, CLOCK = ⌞ (IN).
2. On A2A6, use switch position 4.
3. Associated connector: A2A10J8.

Table 8-211. A2A4 Frequency Output Board Signatures (see Notes)

MNEMONIC	SIGNATURE				MNEMONIC	SIGNATURE
GND	0000	18	36		0000	GND
BREE-L	PP02	17	35		FC34 [4]	DF5-1
		16	34		CC0C [4]	DF5-2
		15	33		2643 [4]	DF5-4
		14	32		6080 [4]	DF5-8
		13	31		87A9 [5]	DF6-1
		12	30	XA2B	FFUU [5]	DF6-2
		11	29		1789 [5]	DF6-4
		10	28		UUAH [5]	DF6-8
		9	27		[3]	DB9-2
DF4-8	9A90 [4]	8	26		[3]	DB9-1
DF4-4	14P9 [4]	7	25		[3]	DB8-4
DF4-2	C96C [4]	6	24		[3]	DB8-2
DF4-1	05UC [4]	5	23		[3]	DB8-1
DF2-8	1UH8 [4]	4	22		[3]	DB7-8
DF2-4	9PFA [4]	3	21		[3]	DB7-4
DF2-2	26FC [4]	2	20		[3]	DB7-2
DF2-1	10A0 [4]	1	19		[3]	DF7-1
		18	36		UPH3 [4]	DF3-1
MON	PP02	17	35		86H5 [4]	DF3-2
		16	34		4F74 [4]	DF3-4
		15	33		26P5 [4]	DF3-8
		14	32		00FA [4]	DF1-1
		13	31		P66C [4]	DF1-2
		12	30	XA2A	FC5F [4]	DF1-4
		11	29		0H78 [4]	DF1-8
		10	28		015P [7]	R4
DF7-8	H00C [5]	9	27		AH8C [7]	R5
DF7-4	5H6U [5]	8	26		505C [7]	R6
DF7-2	FHU5 [5]	7	25		F5F7 [6]	DF8-1
FLE	PP02	6	24		1162 [7]	R3
DF0-1	F127 [4]	5	23		A180 [7]	R2
DF0-2	UFA4 [4]	4	22		CC0H [7]	R1
DF0-4	7HU4 [4]	3	21		898A [7]	R0
DF0-8	F898 [4]	2	20		PP02	FTE
+5V	PP02	1	19		PP02	+5V

Notes:
1. On the analyzer, CLOCK = ⌜ (OUT)
2. On A2A6, use switch position 4.
3. For pins B19-27, use the "Mainframe Stimulus Diagnostic" on Service Sheet B1.
4. Associated connector: A2A10J4.
5. Associated connector: A2A10J5.
6. Associated connector: A2A10J6.
7. Associated connector: A2A10J8.

FREE RUN MODE

SET-UP

1. Connect a jumper from GND (TP6) to R (TP4) on A2A6. There must be no shorting connector on the top pc edge connector of A2A6.

2. Connect the signature analyzer to the A2A6 assembly as follows:

Analyzer	A2A6
START	ST (TP2)
STOP	ST (TP2)
CLOCK	SA CK (TP1)
GND	GND(TP6)

3. Set the analyzer pushbutton switches as follows:

START	⌜ (OUT)
STOP	⌞ (IN)
CLOCK	⌞ (IN)
HOLD	OFF (OUT)
SELF TEST	OFF (OUT)

4. Touch the probe to +5V. The signature should be 0001.

† Table 8-212. A2A6 Microprocessor Board Signatures (Top Connector)

Pin	Signature
11	F2AP
12	5CP8
13	CU33
14	FU78
15	9788
16	HPPF
17	3984
18	41F3

Table 8-213. A2A6 Microprocessor Board Signatures (Bottom Connectors)

MNEMONIC	SIGNATURE				MNEMONIC	SIGNATURE
GND	0000	18	36		0000	GND
A0	5555	17	35			
A1	CCCC	16	34			
A2	7F7F	15	33			
A3	5H21	14	32			
A4	0AFA	13	31			
A5	UPFH	12	30	XA2A6B		
A6	52F8	11	29			
A7	HC89	10	28			
A8	2H70	9	27			
A9	HPP0	8	26		0001	PRW
A10	1293	7	25			
A11	HAP7	6	24		2828	SA2
A12	3C96	5	23			
A13	3827	4	22			
A14	755U	3	21			
A15		2	20			
		1	19			
		18	36			
		17	35			
		16	34			
SA1C	A68C	15	33			
		14	32			
SA18	A277	13	31			
MON	1020	12	30	XA2A6A		
LTE	4084	11	29		956C	SB4
FTE	0215	10	28		F488	SC0
DAL	0851	9	27		5P18	SA3
SME	2141	8	26		H479	BREE
MAL	8501	7	25		C9C8	FLE
MSE	1400	6	24		2205	STB
LEL	5004	5	23		8103	LEH
LME	4014	4	22		2041	MAH
MOD32	0054	3	21		8811	DAH
MOD10	0157	2	20			
+5V	0001	1	19		0001	+5V

MEMORY AND INDICATORS DIAGNOSTICS

DESCRIPTION

ROM Diagnostic

The ROM diagnostic checks all the ROMs in the DCU. Every ROM is manufactured so that the checksum of the contents of the ROM is zero. The diagnostic program reads the contents of each ROM and calculates the checksum. If a checksum is not zero, an error code is displayed in the front panel frequency display. If no errors are found, "00" is displayed at the end of the test. The testing program is the same for both switch settings. The difference is that when switch setting 6 is used, the program will display an error code when an error is found and then continue testing so that if several errors existed, all would be displayed one after another. In switch position 7, when an error is found, the program will halt and display the error code. This is particularly useful if the failure is intermittent.

RAM and Indicators Diagnostic

The RAM diagnostic checks 4 different types of failures. The test takes one minute to run and a counter is displayed in the left digits of the frequency display while the test is running. The counter is a visual indication that the test is running but the counter doesn't contain any failure information. This test also lights the front panel indicators so their operation can be checked. The testing program is the same for both switch settings and both stop when an error is detected. The difference is that when switch setting 9 is used, the program does not stop after it has run once and found no errors but continues to rerun the program until an error is found. Using switch setting 8 will cause the program to stop at the end with an indication that no errors were found.

SET-UP

1. Insert a shorting pc edge connector on the top connector of the A2A6 assembly.
2. Connect a jumper from GND (TP6) to R (TP4) on A2A6.
3. Set the rotary on the A2A6 Microprocessor Assembly to select the diagnostic test program as indicated in Table 8-214.

Table 8-214. Memory and Indicator Diagnostic Test Selections

Switch Setting	Program
6	ROM diagnostic, continuous run, displays all errors.
7	ROM diagnostic, halt on and display first error.
8	RAM and Indicators diagnostic, stop on first error or stop at end of program
9	RAM and Indicators, run continuously until first error found.

4. Momentarily short RES (TP3) to ground on A2A6 or cycle the LINE switch.
5. Follow the operating instructions for the diagnostic being run.

OPERATING INSTRUCTIONS

ROM Test

1. Remove the jumper between R (TP4) and ground on A2A6.
2. If no ROM errors are found, "00" will be displayed in the right side of the front FREQUENCY display. The display will retain this value for about a second and then go blank while the test is repeated. At the end of the test "00" is displayed again to indicate no errors were found.
3. If a two-digit code other than "00" is displayed, a ROM error has been found. Refer to Table 8-215 to translate the error code to the actual hardware failure.

† **Table 8-215. ROM Test Error Codes**

Error Code	Memory Address	Hardware Failure	
		Assembly (Service Sheet)	Device
01	1800	A2A5(5)	U11
02	2000	A2A9(9)	U9
03	2800		U3
04	3000		U4
05	3800		U10
06	4000		U8
07	4800		U2
08	5000		U1
09	5800		U7
10	6000		U5
11	6800		U11
12	7000		U6
13	7800		U12

RAM and Indicator Test

1. The front panel FREQUENCY display should contain "–1".
2. Remove the jumper between R (TP4) and ground on A2A6. The following should happen:

   a. All the LED indicators on the keyboard and the REMOTE and ADDRESSED lights on the display should light.

   b. A four-digit number (counter) with interspaced decimal points should appear in the left side of the frequency display. This counter is incremented to show the test is running.

3. When the counter value reaches 2047, the following happens:

   a. The counter momentarily stops at 2047.

   b. The annunciators on the display turn on sequentially until all are lighted.

   c. All the LEDs that were on during the first part of the test turn off.

   d. The counter continues incrementing but the decimal points are turned off.

4. The test takes approximately one minute to run. If no errors are found, "00" will be displayed in the right side of the front panel FREQUENCY display and the diagnostic program will halt in this condition (switch position 8) or display "00" for a few seconds and then repeat the test (switch position 9). If an error is found, the diagnostic program will halt with an error code in the display.
5. Error Codes. When an error is found, there are three types of codes which could be displayed:

   a. Error code is "-1". This code is displayed at the start of the test before the jumper is removed from R (TP4). If the display does not change when the jumper is removed, an error has been found in the first memory locations checked. The active memory IC's associated with this failure are A2A7U7 and U8.

   b. Error code is "1-XX" or "2-XX". XX is a two-digit code which represents the memory IC where the error was found. Table 8-216 maps the two-digit code to a component reference designator. The "2-XX codes can only narrow the failure down to two possible components.

Table 8-216. RAM Test Error codes

Error Code 1-	Device Reference Designator (A2A7)	Error Code 2-	Device Reference Designator (A2A7)
01	U8	01	U7 or U8
02	U7	02	U6 or U5
03	U6	03	U4 or U3
04	U5	04	U2 or U1
05	U4	05	U16 or U15
06	U3	06	U14 or U13
07	U2	07	U12 or U11
08	U1	08	U10 or U9
09	U16		
10	U15		
11	U14		
12	U13		
13	U12		
14	U11		
15	U10		
16	U9		

TROUBLESHOOTING

1. When a memory error is found, the error code points to a specific memory device; however, the actual failure could be the address decode or data bus buffer associated with the memory device. Especially if multiple errors occur, check these components first. Signature analysis (Free Run Mode, Service Sheet B2) makes it easy to check the decoders. Normal signatures are contained on the Service Sheets 3 through 17.
2. The tests that run continuously and stop on first failure (switch settings 7 and 9) are useful for finding intermittent problems. The diagnostic can be left running unattended and if the failure occurs, the diagnsotic program will halt with the error code in the front panel display. This code greatly narrows down the location of the intermittent fault.

Memory and Indicators Diagnostic
SERVICE SHEET B3

SERVICE SHEET C
REFERENCE SECTION BLOCK DIAGRAM

TROUBLESHOOTING HELP

Block Diagram A
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post Repair Adjustment Procedures

PRINCIPLES OF OPERATION

The Reference Section provides the following output signals:

FM Loop 10 MHz Reference Signal
Frac N 10 MHz Reference Signal
N Loop ϕ Detector Reference (10 Mz)
RS Loop ϕ Detector Reference (10 or 20 MHz)
FMS Loop ϕ Detector Reference (20 MHz CW)
Down Converter Band Mixer RF (520 MHz)
RS Loop Mixer RF (320-640 MHz, $\Delta f = 20$ MHz)
FM Loop Mixer LO (120 MHz)

These signals are distributed to other sections of the instrument. All of the Reference Section outputs are derived from either a 10 MHz internal source (temperature controlled quartz oscillator) or an external frequency standard of 5 MHz or 10 MHz. The accuracy and stability of all signals generated in the Generator are traceable to the outputs from the Reference Section. The various output signals are generated by employing several frequency translation techniques (multiplying, dividing and heterodyning).

TROUBLESHOOTING

There are five signals generated in the Reference Section (besides three 10 MHz signals) and sent to other sections of the instrument:

1) 320-640 MHz in 20 MHz steps (A6A3J4)
2) 520 MHz reference signal (A6A3J1)
3) 120 MHz reference signal (A6A10J2)
4) 10/20 MHz signal (A6A1J3)
5) 20 MHz reference signal when the instrument is in FM mode (A6A10J4)

When the frequency or level of one of these signals is not the value shown on the block diagram, the problem is in the Reference Section. Table 8-217 shows at what frequencies the variable frequency signals are for output frequencies in the basic band (that is, 320 to 640 MHz). Troubleshoot the Reference Section by backtracing until the bad assembly is found. Then continue troubleshooting with the service sheet for the defective assembly.

Table 8-217. Reference Section Variable Frequency Signals

Output Frequency (MHz)		Reference Section Variable Signals (MHz)		
≥	<	A6A3J4 (320-640)	A6A1J3 (10/20)	A6A2J2[1] (60-140)
320.0	330.0	320.0	10.0	DC
330.0	340.0	340.0	20.0	140.0
340.0	350.0	340.0	10.0	140.0
350.0	360.0	360.0	20.0	120.0
360.0	370.0	360.0	10.0	120.0
370.0	380.0	380.0	20.0	60.0
380.0	390.0	380.0	10.0	60.0
390.0	400.0	400.0	20.0	80.0
400.0	410.0	400.0	10.0	80.0
410.0	420.0	420.0	20.0	60.0
420.0	430.0	420.0	10.0	60.0
430.0	440.0	440.0	20.0	120.0
440.0	450.0	440.0	10.0	120.0
450.0	460.0	460.0	20.0	140.0
460.0	470.0	460.0	10.0	140.0
470.0	480.0	480.0	20.0	DC
480.0	490.0	480.0	10.0	DC
490.0	500.0	500.0	20.0	140.0
500.0	510.0	500.0	10.0	140.0
510.0	520.0	520.0	20.0	120.0
520.0	530.0	520.0	10.0	120.0
530.0	540.0	540.0	20.0	60.0
540.0	550.0	540.0	10.0	60.0
550.0	560.0	560.0	20.0	80.0
560.0	570.0	560.0	10.0	80.0
570.0	580.0	580.0	20.0	60.0
580.0	590.0	580.0	10.0	60.0
590.0	600.0	600.0	20.0	120.0
600.0	610.0	600.0	10.0	120.0
610.0	620.0	620.0	20.0	140.0
620.0	630.0	620.0	10.0	140.0
630.0	640.0	640.0	20.0	DC

[1]The variable signal at A6A2J2 is used only within the Reference Section.

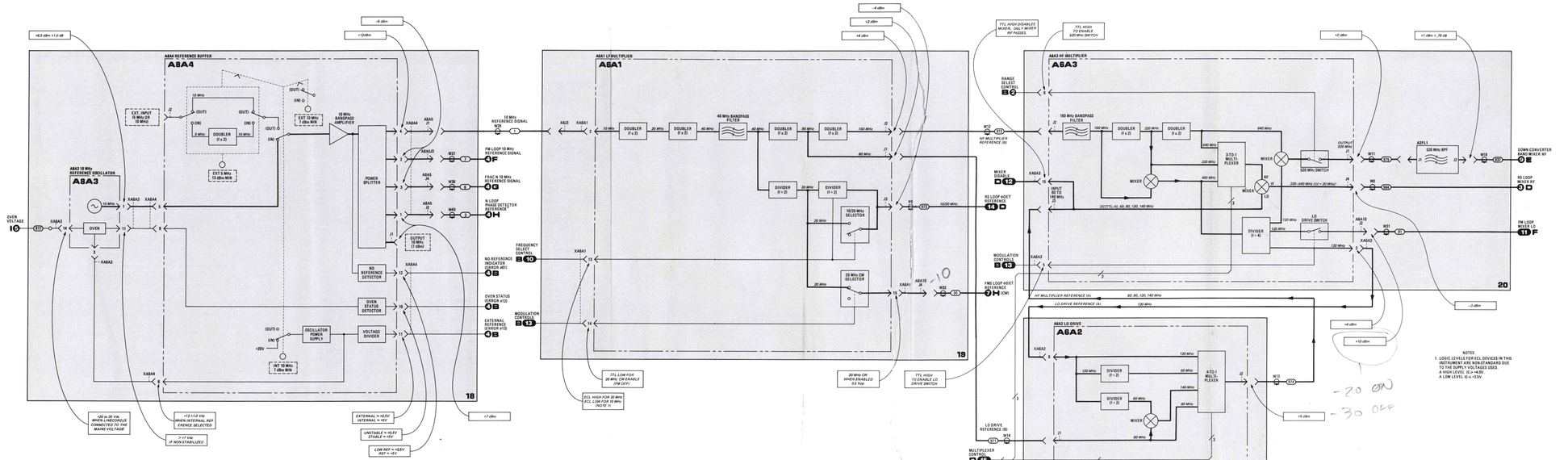


Figure 8-206. Reference Section Block Diagram

SERVICE SHEET D
HIGH FREQUENCY LOOPS BLOCK DIAGRAM

TROUBLESHOOTING HELP

Block Diagram A
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post Repair Adjustment Procedures

PRINCIPLES OF OPERATION

The High Frequency Section generates the basic (fundamental) band which is sent to the Output Section (Block Diagram E). This section employs two phase lock loops to generate the basic band. The 320 to 640 MHz and 10/20 MHz signals from the Reference Section are first mixed in the Reference Sum Loop to produce a 310 to 620 MHz, 10 MHz step resolution signal. This signal is then mixed in the Output Sum Loop with the 10 to 20 MHz, 0.1 Hz step resolution, signal from the Low Frequency Section to produce the 320 MHz to 640 MHz, 0.1 Hz step resolution, basic band signal at the A8A1J3 output. Figure 8-207 is a block diagram of the basic high frequency loop. The only difference between the Reference Sum (RS) Loop and the Output Sum (OS) Loop is that, in the case of the RS loop, the VCO output frequency is always less than the high frequency reference input at the mixer, whereas the opposite is true for the OS Loop. Coarse tuning and speedup is regulated by the Controller Board (Service Sheet 22) in the High Frequency Loops Section.

The frequency error circuits (Service Sheets 25 and 29) contain the frequency comparator and VCO correction circuitry. Under normal operating conditions, when the VCOs are locked, these lock acquisition circuits remain inactive. When the loop is un-locked, a beat note exists which is the difference between the loop IF down converted frequency and the reference frequency. If this beat note is within 200 kHz of the loop bandwidth (which is between 250 kHz and 500 kHz) the loop will acquire lock by itself. If the beat note is greater than the loop bandwidth by more than 200 kHz, the lock acquisition circuitry will be activated, coarsely tuning the VCO to within 200 kHz of the desired frequency. At this point, the phase lock loop will take over and complete the lock cycle.

SERVICE SHEET D (Cont'd)

TROUBLESHOOTING

When a problem has been traced to the High Frequency Loop Section, this procedure can be used to isolate the problem to an assembly. The Reference Sum (RS) Loop must be locked before the Output Sum (OS) Loop will lock, therefore, work on the RS Loop first if both are unlocked.

Procedure:

1. Set the front panel frequency to a value in the basic band (320.0 to 640.0 MHz). If the problem doesn't occur in this band, the fault is most likely in the Output Section (Service Sheet E) rather than the HF Loop Section.

2. Measure the input signals to the loop being tested. These input signals are described in Table 8-218. If any of the input signals are not normal, look for the problem at the source of the input signal.

3. Pull out the A6A4 (OS Loop) or A6A5 (RS Loop) assembly and move the slide switch to the TEST position. This opens the loop so the VCO can be checked. Use Table 8-219 or Table 8-220, depending on the loop being checked, and check the VCO output for the front panel frequency settings given in the table. If the VCO functions normally, continue troubleshooting with step 4. If the VCO output is not normal, check the two input signals to the VCO.

   a) The tuning voltage should be the value given in the table. If the voltage is not normal, there is most likely a problem in the pretuning circuitry on A6A4 or A6A5 (whichever drives the VCO where the problem exists).

   b) The inductor switch signals. The table states which inductor should be turned on. Service Sheet 22 shows the pin numbers where the switch signals can be measured and what the normal levels are. If the switch signals are not normal, the problem is most likely on A6A9.

If the input signals are normal and the VCO output is bad, then the VCO is defective. The VCO's are not field-repairable. Exchange assemblies are available.

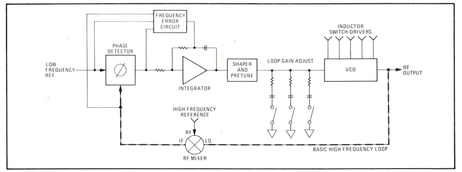


Figure 8-207. Basic High Frequency Loop Block Diagram

Reference Section
Block Diagram
SERVICE SHEET C

4. If the VCO output is normal, check the output of the RF Mixer Assembly (A6A6 or A6A8). The frequency of the output signal should be in the range of 10—20 MHz ± the error of the VCO signal which is running open loop. If the output is not normal, check the input signals first to locate the source of the problem.

5. If the output of the RF Mixer Assembly is normal, the problem is most likely to be with the Phase Detector Assembly (A6A4 or A6A5). Use the troubleshooting procedure in Service Sheet 24 or 28 to isolate the problem.

Table 8-218. HF Loops Input Signals

Loop	Signal	Where to Measure	Frequency	Level
Reference Sum	HF Reference	W8(964) to A6A6J2	Table 8-221	-3 dBm
	10/20 Reference	W9(973) to A6A5J1	Table 8-221	-4 dBm
Output Sum	FM Sum Loop Output	W10(961) to A6A4J1	10—20 MHz	-3 dBm
	RS Loop Output	W2(965) to A6A7J1	Table 8-221	+3 to -13 dBm

Table 8-219. Output Sum Loop VCO Pretuning Check (A8A1)

Front Panel Frequency Setting (MHz)	VCO Frequency * (±3 MHz)	Bit On	Tuning Voltage (±1.0 Vdc) A6A4J2	Inductor On
524.0	527.5	None	-36.10	E
523.0	526.0	P1	-33.40	E
521.0	524.5	P2	-30.70	E
517.0	520.5	P4	-26.20	E
511.0	514.5	P8	-19.70	E
452.0	456.0	All	-13.00	D & C
330.0	334.0	None	-36.10	A
344.0	347.0	None	-36.10	B
370.0	375.0	None	-36.10	C
421.0	426.0	None	-36.10	D
524.0	527.5	None	-36.10	E

*Measure at W4(935) at A4A4J1 or W5(967) at A6A8J1.

Table 8-220. Reference Sum Loop VCO Pretuning Check (A8A2)

Front Panel Frequency Setting (MHz)	VCO Frequency* (±3 MHz)	Bit On	Tuning Voltage (±1.0 Vdc) A6A5J2	Inductor On
340.0	336.5	None	-36.10	A
350.0	346.5	P4	-26.60	B
380.0	376.0	None	-36.10	C
430.0	425.5	P1	-33.40	D
520.0	516.0	P8	-19.70	E
530.0	525.5	P2	-30.70	E

*Measure at W1(963) at A6A8J1 and W2(965) at A6A7J1

Table 8-221. Reference Sum Loop Variable Frequency Signals

Front Panel Frequency Setting (MHz)	Reference Sum Loop Output (MHz) W2(965) to A6A7J1	10/20 MHz Reference W9(973) to A6A5J1	HF Reference (MHz) W8(964) to A6A6J2
32X.X	310.0	10.0	320.0
33X.X 34X.X	320.0 330.0	20.0 10.0	340.0
35X.X 36X.X	340.0 350.0	20.0 10.0	360.0
37X.X 38X.X	360.0 370.0	20.0 10.0	380.0
39X.X 40X.X	380.0 390.0	20.0 10.0	400.0
41X.X 42X.X	400.0 410.0	20.0 10.0	420.0
43X.X 44X.X	420.0 430.0	20.0 10.0	440.0
45X.X 46X.X	440.0 450.0	20.0 10.0	460.0
47X.X 48X.X	460.0 470.0	20.0 10.0	480.0
49X.X 50X.X	480.0 490.0	20.0 10.0	500.0
51X.X 52X.X	500.0 510.0	20.0 10.0	520.0
53X.X 54X.X	520.0 530.0	20.0 10.0	540.0
55X.X 56X.X	540.0 550.0	20.0 10.0	560.0
57X.X 58X.X	560.0 570.0	20.0 10.0	580.0
59X.X 60X.X	580.0 590.0	20.0 10.0	600.0
61X.X 62X.X	600.0 610.0	20.0 10.0	620.0
63X.X	620.0	20.0	640.0

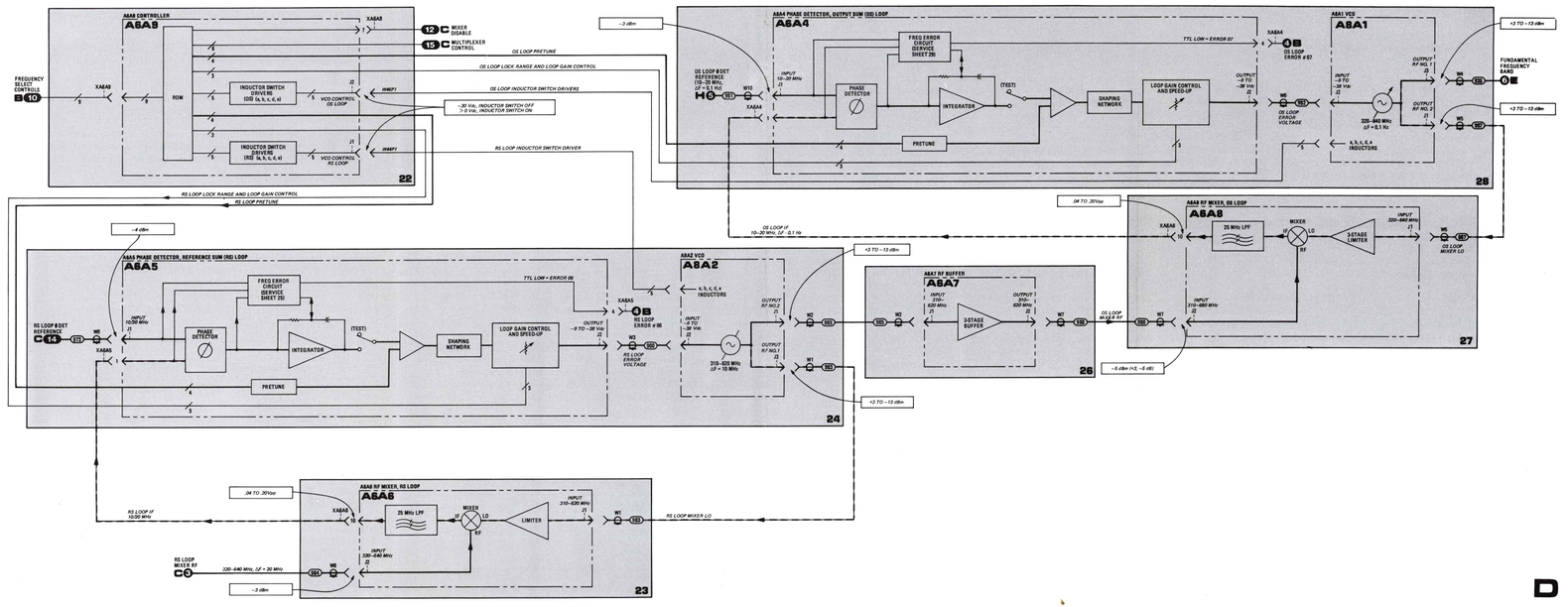


Figure 8-208. High Frequency Loops Block Diagram

SERVICE SHEET E
OUTPUT SECTION BLOCK DIAGRAM

TROUBLESHOOTING HELP

Block Diagram A
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post Repair Adjustment Procedures

PRINCIPLES OF OPERATION

The Output Section translates the basic 320 to 640 MHz band, to the Signal Generator's complete output range (Table 8-222),by doubling (for the doubler band), passing straight through or dividing (for the midband), or mixing (for the down-converter band). This section also controls the level of the RF signal. Coarse level control is provided by an electromechanical 5 dB-step attenuator at the RF output. Electronic leveling keeps the output level constant and provides finer step resolution (0.1 dB). The reverse power protection circuitry, if triggered, opens a relay in series with the output line. The trigger level is set for 10 volts peak RF. Limiting diodes provide protection until the relay opens. AM is generated within this section when a modulation signal is applied.

Table 8-222. Frequency Bands Derived from the Basic Band

Band	Frequency Range
Down-Converter Band	0.01—120 MHz
Midband	120 MHz—640 MHz
Doubler Band	640 MHz—1280 MHz

TROUBLESHOOTING

If the front panel RF output is not correct and the problem has been traced to the Output Section by following the overall instrument troubleshooting procedure, check the input signals shown in Table 8-223.

Table 8-223. RF Output Section Input Signal Levels

Signal	Measure at	Frequency	Level
320 to 640 MHz Fundamental band signal	Cable W4 (white/orange/green) going to A4A4J1	Same as front panel frequency setting between 320.0—639.999.9999 MHz	+3 to −13 dBm (varies with frequency)
520 MHz Reference	Cable W18 (white/orange/violet) going to A4A5J3	520.0 MHz	0 dBm ±0.75 dB (when front panel setting <120 MHz)

If these input signals are normal, the problem is in the Output Section. Output Section problems can be divided into five classes:

1. Front panel status indicates error in Output Section.
2. Output frequency wrong.

SERVICE SHEET E (Cont'd)

3. RF output level wrong.
4. Amplitude Modulation (AM) problems.
5. Harmonics.

Output Section Status Error

There are two error conditions in the output section which will cause the front panel status light to flash. Error code 09 indicates the reverse power detect circuitry has triggered. Turn to Service Sheet 36 to troubleshoot a problem with this circuitry. Error code 10 indicates a power level problem which has two possible sources. Remove the top cover of the instrument. If the LED indicator on top of the A4A4 assembly is lit, there is a problem with the A4A4 Distributor Assembly. Begin troubleshooting on Service Sheet 30. If the indicator on A4A4 is off and the indicator on top of the A4A7 AGC Assembly is lit, the problem could be any output section board. Begin troubleshooting with the RF Output Level Wrong section.

NOTE

Under certain conditions, it is possible for Status code 10, "Amplitude out of specification", to turn on when no amplitude error exits. This can happen during fast repetitive sweeps (for example, Auto Sweep or Remote Stepped Sweep, with the time/step less than 1 ms). Corrective action is not required unless code 10 persists in conditions other than the fast repetitive sweep.

Output Frequency Wrong

The most likely cause is bad digital data from the DCU. Continue troubleshooting with the A4A4 Assembly (Service Sheet 30). This assembly would be affected by bad data and its output is easy to check.

RF Output Level Wrong

1. Set the RF output level of the Generator to the values in the first column of Table 8-224. If the RF output of the instrument is not the specified value, measure the power level at A4A1J4 and compare to the value in the table. If the power level at A4A1J4 is correct, the problem is most likely the mechanical step attenuator. Continue troubleshooting on Service Sheet 36.

When the level at A4A1J4 is bad, the problem is with one of the output section boards. Continue troubleshooting with step 2.

Table 8-224. RF Output Level Setting Vs Power Level

Front Panel RF Output Level Setting (dBm)	A4A1J4 Level (dBm)
+16.0	+16.0
+ 5.0	+10.0
0.0	+10.0
−10.0	+10.0
−30.0	+10.0
−70.0	+10.0

SERVICE SHEET E (Cont'd)

If the indicator light on top of the A4A7 assembly is lighted, the power output level at A4A1J4 is wrong.

2. Measure the outputs of the A4A4 Distributor Assembly. Set the Generator's front panel frequency to the values in the first column of Table 8-225. Tune the spectrum analyzer to the values in the second column and measure the power level at each of the three output jacks. Compare these to the values given in the table.

If the output levels are normal, the A4A4 assembly is good. Continue troubleshooting with step 3, below. If these levels are abnormal, there is a problem with A4A4 or the digital data from the DCU. Continue troubleshooting with A4A4 on Service Sheet 30.

Table 8-225. A4A4 Distributor Assembly Frequency Vs Power Level

Front Panel Frequency (MHz)	A4A4 Output Frequency (MHz)	Level (dBm)		
		A4A4J2	A4A4J3	A4A4J4
80.0	600.0	<−26	>0	<−52
150.0	150.0	<−37	<−38	>0
190.0	190.0	<−35	<−36	>0
300.0	300.0	<−34	<−36	>0
400.0	400.0	<−27	<−28	>0
600.0	600.0	<−26	<−27	>0
800.0	400.0	>0	<−27	<−56
1000.0	500.0	>0	<−28	<−55

3. Set the Generator to the center frequencies in Table 8-226. Each of these center frequencies uses a different signal path in the Output Section. Remeasure the levels at A4A1J4 (see Table 8-224). If the level at A4A1J4 is wrong for each frequency, the problem is probably in the output amplifier circuitry on A4A1, or the AGC circuitry (A4A7). Proceed to step 4.

If the levels at A4A1J4 are correct for at least one center frequency, the problem is probably in one of the intermediate amplifier stages. Proceed to step 5.

Table 8-226. Output Bands for Three Front Panel Frequency Settings

Front Panel Freq. (MHz)	Band
80.0	Down Converter
600.0	Midband
1200.0	Doubler

4. Set the Generator to 100.0 MHz and +16 dBm RF output level. Drive the A4A1J2 input with an auxiliary signal generator with calibrated, adjustable output level. Set this auxiliary generator to 100.0 MHz and −20 dBm. Measure the RF output level of the Generator under test. Then increase the output level of the auxiliary generator until the Generator under test output is at +16 dBm.

SERVICE SHEET E (Cont'd)

If more than +6 dBm output level is required from the auxiliary generator to drive the Generator under test output to +16 dBm, the A4A1 assembly has low gain. Continue on Service Sheet 34 to troubleshoot this problem.

Decrease the RF output of the auxiliary generator so the output of the Generator under test assumes the value in Table 8-227. Check that:

a. There is a one-to-one decrease in the output levels of the auxiliary generator and the Generator under test.

b. The detector output voltage as measured on the output section motherboard (A4A10TP1) changes the same amount (in dB) as the output power. The values in the table are typical.

If either of these conditions is not met, there is a problem on the A4A1 assembly (Service Sheet 34). If these conditions are met, the problem is most likely on the A4A7 assembly (Service Sheet 37). Continue troubleshooting on the appropriate service sheet.

Table 8-227. RF Output Level Vs. Detector Output Voltages

Generator Under Test RF Output Level (dBm)	Detector Output Voltage (Vdc)
+16	3.79
+10	1.91
+ 6	1.21
0	0.58

5. If one or more frequency bands is normal, remove the A4A7 AGC assembly from the instrument. This removes bias from all the PIN modulators. Set the front panel frequency to within the nonfunctioning band. Using Table 8-228, identify the assembly containing the PIN modulator for the nonfunctioning band and measure the output. The level must be less than −40 dBm because the modulator should be turned fully off. If the output level is too high, there is a problem with the PIN modulator. In this case continue troubleshooting on the PIN modulator portion of the assembly.

Extend the PIN modulator assembly and short together with a small clip the two test points listed in Table 8-228. This should turn the modulator fully on. Measure the level at the output of the assembly. The level should be greater than the maximum level shown in Table 8-228. If the level is too low, there is a problem on that assembly. Therefore, continue troubleshooting on the service sheet for that assembly.

6. Leave the PIN modulator assembly extended with the test points shorted together. Connect all cables so the signal from the assembly reaches the A4A1 Output Amplifier Assembly. Measure the level at A4A1J4. This level should be +16 dBm or greater. If the level is too low, there is a problem with the A4A1 assembly. In this case, continue troubleshooting on Service Sheet 34.

SERVICE SHEET E (Cont'd)

Table 8-228. PIN Modulators Output Levels

Band	PIN Modulator			
	Assembly	Output	Max Output Level (dBm)	Test Points
Down Converter	A4A5	A4A5J2	−5	TP5 and TP6
Midband	A4A1	A4A1J4	+16	TP2 and TP13
Doubler	A4A2	A4A2J2	−5	TP6 and TP9

If the level is normal, the problem is most likely on the A4A7 AGC Assembly. Therefore, continue troubleshooting on Service Sheet 37.

To determine if the problem is on all frequency bands, set the Generator to the frequency settings in the first column of Table 8-229.

Table 8-229. AM Problem Isolation

Front Panel Frequency Setting (MHz)	Band	Modulator Assembly	Service Sheet
80.0	Down Converter	A4A5	31
600.00	Midband	A4A1	34
1200.0	Doubler	A4A2	33

SERVICE SHEET E (Cont'd)

If there are problems on all bands, the cause is with the A4A7 AGC assembly so continue with Service Sheet 37. If the problem is only on one band, the cause could be on the modulator assembly listed in Table 8-229, or the AGC assembly (A4A7).

Determine if harmonics are out of specification in all bands or just in one. If harmonics are a problem in all bands, the output amplifier could be defective. Drive the output amplifier from an external signal source and if harmonics are still there, the output amplifier microcircuit is causing them. Continue troubleshooting on Service Sheet 35. Check the bias levels closely.

When harmonics are only present in one band, backtrace until the source is found.

High Frequency Loops
Block Diagram
SERVICE SHEET D

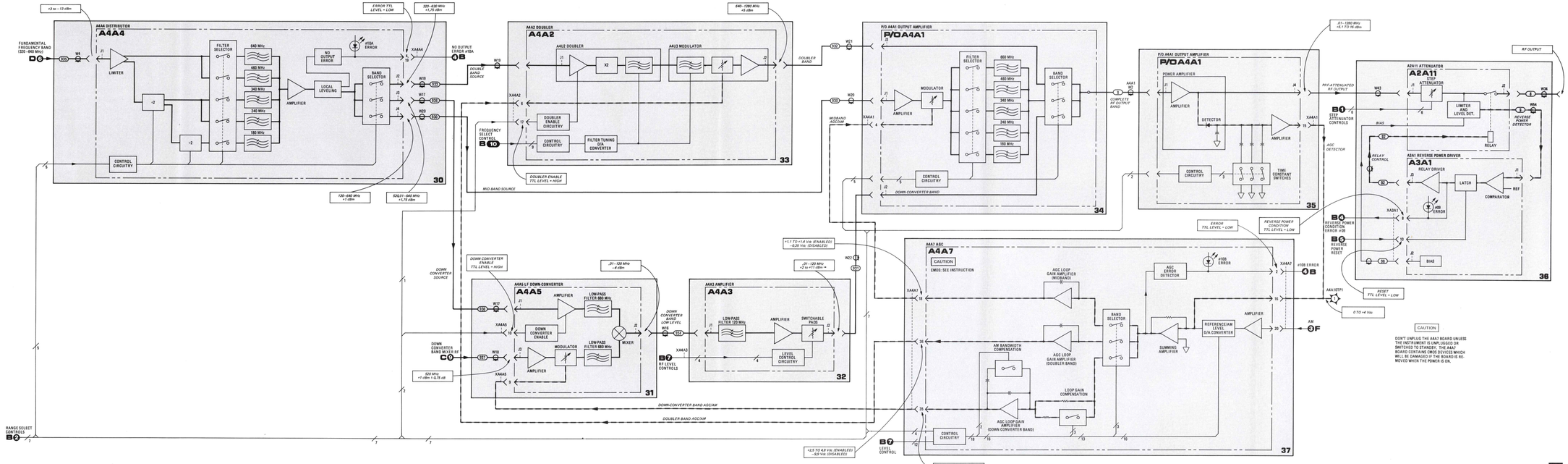


Figure 8-209. Output Section Block Diagram

SERVICE SHEET F
MODULATION SECTION BLOCK DIAGRAM

TROUBLESHOOTING HELP

Block Diagram A
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post Repair Adjustment Procedures

PRINCIPLES OF OPERATION

The Modulation Section controls the amplitude and frequency modulation modes of the Signal Generator. The two primary output signals from this section are the AM modulating signal (AM signal) and the FM modulating signal (FMS LOOP ϕ DET REFERENCE). In the AM mode, the modulating signal is routed to the Output Section where the actual amplitude modulation of the RF signal takes place. In the FM mode, a 20 MHz modulating signal is routed to the Low Frequency Loops Section where it is combined with other signals.

The Signal Generator can be amplitude and frequency modulated using internal or external modulating signals. The internal modulating signals are derived by dividing the 10 MHz signal from the Reference Section. The accuracy and stability of the internal modulating signals are the same as the reference source. External modulation signals are coupled into the Modulation Section through the front panel MODULATION INPUT jack (AM and FM) and the AUX FM INPUT jack (FM only) located on the rear panel.

The frequency modulated 20 MHz signal is generated by applying the modulating signal to the varactor diode that forms part of the VCO's tank circuit. The result is that the 140 MHz VCO output is frequency modulated. The 140 MHz VCO output is then heterodyned with the stable 120 MHz signal to produce the frequency modulated 20 MHz signal.

Phase-locked FM is possible down to a rate of 20 MHz with some limitations on peak deviation at modulation rates below 200 Hz. In EXTERNAL DC mode phase-locked FM is not possible because this mode disables the FM Loop.

TROUBLESHOOTING

General

There are three types of Modulation Section problems covered by this procedure:

1. FM loop unlocked and/or 20 MHz output (A4A10J5) level wrong.

2. Incorrect depth, deviation or function.

3. AM or FM distortion too high.

There is a separate troubleshooting procedure for each of these problem types. If the problem symptoms fit more than one type, start troubleshooting with the symptom highest in the list.

When the front panel STATUS light flashes and the error code is 08, it indicates the FM loop is unlocked. The LED on top of the A4A6 assembly should light when this error occurs.

FM Loop Unlocked And/Or 20 MHz Output (A4A10J5) Level Wrong

1. Remove the A4A8 Phase Detector and A4A9 Modulation Driver Assemblies from the instrument. This leaves the VCO (A4A6) free-running. Check for the following:

   a) Signal at A4A6J1 (top of A4A6 assembly) is 140.0 ± 0.1 MHz at greater than −5 dBm.

   b) Signal at A4A10J5 (20 MHz OUT on mother board) should be 20.0 ± 0.1 MHz. Level should be greater than −20 dBm when in FM mode and less than −50 dBm when not in FM mode.

   c) The LED on top of A4A6 should not be lit.

If any of these conditions are not met, there is a problem on the A4A6 assembly. In this case continue troubleshooting on Service Sheet 39.

2. Plug the Phase Detector Assembly (A4A8) into its connector in the instrument and connect the cable between A4A8 and A4A6. This closes the loop but no modulation is applied because the Modulation Driver (A4A9) is not installed. Check the following:

   a) The LED on top of A4A6 should not be lit.

   b) The signal at A4A8J2 (top of A4A8 assembly) should be 14.0 MHz ±1 count.

If these conditions are met, the loop is locked and the A4A6 and A4A8 assemblies are probably good. The problem is most likely caused by the A4A9 assembly.

Output Section Block Diagram
SERVICE SHEET E

SERVICE SHEET F (Cont'd)

If the frequency at A4A8 is wrong, the loop is unlocked so continue troubleshooting with step 3. If the frequency at A4A8 is correct but the LED is lit, the loop is locked but the phase lock detector on A4A6 is probably malfunctioning so continue troubleshooting with Service Sheet 39.

3. Disconnect the white/yellow/black cable from A4A8J1. This removes the VCO signal from the phase detector. Check for:

a) Voltages at A4A8 pin 10 (mother board TP2) > +7.5 Vdc.

b) Signal at A4A6J1 > 20.5 MHz.

If both conditions are met, continue troubleshooting with step 4. If condition (a) is not met, A4A8 is bad or the 10 MHz reference signal is not reaching A4A8. Continue troubleshooting with Service Sheet 38.

4. Reconnect the cable to A4A8J1. Disconnect the violet cable from A4A10J3 (10 MHz input on mother board). This removes the 10 MHz reference signal from the phase detector. Check for:

a) Voltage at A4A8 pin 10 (mother board TP2) more negative than −6.5 Vdc.

b) Signal at A4A6J1 < 19.5 MHz. Measure with the cable connected using a tee adapter. Use the high impedance input of the counter.

If condition (a) is not met, the A4A8 assembly is bad. If condition (a) is met but condition (b) is not, the A4A6 assembly is bad.

If both conditions are met, this procedure has failed to isolate the problem. In this case continue troubleshooting the VCO on Service Sheet 39.

Incorrect Depth, Deviation or Function

Begin by checking the modulation driver (A4A9) assembly. The modulating signal outputs are available on mother board test points TP4 (AM) and TP3 (FM). These signals should be the level specified on the block diagram (Service Sheet F), and the frequency selected by the front panel MOD switches. If either signal is not normal, troubleshoot the A4A9 assembly (Service Sheet 40) to find the cause. If these signals are normal but the modulation level of the front panel RF output is wrong, the problem is most likely in the A4A6 VCO assembly (FM) or the Output Section (AM). In this case continue troubleshooting on Service Sheet 39 or Service Sheet E.

Distortion Too High

If AM and FM distortion are both too high, the problem is likely to be on the A4A9 Modulation Driver assembly. Measure distortion on the mother board test points TP4 (AM) and TP3 (FM). Distortion should be less than 0.4%. If distortion is higher, proceed to Service Sheet 40 to troubleshoot A4A9.

If only FM distortion is high, the A4A6 FM VCO is the likely cause. Continue troubleshooting on Service Sheet 39.

If only AM distortion is high, the problem is in the Output Section. Continue troubleshooting on Service Sheet E.

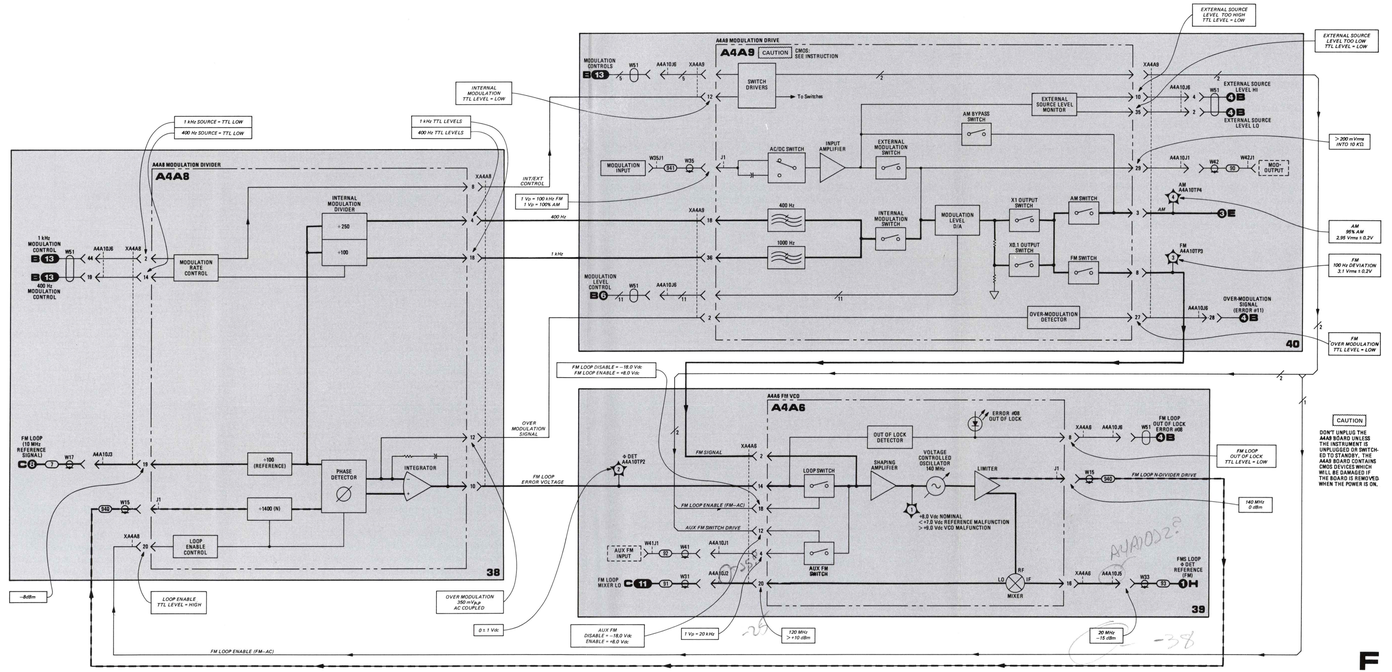


Figure 8-210. Modulation Section Block Diagram

SERVICE SHEET G
FRACTIONAL-N LOOP BLOCK DIAGRAM

TROUBLESHOOTING HELP

Block Diagram A
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post Repair Adjustment Procedures

PRINCIPLES OF OPERATION

The Fractional-N Loop (FN Loop) generates frequencies from 100 to 200 MHz in 100 Hz steps using a 100 kHz reference. The 100 kHz reference is derived by dividing the 10 MHz output signal from the Reference Section. The output frequency from this section is a function of front panel frequency digits D_5, D_4, D_3, D_2, D_1, and D_0 (that is, the six least significant digits) in the Generator's basic frequency band (that is, 320—640 MHz). The three least significant digits, D_2 — D_0, represent the fractional portion of the frequency while the next three digits (D_5 — D_3) contain the integer portion of the frequency. To determine the FN Loop VCO frequency from the front panel frequency display (RF OUTPUT frequency) use the following formula:

$$\text{FN VCO Freq.} = (200 - \underbrace{D_5\,D_4\,D_3}_{\text{Integer Portion}}\,\underbrace{D_2\,D_1\,D_0}_{\text{Fractional Portion}})\ \text{MHz}$$

The Fractional N Loop uses a frequency synthesis technique known as Fractional N. With only one phase lock loop the FN Loop can produce signals with far greater frequency resolution than the traditional N Loop. In an N Loop the VCO is restricted to only work at frequencies N times the reference frequency. Therefore, it can only generate signals that are integer multiples of the reference frequency (VCO Freq. = N x Ref Freq.).

The FN Loop is very similar to the N Loop. It contains all the basic elements of the N Loop with the addition of several new elements. In fact, if the selected frequency does not have a fractional part (that is, when D_2 — D_0 are zeros), the FN Loop works like the N Loop.

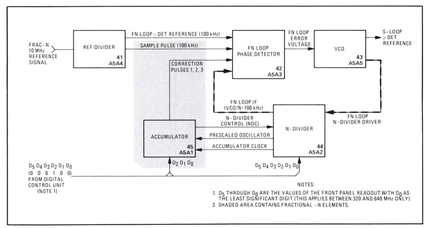


Figure 8-211. Simplified Block Diagram of Fractional-N Loop

SERVICE SHEET G (Cont'd)

Figure 8-211 is a simplified block diagram of a Fractional N phase lock Loop with the shaded area containing the Fractional-N elements.

The major difference between the FN Loop and the N Loop is that the FN loop VCO is not restricted to operating at only N times the reference frequency, but can also operate at frequencies that are fractional multiples of the reference frequency. The frequency resolution of the FN Loop is 100 Hz which means the FN VCO is capable of operating at a fractional multiple of 0.001 of the reference signal (0.001 of 100 kHz = 100 Hz).

Assume that the VCO frequency desired is 199.9900 MHz. In a traditional N Loop it would be impossible to phase lock the loop, since the desired VCO frequency, 199.9900 MHz, is a fractional multiple (1999.9) of the reference frequency. In order to phase lock the loop, the VCO frequency divided by N (VCO/N) must equal the 100 kHz reference signal. This would require an N that had a fractional component (N = 1999.9).

In the FN Loop, division by a fractional component is possible. The N Divider (A5A2) cannot divide by a fractional component directly but it is capable of changing from an N to an N-1 divider. Fractional division is accomplished by dividing by an integer (N) for the number of times and one less than the integer (N-1) for a number of times. The fractional N is then the average of N and N-1. For example, if an N of 1999.9 is required, the N Divider divides by 2000 (N) nine times and by 1999 (N-1) one time. This dividing between N and N-1 results in an average N of 1999.9.

A method of determining when to divide by N or N-1 is required. This is the purpose of the Accumulator (A5A1). When the FN Loop is operating with a fractional part, the VCO/N signal no longer equals the reference frequency, hence the phase difference between the two signals starts to increase. When analyzing the phase relationship between the reference and VCO/N signals it is better to view it in terms of reference periods. A reference period is defined as the time required for the reference signal to complete one cycle (10 µs). The Accumulator does not actually measure the phase difference but it computes what the phase difference should be after each reference period.

Since the phase difference is continuously increasing each reference period, the output from the phase detector is continuously increasing. In an N Loop the error voltage from the phase detector is used to tune the VCO frequency in a direction to reduce the phase difference or error. However, in the FN Loop, the phase difference is allowed to increase until the total or accumulate phase difference reaches or exceeds one full VCO cycle (360°) of phase. Prior to the reference period that the phase difference reaches or exceeds one full cycle, the Accumulator generates an N Divider Control (NDC) signal causing the N Divider to divide by one less than the previous N.

SERVICE SHEET G (Cont'd)

Dividing the FN VCO frequency by N-1 instead of N causes the N divider to reach its terminal count one VCO period sooner. This effectively advances the VCO/N signal one VCO period which counteracts or cancels the previous phase advancement.

When the N Divider divides by a number N, the VCO/N signal starts to lag the reference signal. When the phase difference between the reference signal and the VCO/N signal reaches or exceeds one cycle of phase, the N Divider is programmed to divide by N-1 which now causes the VCO/N signal to lead the reference signal. The resulting averaged VCO/N signal equals the reference frequency and the loop can be phase-locked even though the instantaneous VCO frequency is not an integer-multiple of the reference.

In the example in Figure 8-212, the FN VCO is operating at 199.9900 MHz. That would require that the N Divider divide by an N equal to 1999.900. The N divider is not capable of dividing by 1999.900 but it can divide by 2000 or 1999. Initially the N Divider starts out dividing by 2000. Since the VCO operates at 199.9900 MHz and N = 2000, the VCO/N signal to the phase detector would be 99.9950 kHz. Note, the phase of the VCO/N signal starts to lag the 100 kHz reference frequency which causes the phase detector to output an ever increasing dc level.

As the reference signal goes through one cycle the VCO, operating 1999.9 times faster, goes through 1999.9 cycles. For comparison an N Loop circuit is also examined.

In an N Loop if N = 2000 and reference = 100 kHz, the VCO frequency must equal 200.0 MHz to maintain phase lock. This means the N Loop goes through 2000.0 cycles for each reference period. Note the phase difference between the FN and N Loop VCO's after one reference period. The FN Loop lags the N Loop by 0.1 cycle which represents the fractional part of the frequency. To put it another way, the FN Loop VCO decreases by one tenth of a cycle relative to its integer part (N Loop) for every reference period. After the passage of two reference periods the FN VCO will have gone through 3999.8 cycles and the phase difference will have increased to 0.2 cycles. After each reference period the phase difference will increase by another 0.1 cycle. Table 8-230 illustrates this point.

After ten reference periods, the phase difference between the VCO/N and reference signals will have increased exactly one VCO cycle. Prior to the reference period that the phase difference reaches one VCO cycle the N Divider receives an NDC command from the Accumulator. This causes the N Divider to divide by 1999 (one integer less than 2000). This has the effect of cancelling the previous phase difference, hence the VCO/N frequency averaged over ten reference periods now equals the 100 kHz reference and therefore the loop can be phase locked.

This example uses a fractional N of 0.1. As another example, suppose the FN Loop VCO frequency was equal to 150.0050 MHz. This represents a fractional N of 0.95. For this example, the N Divider divides by N-1 (1500) nineteen out of twenty reference periods.

SERVICE SHEET G (Cont'd)

Table 8-230. Phase Difference Versus Reference Periods

Number of Reference Periods	Cycles Per Reference Period		Phase Difference (Cycles of Phase)
	N Loop = 200 MHz	FN Loop = 199.99 MHz (fraction N = 0.1)	
1	2000	1999.9	0.1
2	4000	3999.8	0.2
3	6000	5999.7	0.3
4	8000	7999.6	0.4
5	10000	9999.5	0.5
6	12000	11999.4	0.6
7	14000	13999.3	0.7
8	16000	15999.2	0.8
9	18000	17999.1	0.9
10	20000	19999.0	1.0

Continuously dividing by N and N-1 causes the phase detector to output a sawtooth waveform riding on a dc level. As shown in Figure 8-212, the output from the phase detector increases linearly (ramps) as the phase difference increases. The output continues to increase until the N Divider divides by N-1 which cancels the previous phase difference. This causes the output of the phase detector to return to its initial level.

The dc voltage level on which the sawtooth waveform is riding represents the proper tune voltage to phase-lock the VCO to the reference. Any ac components (sawtooth) on the dc tune voltage would prevent phase-lock and cause frequency modulation. To counteract this sawtooth waveform an equal but opposite ac signal is generated by the Fractional-N Correction Pulse Width-to-Current Converters. This signal is then summed with the phase detector output to cancel the sawtooth components, leaving only the desired dc tuning voltage.

The fractional portion of the VCO frequency contains the information needed to develop the signal that counteracts the changing phase detector output. The fractional part of the frequency is presented to the Accumulator in BCD form. Once during each reference period the contents of the Accumulator are incremented by the fractional part. The number stored in the Accumulator corresponds to the difference in phase between the VCO/N and the reference signal. Since the Accumulator is incremented each reference period, its contents represent an instantaneous fractional sum which grows until one VCO cycle of phase difference has occurred. The contents of the Accumulator as viewed with respect to time is shown in Figure 8-213. The contents of the Accumulator can be represented by a staircase ramp resetting each reference period when the N Divider divides by N-1. Note the contents of the Accumulator when viewed graphically, has the same characteristics as the sawtooth output from the phase detector.

SERVICE SHEET G (Cont'd)

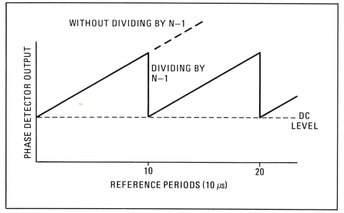


Figure 8-212. Phase Detector Output

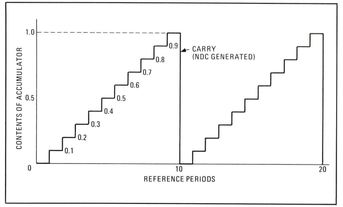


Figure 8-213. A Pictorial View of the Contents of the Accumulator

The numbers stored in the Accumulator are in BCD form. First the BCD information is inverted and then converted into signals with varying pulse widths. These signal lines are labeled Correction Pulse 1, 2, and 3. The Correction Pulses are then fed into the Pulse Width-to-Current Converter circuit which is located on the Fractional-N Loop Phase Detector Assembly (A5A3). The outputs from the Pulse Width-to-Current Converter circuit is then summed with the output from the phase detector. This cancels the sawtooth portion of the output from the phase detector leaving only a clean dc tuning voltage for the VCO.

Modulation Section Block Diagram
SERVICE SHEET F

SERVICE SHEET G (Cont'd)

TROUBLESHOOTING

When a problem has been traced to the Fractional N Loop or the instrument status code gives error 02, use the following procedure to isolate the problem to an assembly.

1. Check the 10 MHz reference signal at mother board test point TP1. This signal should be the level shown on the block diagram.

2. Pull out the A5A1 Accumulator Assembly. This removes the fractional part of the loop. Set the front panel frequency to 320.050 050 0 MHz. The loop should lock at a frequency of 149.9 MHz. Measure this frequency with a counter at A5A5J2. If the loop does lock, the Accumulator assembly is defective. If the loop doesn't lock, leave the Accumulator assembly out and continue with the next step.

3. Move the switch on the A5A3 Phase Detector Assembly to the TEST position. This opens the loop so that only the pretuning circuitry is driving the VCO. Set the front panel frequency to the values in Table 8-231 and measure the VCO frequency at A5A5J2. This tests all the bits in the pretuning by turning on but one at a time.

If all these frequencies are within limits, the VCO and pretuning are good. This is most of the A5A5 assembly so proceed to the next step. If one or more frequencies are bad, the problem is on the A5A5 assembly.

4. Measure the PDV signal from the A5A2 N Divider Assembly at TP5 on the mother board. The frequency of this signal should be 100 kHz ±5 kHz. Use an oscilloscope to check that levels of this signal are valid TTL levels (high is greater than 2.4 Vdc and low is less than 0.8 Vdc). If this signal is correct, the A5A2 assembly is operating properly, otherwise, there is a problem on A5A2.

Table 8-231. Fractional-N Loop Troubleshooting

Front Panel Frequency Setting (MHz)	Pretuning Bit On	A5A5 VCO Frequency Measured at A5A5J2 (MHz ±3 MHz)
320.099	A11	102
320.080	D5-8	122
320.040	D5-4	162
320.020	D5-2	182
320.010	D5-1	192
320.008	D4-8	194
320.004	D4-4	198
320.0	None	202

5. Measure the PDR and SMP signals from the A5A4 Reference Divider Assembly on the mother board at TP3 (PDR) and TP2 (SMP). The frequency of both these signals should be 100.0 kHz. Look at the waveforms on an oscilloscope to check for valid TTL levels and the timing relationship between the waveforms as shown in Figure 8-214.

If these signals are correct, the A5A4 is operating properly, otherwise, there is a problem on A5A4.

6. If all the previous checks do not show any problems, the A5A3 Phase Detector is the most likely cause of the problem.

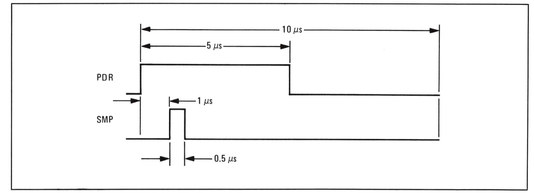


Figure 8-214. Timing Diagram for 100.0 kHz PDR and SMP Signals

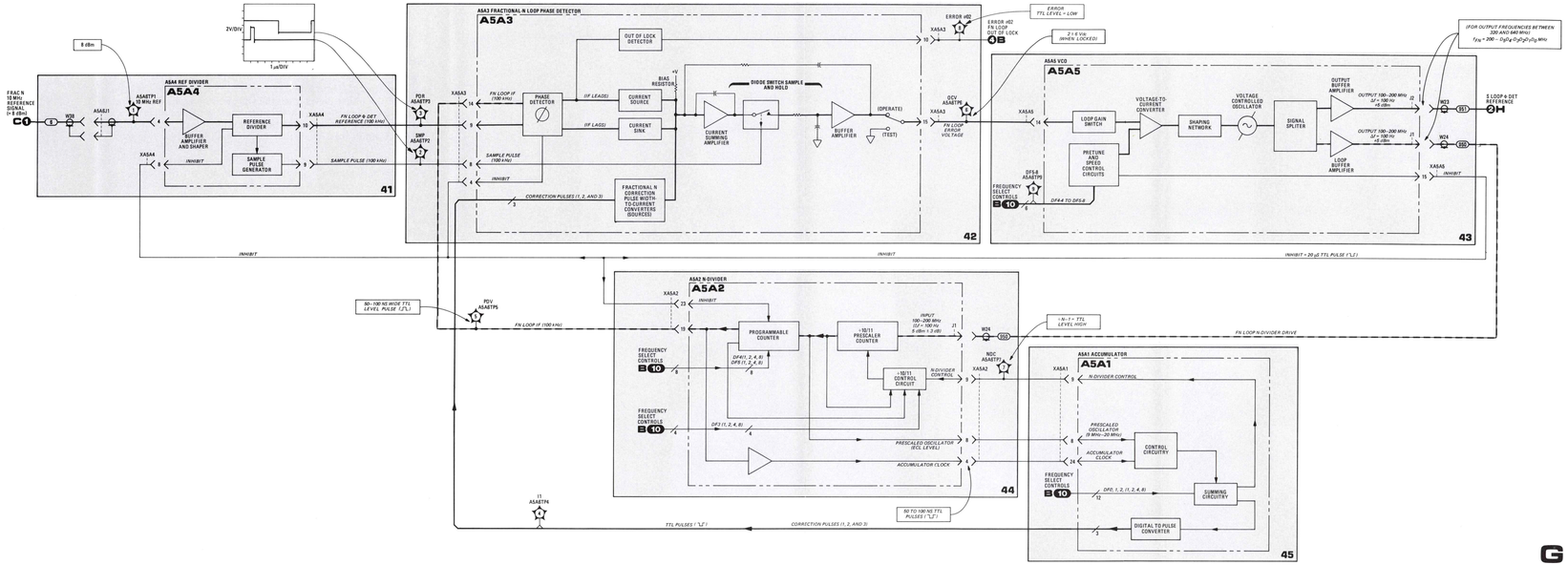


Figure 8-215. Fractional-N Loop Block Diagram

SERVICE SHEET H
LOW FREQUENCY LOOPS BLOCK DIAGRAM

TROUBLESHOOTING HELP

Block Diagram A
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post Repair Adjustment Procedures

PRINCIPLES OF OPERATION

The Low Frequency Loops Section serves two functions. First, it produces the 10 MHz to 20 MHz reference signal which is sent to the input of the phase detector (in the Output Sum Loop of the High Frequency Loops Section) so that the 320 MHz to 640 MHz, 0.1 Hz step resolution, fundamental frequency band can be generated. Secondly, if FM is desired at the output, it is summed in at this point.

The Low Frequency Loops are composed of three principal sections: the N Loop, the Low Frequency Sum Loop, and the FM Sum Loop. Each is a discrete phase lock loop. The N Loop takes the 10 MHz reference signal (which must be greater than +7 dBm) and multiplies it, using fractional-N synthesis, to a frequency band of 122 MHz to 221 MHz (1 MHz step resolution). This frequency is related to the 1 MHz and 0.1 MHz digits of the front panel readout display (D7 and D6 in the basic frequency band).

The signal from the N Loop is sent to the Low Frequency Sum Loop where it is locked to the signal from the Fractional-N Loop (Block Diagram C). This signal varies between 100 MHz and 200 MHz (100 Hz step resolution), but is divided by two decade counters (divide by 100) in the Low Frequency Sum Loop so that it varies between 1 MHz and 2 MHz (with 1 Hz resolution) at the input of the phase detector. The output of the Low Frequency Sum Loop (120 MHz to 220 MHz, 1 Hz step resolution) is sent to the FM Sum Loop.

In the FM Sum Loop, the signal is summed with either a 20 MHz continuous wave (CW) signal from the Reference Section or a 20 MHz frequency modulated signal from the Modulation Section (Block Diagram F). The output of this loop is a 100 MHz to 200 MHz (1 Hz step resolution) signal which is passed through a decade divider before leaving the board. The output of the decade divider is a frequency band which extends from 10 MHz to 20 MHz in 0.1 Hz steps. This signal is sent to the phase detector in the Output Sum Loop of the High Frequency Loops Section at 0 dBm to +16 dBm.

TROUBLESHOOTING

General

There are three phase lock loops in this section. The hierarchy is:

- N Loop (Error code 03)
- Sum Loop (Error code 04)
- FM Sum Loop (Error code 05)

There is a separate troubleshooting procedure for each loop. If more than one of the loops is unlocked, always start with the highest order unlocked loop because it will cause the lower order loops to be

SERVICE SHEET H (Cont'd)

unlocked. If the front panel status display gives a hardware malfunction code of 03, 04, or 05, then this code indicates at which loop to start troubleshooting.

N-Loop Troubleshooting

When it has been determined that there is a problem in the Low Frequency N Loop by troubleshooting on the overall block diagram (Service Sheet A) or the out-of-lock indicator being lit, perform the following sequence to isolate the defective assembly:

1. Unplug the A3A3 assembly and remove it from the instrument. This opens the loop and leaves the A3A4 assembly being driven by only the pretune voltage from A3A6. Set the front panel frequency to the values in the first column of the table on the block diagram. Measure the VCO frequency at A3A4J2 and compare it to the normal values given in the table. Each frequency setting turns on one bit of the eight which drive the pretune circuitry. If the VCO frequencies are correct, the A3A4 VCO assembly is operating properly and the A3A3 divider/phase detector assembly is the likely cause of the problem. In this case proceed to Service Sheet 46 and troubleshoot the A3A3 assembly.

2. When the VCO frequencies are not correct, use procedure in paragraph 3 of Sum Loop Troubleshooting.

Sum Loop Troubleshooting

When it has been determined that there is a problem in the Low Frequency Sum Loop by troubleshooting on the overall block diagram (Service Sheet A) or the out-of-lock indicator being lit, perform the following sequence to isolate the defective assembly:

1. Remove the two jumpers on the A3A7 VCO Assembly and plug the board back into its socket. Removing these jumpers opens the loop and the VCO is driven only by the pretuning voltage from the A3A6 assembly.

2. Set the front panel frequency to the values in the first column of the table on the block diagram. Measure the VCO frequency at A3A7J1 and compare to the normal values given in the table. Each frequency setting turns on one bit of the eight which drive the pretune circuitry. If the VCO frequencies are correct, the A3A7 VCO is operating properly so proceed to step 4 to continue troubleshooting.

3. When the VCO frequencies are not correct, try the following:
   a) Perform the open-loop pretune adjustment procedure on the block diagram. If these adjustments can be made, repeat step 2. Otherwise, continue below.
   b) Measure the pretune voltage (TP8 on motherboard) for the front panel frequency settings given in the table on the block diagram. If these voltages are not normal, trace the problem starting with the pretune circuitry on A3A6.

Fractional-N Loop Block Diagram
SERVICE SHEET
G

SERVICE SHEET H (Cont'd)

If the open-loop pretune adjustments cannot be made but the pretune voltages (TP8) are normal, the A3A7 VCO is faulty.

4. Set the front panel frequency to 320.0 MHz. Adjust the GAIN control on A3A7 to set the VCO output frequency at A3A7J2 to 120.0 ±0.5 MHz. The W28 cable must be in place on A3A7J2.

Check the following:

a) A 2.0 ±0.5 MHz signal at TP5 on the mother board. Amplitude >3 Vp-p.

b) A steady TTL low signal at TP7 on the motherboard. This is the frequency detector output.

c) A steady TTL low signal at pin 11 of A3A5. This is the out-of-lock signal from A3A6 which should be active (low) when the loop is open.

5. Turn the A3A7 GAIN adjustment counterclockwise (CCW) while monitoring the frequency of the mixer output at TP5 on the mother board. Turning the GAIN adjustment CCW increases the VCO frequency. The N Loop output is at 122 MHz so the mixer output (TP5) should decrease in frequency, reach zero and begain increasing. When the frequency reaches zero and begins to increase, check TP7 on the motherboard for positive going TTL pulses. This is the output of the frequency detector and pulses indicate that the VCO is higher in frequency than the N Loop output.

If any of these checks gives abnormal results, the problem is likely on the A3A5 assembly, otherwise, the A3A6 Phase Detector Assembly is the likely cause of the problem.

FM Sum Loop Troubleshooting

When it has been determined that there is a problem in the FM Sum Loop by troubleshooting on the overall block diagram (Service Sheet A) or the out-of-lock indicator being lit, perform the following sequence to isolate the defective assembly:

1. Pull the A3A9 Mixer Assembly up far enough so that the bottom edge connector is completely out of the motherboard connector, but leave all the RF cables connected to the top of the assembly. This opens the loop by disconnecting the phase detector drive circuitry but leaves the mixer connected. In this condition, the VCO is only driven by the pretune voltage from A3A6. Set the front panel frequency to the values in the first column of the table in the block diagram. Measure the A3A8 VCO frequency at A3A8J3 and compare it to the normal values given in the table. Each frequency setting turns on one bit of the eight which drive the pretune circuitry.

2. If the VCO frequencies are correct, the A3A8 VCO is operating properly. Check that the outputs at A3A8J1 and A3A8J2 are the proper level as stated on the block diagram. Notice that the frequency at A3A8J2 is one-tenth that of the other outputs. Proceed to step 3 to continue troubleshooting. When the VCO frequencies are not correct, try the following:

   a) Perform the open-loop pretune adjustment procedure on the block diagram. If these adjustments can be made, repeat the VCO check. Otherwise, continue below.

   b) Measure the pretune voltage (TP8 on the mother board) for the front panel frequency settings given in the table on the block diagram. If these voltages are not normal, trace the problem starting with the pretune circuitry on A3A6.

If the open-loop pretune adjustments cannot be made but the pretune voltages (TP8) are normal, the A3A8 VCO is faulty.

3. Measure the output of the mixer at A3A9J2. Set the front panel frequency to values in the first column of the table on the block diagram. The loop should still be opened by having A3A9 out of the motherboard socket. The frequency output of the mixer should be 20 ±4 MHz for all front panel frequency settings and the level should be as stated on the block diagram. If correct, the mixer portion of A3A9 is good. Connect cable W26 to A3A9J2 but leave A3A9 out of the bottom connector.

4. The phase detector on A3A10 is a double balanced mixer so the frequency of the output will be the difference between a 20 MHz reference signal and the nominal 20 MHz IF signal from the mixer on A3A9. Using any front panel frequency setting, vary the GAIN adjustment on the top of the A3A8 VCO assembly to vary the frequency of the IF signal. Turning the GAIN adjustment clockwise increases the frequency of the IF signal. The normal cable must be connected to A3A9J2 but the IF signal can be monitored there with the *high impe-*

SERVICE SHEET H (Cont'd)

dance of a counter by using a T adapter. Vary the input IF frequency above and below 20 MHz and look for the difference signal at A3A10 pin 14.

5. Monitor the frequency detector output at A3A10 pin 12. Vary the IF signal frequency using the A3A8 GAIN adjustment and check the frequency detector output with the values shown in Table 8-232.

The GAIN adjustment is coarse so the IF signal frequency cannot be controlled precisely. The IF signal frequency limits in the table should be treated as approximate. It is important to verify that three different output states of the frequency detector exist but not that they occur at precise values of IF frequency.

6. If both the phase detector and the frequency detector operate normally as described above, the A3A10 assembly is probably normal. Therefore, the problem is most likely with the active circuitry onthe A3A9 assembly.

Table 8-232. IF Signal Vs Frequency Detector Output

IF Signal	Frequency Detector Output (A3A10 pin 12)
>21 MHz <19 MHz 20 ±1 MHz	dc level > +1.5 Vdc dc level <–3.0 Vdc pulses high-low levels change as IF goes above and below 20 MHz

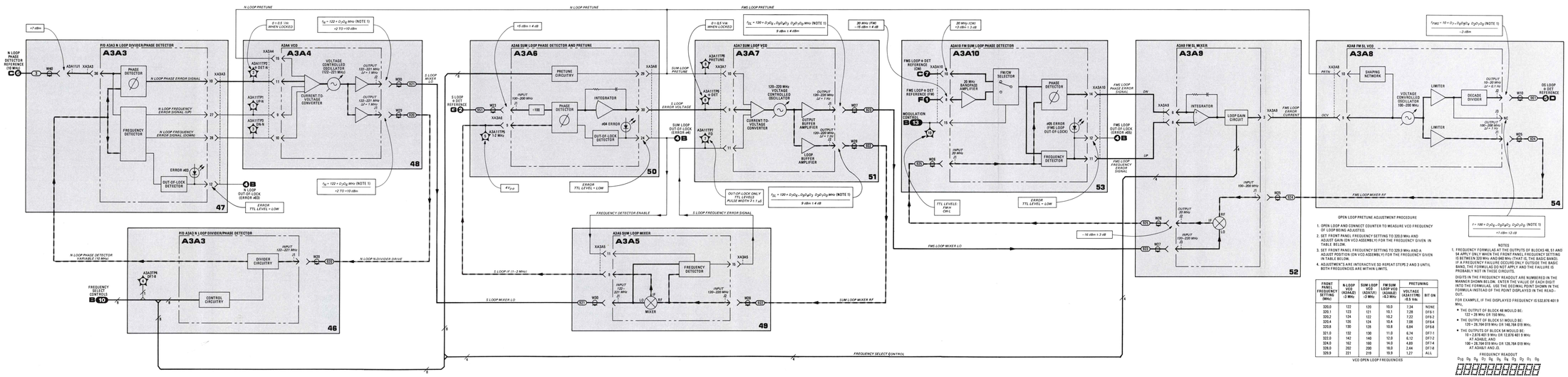


Figure 8-216. Low Frequency Loops Block Diagram

SERVICE SHEET I
POWER SUPPLY SECTION

TROUBLESHOOTING HELP

Block Diagram A
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post Repair Adjustment Procedures

PRINCIPLES OF OPERATION

The Signal Generator utilizes a switching power supply for reduced size, weight, and heat dissipation. The supply is made up of five major elements: an input rectifier/filter, the regulator switching transistors, a step-down/isolation transformer, output rectifiers (and associated L-C filters and IC regulators), and a pulse-width-modulated regulation network. The circuitry is on four boards. These are the Power Supply Motherboard, Inverter Board, Control Board, and the Linear Regulator Board. Supplementary circuits include current limiters, overvoltage protection networks, and a reference voltage supply.

At the power line receptacle, the instrument can be switched for use with 115 Vac or 220 Vac power. Following line filtering, the raw ac is rectified and coarsely filtered to produce plus and minus 160 Vdc. In the case of 115 Vac operation, voltage doubling occurs during rectification. The plus and minus 160 Vdc is then chopped at a 20 kHz rate to drive step-down/isolation transformer A7A3T3. Voltages at the tapped outputs of T3 are rectified and filtered. Sense lines from the +5.2 volt supply line are fed to the switching-regulator circuitry on the Control Board. The +5.2 volt line is the only line which is regulated by the switching action of the supply. The +20 Vdc, –10 Vdc, and –40 Vdc lines are maintained at constant voltage by linear regulators (Service Sheet 56).

The +5.2 volt line is regulated by a feedback network consisting of the constant voltage comparator, turn-on level comparator, 40 kHz oscillator, pulse-width modulator (duty-cycle control circuitry), and switch drivers. If the output voltage attempts to decrease, the feedback network senses the change and holds switching transistors A7A3Q3 and A7A3Q4 ON for longer periods of their switching cycles; an attempted increase is corrected by reducing the ON periods of the transistors. In this manner, the power delivered by the supply is matched to the requirements of the instrument, resulting in maximum operating efficiency.

TROUBLESHOOTING

This procedure can be used to isolate a malfunction in the power supply. Once the problem is isolated to an assembly, continue troubleshooting on the service sheet for that assembly to find the bad component.

WARNING

Plus and minus 160 Vdc, and line voltage, are present whenever the power cable is plugged in. This high voltage exists on the red heatsink, on the other portions of the inverter board and on the mother board. Be extremely careful when working in this area.

Before removing or inserting power supply plug-in boards, disconnect ac power cable and allow 30 seconds for filter capacitors to discharge.

Failure to observe these precautions may result in injury to personnel or damage to equipment.

CAUTION

If the line fuse burns out, do not replace it until the cause for the failure has been determined and repaired (by a qualified service person only and specifically with resistance checks in the power supply. See Service Sheet 55). Replacing this fuse in a damaged generator can cause additional damage.

1. General

Measure the +5.2V test point with a DVM. If the reading is not 5.20 ±0.02 Vdc and cannot be adjusted to bring the voltage within these limits, continue troubleshooting with the next step listed in Table 8-233, based on the DVM reading. The +5.2V supply should be operating normally before working on problems with the other supply voltages. If the +5.2V supply is normal and one of the other supply voltages is not, continue troubleshooting with step 5.

Table 8-233. +5.2V Test Point Conditions

DVM Reading	Condition	Next Step
V < 0.05	Shut down	2
0.05 < V < 5.20	Low Voltage	4
5.18 < V < 5.22	Normal	5
V > 5.22	High Voltage	6

2. Shut Down

Check the following:

a) The linear regulator overvoltage shut-down LED visible through an opening in the top of the power supply. If this LED is lit, the overvoltage shut-down has triggered so continue troubleshooting with step 3.

b) The fuses on the rear panel. If either fuse is blown, continue troubleshooting with Service Sheet 55.

Low Frequency Loops Block Diagram
SERVICE SHEET H

3. Linear Regulator Overvoltage Shutdown

Turn the line switch to STANDBY. Unplug the line cord from the rear panel. Remove the A7A1 Linear Regulator Assembly from the instrument. Mount the A7A2 Control Board Assembly on its extender board from the service kit. Connect a short jumper wire between TP5 and ground on A7A2. Connect the line cord and turn the line switch to ON. Measure TP1 (5.2V supply) on A7A2.

If the voltage is 5.20 ±0.02 Vdc or can be adjusted to within the range, the problem is on the A7A1 assembly so continue troubleshooting on Service Sheet 56. Otherwise, refer to Table 8-234 and continue troubleshooting with the next step listed in the table based on the actual voltage reading at TP1. The jumper from TP1 to ground must remain connected and A7A1 must remain out of the power supply. Once the 5.2V supply is normal, remove the jumper and install A7A1. Measure all supplies. If there are any abnormalities, restart with step 1 of this procedure.

4. +5.2V Supply Low

Turn the line switch to STANDBY and unplug the line cord from the rear panel. Mount the A7A2 Control Board Assembly on its extender board. Connect the line cord and turn the line switch to ON. Use a DVM with floating inputs and measure the voltage between pins 17 and 18 on the edge

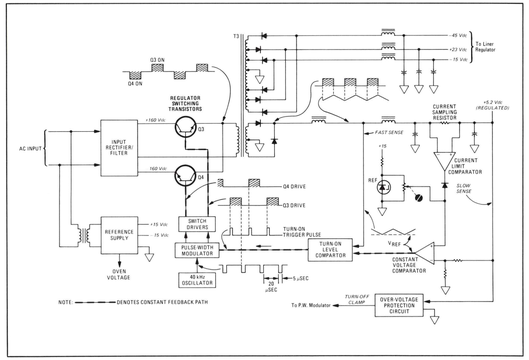


Figure 8-217. Simplified Power Supply Block Diagram

SERVICE SHEET I (Cont'd)

connector of A7A2. This voltage is the drop across the current sensing resistor in series with the output. If this voltage is greater than 0.070V, the load is drawing too much current and the supply is in current limit. Look for the cause of the excess current draw in the other sections of the instrument.

If the problem is not current limiting, look at TP6 and TP7 with an oscilloscope. The waveforms should be as shown on the block diagram. The pulse width of the positive part of the waveform should be 20 μs or more. If the pulse width is less, there is a problem on the A7A2 control board so continue troubleshooting on Service Sheet 57. If the pulse width is normal, the problem is most likely on the A7A3 inverter board or the A7A4 mother board so continue troubleshooting on Service Sheet 55.

5. +5.2V Supply Normal, Linear Regulator Problem

Table 8-234 gives the normal input and output voltages for the A7A1 Linear Regulator Board and the test points where these voltages can be measured.

Table 8-234. Linear Regulator Voltages

Normal Output (Vdc)	Output	Input	Normal Input (Vdc)
20.0 ±0.1	TP1	TP4	> +22.5
−10.0 ±0.04	TP2	TP5	> −12.5
−40.0 ±0.2	TP3	TP6	> −44.0

Measure the outputs and try to adjust any that are not within the normal range. If an output is too high, the problem is most likely on the A7A1 Linear Regulator. If an output voltage is low, measure the input. If the input is too low, the problem is likely to be on the A7A3 Inverter Assembly but if the input is normal, the A7A1 Linear Regulator is malfunctioning or the load is drawing too much current. Continue troubleshooting with the service sheet where the problem appears to be.

6. +5.2V Supply Higher Than Normal

This is most likely a problem with A7A2 Control Assembly. Continue troubleshooting on Service Sheet 57.

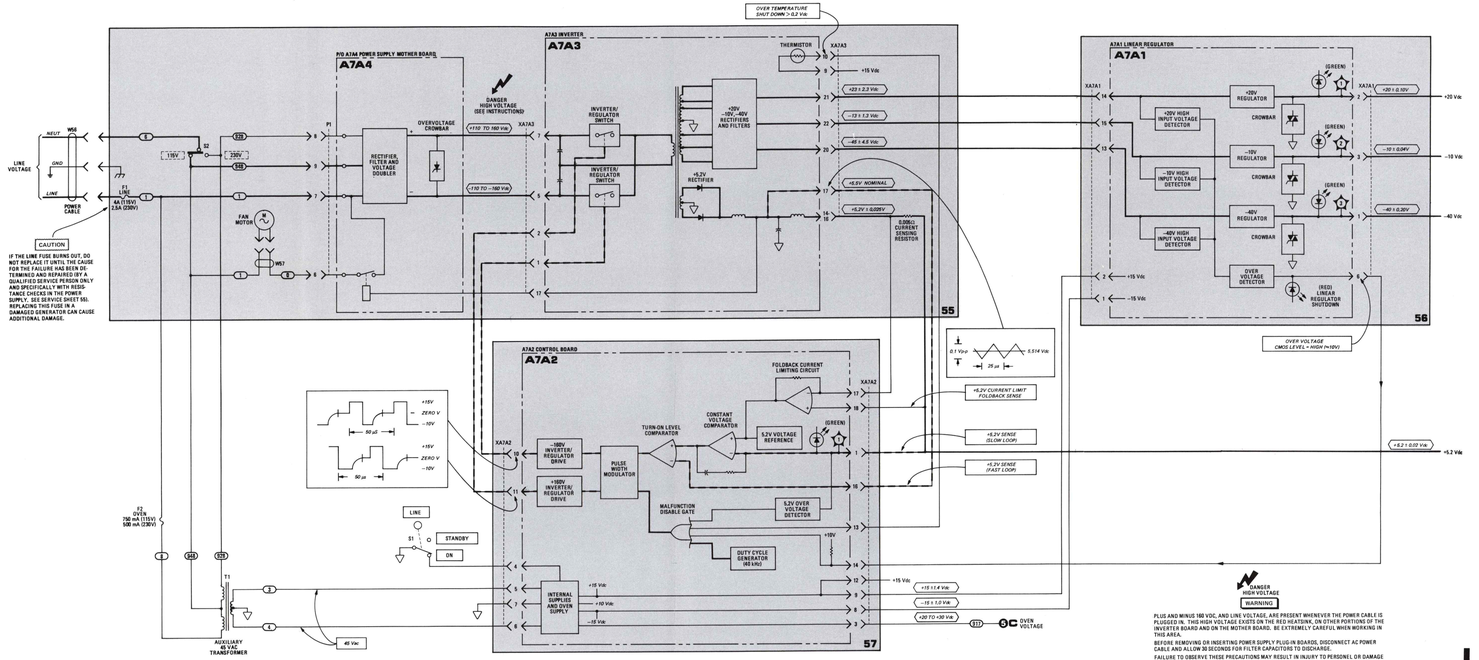


Figure 8-218. Power Supply Block Diagram

Power Supply Block Diagram
SERVICE SHEET



Printed in U.S.A.

SERVICE MANUAL

8662A Synthesized Signal Generator

10 kHz — 1280 MHz



P/O Section VIII
Service Sheets

1-17

Digital Control Unit (DCU)

HP Part Number 08662-90043
Printed January 1980
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HEWLETT PACKARD

SERVICE SHEET 1
A1A3 RIGHT KEYBOARD ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram B
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

Service sheet 1 depicts the circuit configuration for the right-hand side of the front panel keyboard. This keyboard is composed of data, storage, mode, and special function keys. These keys are essentially DPST pushbutton switches (normally open), arranged in a matrix with row (called "key down") and column outputs. Each button, when pressed, generates unique logic signals at the row and column outputs which are sent to the Keycode Board (Service Sheets 3 and 4) for decoding. There are five COLUMN ("C") lines and eight KEY DOWN ("KD") lines.

Many of the front panel buttons have lamps to indicate active conditions or call attention to malfunctions or errors. The lines which enter the keyboard to drive these lamps originate at the Sweep D/A Board (Service Sheet 17). The lamps are mounted on the circuit board in back of the buttons and light is transmitted to the front surface of the buttons by way of a "light pipe". Nine LEDs are used on this keyboard.

NOTE

The KEY CODE CHART at the lower right-hand side of the service sheet gives both the binary and hexidecimal codes at the output of the encoders on the Keycode Board. The binary code from this table should match that displayed by the seven LEDs at the top of the Keycode Board (which are visible when the top cover of the Signal Generator is removed).

Rotary Pulse Generator

The Rotary Pulse Generator (RPG) operates photoelectrically to produce a series of digital logic pulses that are used to increment or decrement various front panel functions. The RPG knob may be turned continuously in either direction. When the RPG is turned, it outputs two square wave pulses, in quadrature, with the leading pulse determining the direction of rotation. A logic circuit on the Keycode Board senses the direction and number of pulses being generated by the RPG and uses this information to adjust the user specified parameter.

The RPG is located in close proximity to, but not on, the Right Keyboard. The Keycode Board accesses the clockwise (CW) and counterclockwise (CCW) lines from the RPG by way of the Right Keyboard at pins 28 and 29. (See Keycode Board; Service Sheet 3).

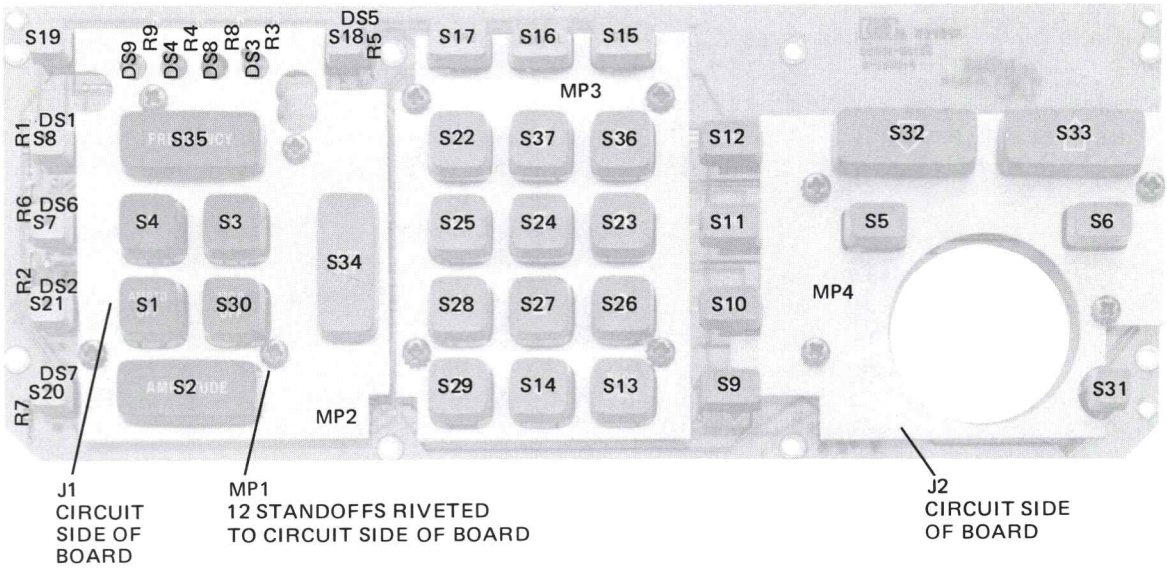


Figure 8-301. A1A3 Right Keyboard Component Locations

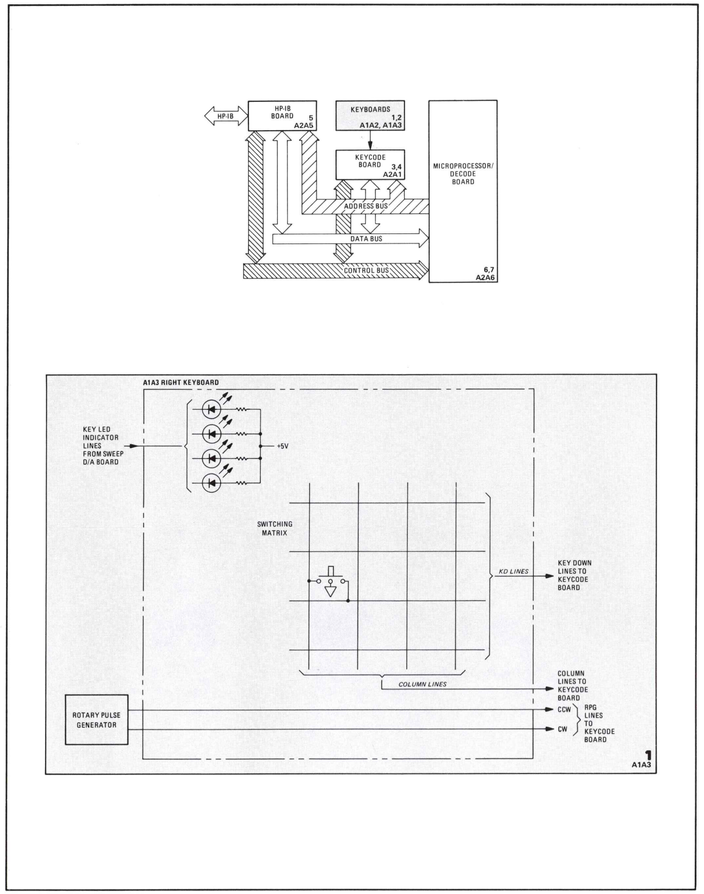
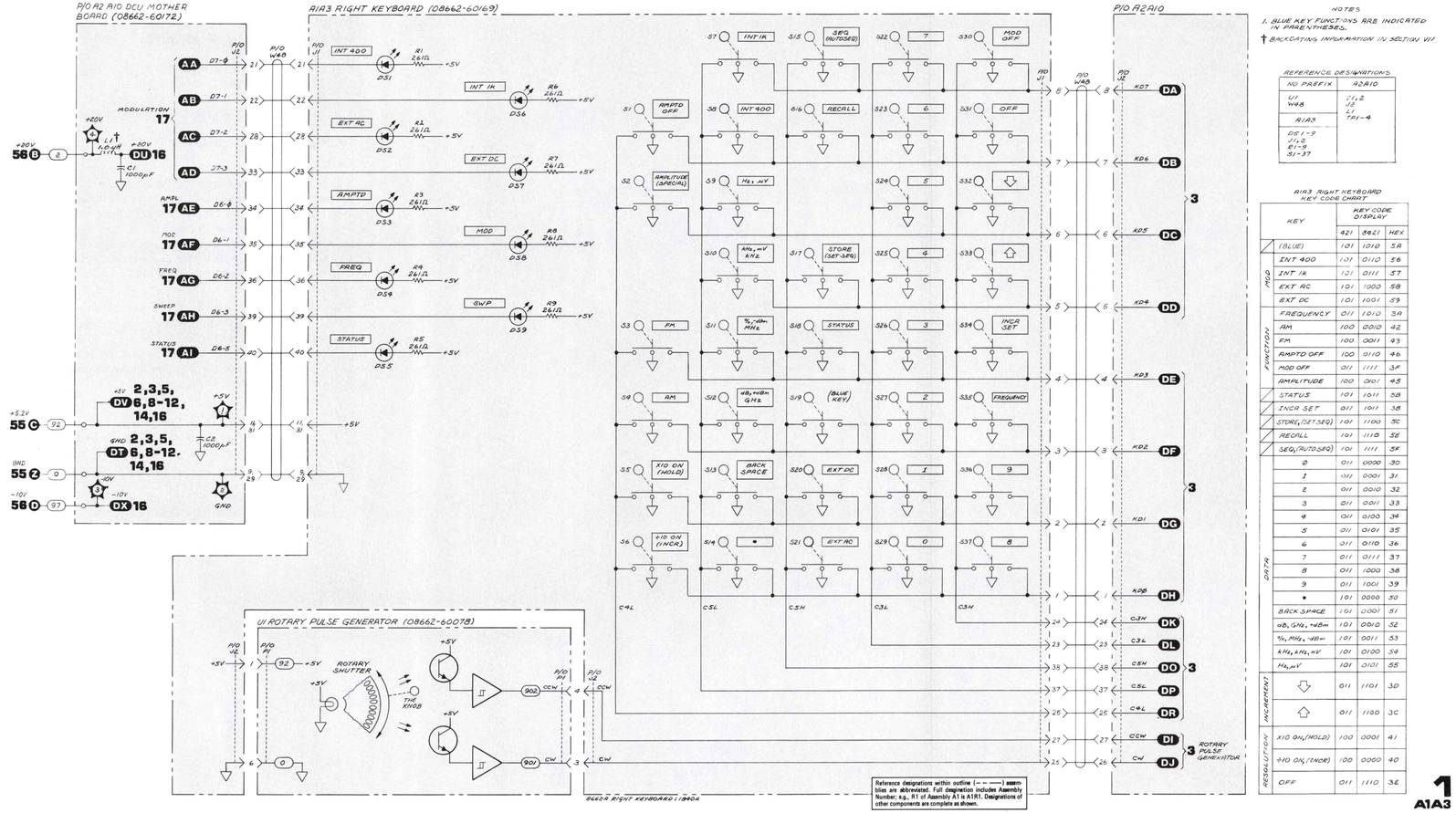


Figure 8-302. A1A3 Right Keyboard Block Diagrams



NOTES

1. BLUE KEY FUNCTIONS ARE INDICATED IN PARENTHESES.

† BACKDATING INFORMATION IN SECTION VII

REFERENCE DESIGNATIONS

NO PREFIX	A2A10
U1 W48	J1, 2 J2 J3 TP1-4
A1A3	
DS1-9 J1, 3 P1-9 S1-37	

A1A3 RIGHT KEYBOARD KEY CODE CHART

	KEY	KEY CODE DISPLAY		
		421	8421	HEX
	(BLUE)	101	1010	5A
MOD	INT 400	101	0110	56
MOD	INT 1K	101	0111	57
MOD	EXT AC	101	1000	58
MOD	EXT DC	101	1001	59
FUNCTION	FREQUENCY	011	1010	3A
FUNCTION	AM	100	0010	42
FUNCTION	FM	100	0011	43
FUNCTION	AMPTD OFF	100	0110	46
FUNCTION	MOD OFF	011	1111	3F
FUNCTION	AMPLITUDE	100	0101	45
	STATUS	101	1011	5B
	INCR SET	011	1011	3B
	STORE (SET-SEQ)	101	1100	5C
	RECALL	101	1110	5E
	SEQ (AUTOSEQ)	101	1111	5F
DATA	0	011	0000	30
DATA	1	011	0001	31
DATA	2	011	0010	32
DATA	3	011	0011	33
DATA	4	011	0100	34
DATA	5	011	0101	35
DATA	6	011	0110	36
DATA	7	011	0111	37
DATA	8	011	1000	38
DATA	9	011	1001	39
DATA	•	101	0000	50
DATA	BACK SPACE	101	0001	51
DATA	dB, GHz, +dBm	101	0010	52
DATA	%, MHz, -dBm	101	0011	53
DATA	kHz, Hz, mV	101	0100	54
DATA	Hz, μV	101	0101	55
INCREMENT	⇩	011	1101	3D
INCREMENT	⇧	011	1100	3C
RESOLUTION	X10 ON (HOLD)	100	0001	41
RESOLUTION	+10 ON (INCR)	100	0000	40
RESOLUTION	OFF	011	1110	3E

1
A1A3

Figure 8-303. A1A3 Right Keyboard Schematic

SERVICE SHEET 2
A1A2 LEFT KEYBOARD ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram B
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

Service sheet 2 is the schematic for the left-hand side of the front panel Keyboard. This keyboard is composed primarily of sweep function keys. These keys are DPST pushbutton (normally open) switches arranged in a matrix with row (called "key down") and column outputs. Each button, when pressed, generates unique logic signals at the row and column outputs which are sent to the Keycode Board (Service Sheets 8 and 9) for decoding. There are three COLUMN ("C") lines and eight KEY DOWN ("KD") lines.

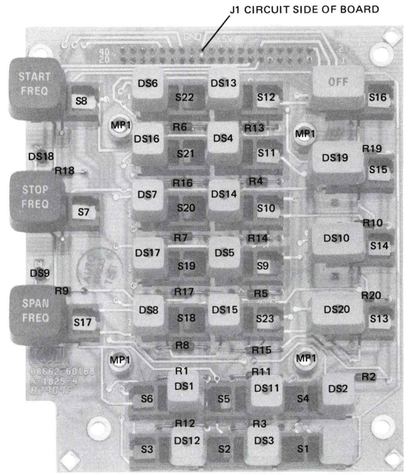
Many of the front panel buttons have lamps to indicate active conditions. The lines which enter the keyboard to drive these lamps originate at the Sweep D/A Board (Service Sheet 17). The lamps are mounted on the circuit board in back of the buttons and light is transmitted to the front surface of the buttons by way of a "light pipe". Twenty LEDs are used on this keyboard.

NOTE

The KEY CODE CHART at the lower right-hand side of the service sheet gives both the binary and hexidecimal codes at the output of the encoders on the Keycode Board. The binary code from this table should match that displayed by the seven LEDs at the top of the Keycode Board (which are visible when the top of the Signal Generator is removed).

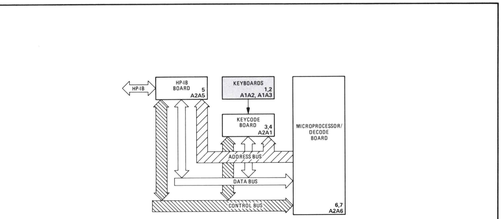
Right Keyboard A1A3 SERVICE SHEET 1

A1A2 ASSEMBLY



THE PLATE COVERING SWITCHES IS MP2

Figure 8-304. A1A2 Left Keyboard Component Locations



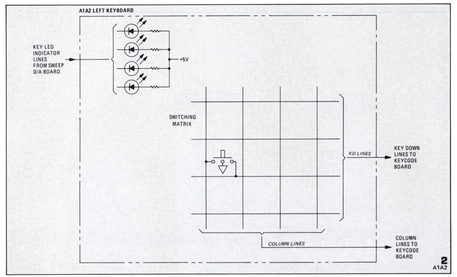
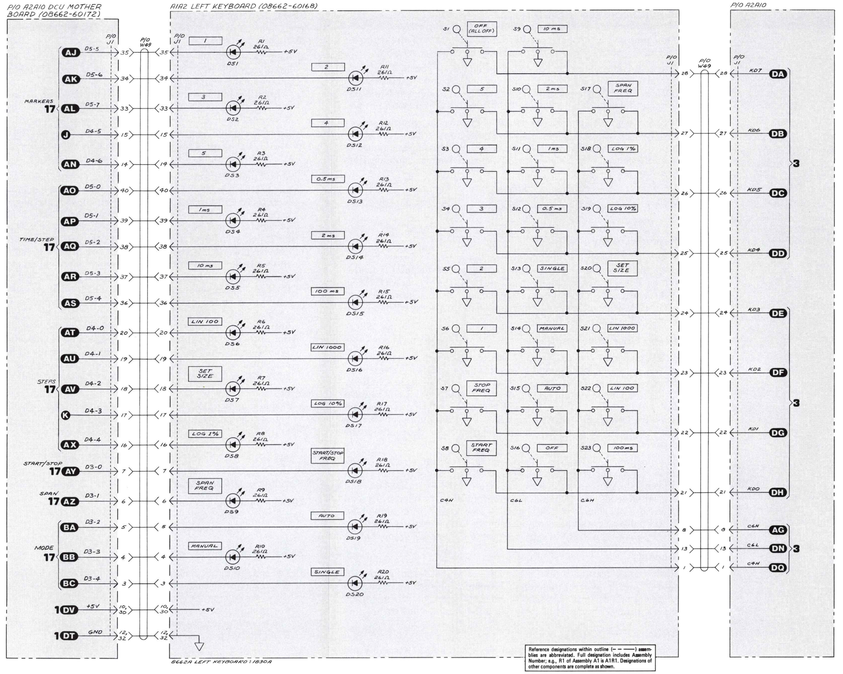


Figure 8-305. A1A2 Left Keyboard Block Diagrams



REFERENCE DESIGNATIONS

NO PREFIX	A2A10
W49	J1
A1A2	
DS1-20	
R1-20	
S1-23	

A1A2 LEFT KEYBOARD KEY CODE CHART

	KEY	KEY CODE DISPLAY		
		#2	#1	HEX
SWEEP	START FREQ	100	1000	98
	STOP FREQ	100	1001	99
	SPAN FREQ	110	1110	6E
STEP	LIN 100	110	1001	69
	LIN 1000	110	1010	6A
	SET-SIZE	110	1011	6B
	LOG 10%	110	1100	6C
	LOG 1%	110	1101	6D
FUNCTION	0.5 ms	110	0100	64
	1 ms	110	0101	65
	2 ms	110	0110	66
	10 ms	110	0111	67
	100 ms	110	1000	68
	OFF	110	0000	60
MODE	AUTO	110	0001	61
	MANUAL	110	0010	62
	SINGLE	110	0011	63
MARKER	1	100	1010	4A
	2	100	1011	4B
	3	100	1100	4C
	4	100	1101	4D
	5	100	1110	4E
	OFF (ALL OFF)	100	1111	4F

Figure 8-306. A1A2 Left Keyboard Schematic

SERVICE SHEET 3
P/O A2A1 KEYCODE ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram B
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The Keycode Board encodes signals from either the front panel keyboard or from external devices connected to the rear panel auxiliary input. It also encodes malfunction and status signals from the mainframe of the instrument so that the microprocessor can be alerted to various problems, errors, or malfunctions. The sweep step-time divider circuitry is also found on the Keycode Board.

The Keycode Board has been broken down into two service sheets. Service sheet 3 shows the keyboard inputs, auxiliary input encoding circuitry, and the peripheral interface adapter (PIA); service sheet 4 contains the malfunction detection and sweep step-time divider circuitry.

Peripheral Interface Adapter (PIA)

When the Signal Generator is first turned on, the peripheral interface adapter (PIA) is initialized as follows:

Pin(s)	Designation
2-4	Coded Key Down lines (PA0-PA2)
5-9	Coded Column lines (PA3-PA6)
10-13	Error alert inputs (PB0-PB3)
14-17	Error alert outputs (PB4-PB7)
18, 19, 40	Input interrupts (CB2, CB1, CA1)
39	Output handshake clear (CA2)
other pins	Reserved for data and μP signals

The signals which control the initialization process enter the Keycode Board by way of pins 9, 11-16, and 35.

When a front panel key is pressed, matrix data from the key down (KD) lines and the column (C) lines is encoded by U13 and U14 and then debounced by U12 and half of U4. After debouncing, pin 6 of U12 goes LO creating an interrupt to the microprocessor. The microprocessor reads the keyboard data and information which is present at pins 26-33 of the PIA. Following the read operation, the PIA generates a "handshake" signal at pin 39 (CA2) which resets the encoding circuitry.

Priority Keyboard Encoders

The key down (KD) and column (C) inputs drive priority encoders U13 and U14, respectively. These encoders generate a 3-bit code representing the input having the highest numerical value (priority). The B7 input, for example, has a higher priority than any other input. If two inputs are received at the same time, which is not a normal function, the output code will correspond to the input with the highest priority.

The step up, step down, and various sweep function control lines which enter the instrument by way of the rear panel AUX jack are encoded by U21 and U22, taking second priority to the front panel keyboard. If the user attempts to input information from the rear panel while at the same time trying to input from the front panel keyboard, the keyboard will have priority because of the various interlocks provided.

The user can prepare the Keycode Board (service sheets 3 and 4) to accept internal inputs (from the rear panel AUX connector) that have noise or bounce on them, or signals that are electronically clean (that is noise and bounce free). This is the function of the on-board jumper.

With jumper 1 (J1) in place, the debounce circuitry is bypassed so that the circuit response to clean signals is very fast; in the order of 100 nanoseconds. With jumper 2 (J2) connected, the circuit response is 7 to 9 milliseconds. This time delay gives un-debounced signals time to settle.

NOTE

The Signal Generator is shipped with the J1 jumper installed.

Keycode Display

Inputs PA0 through PA6 are sampled at the PIA by inverters. The outputs of these inverters feed the cathodes of seven LED indicator lamps. These lamps, which can be viewed from the top edge of the Keycode Board, give a visual indication of the code present at the input of the PIA. These codes can be interpreted as keystrokes with the data shown on schematics 1 and 2.

Rotary Pulse Generator (RPG)

The rotary pulse generator (RPG) operates photo-electrically to produce a series of digital logic pulses that are used to increment or decrement various front panel functions. The RPG consists essentially of a slotted disc through which light is passed. The disc is coupled to the RPG knob on the front panel. When it is turned, phototransistors sense the light as it flashes through the slots. Two square wave pulses are output, in quadrature, with the leading pulse determining the direction of rotation.

The clockwise (CW) and counter-clockwise (CCW) lines from the RPG enter the Keycode Board at pins 4 and 21 and trigger the RPG latch and encoding circuitry. This circuitry (formed by U11, U20, U21, and U22) then sends direction and rate information to the microprocessor. There are 120 slots in the RPG disc, so for every 3° of rotation of the RPG knob a pair of pulses is output from the RPG. For many functions, these pulses are divided in software to give a better feel to the control.

Monitor

Rather than treating the external reference and oven status inputs at pins 39 and 40 as error messages, the monitor formed by U26 treats these signals as status bits and sends them directly to the microprocessor through the data bus, bypassing the data bus buffers.

TROUBLESHOOTING

Signature analysis can be used to troubleshoot the A2A1 assembly and the instructions for using this technique are given in this service sheet, and service sheet 4. However, there are some checks that can be made with just a logic probe that will find the problem or narrow it down so signature analysis can be applied to a specific part of the circuitry.

SERVICE SHEET 3 (Cont'd)

Manual Procedure

1. Remove the top cover of the Generator so the yellow LED indicators on the top of the A2A1 assembly can be seen. Press a front panel key or activate a contact closure on the rear panel AUX connector (whichever is the source of the problem). As long as the key is pressed, the keycode for the key should be displayed by the LEDs. Keycodes for all keys are given in the tables on service sheets 1 and 2. If the keycode is wrong, trace the problem back to the input of A2A1. Determine if the problem is on A2A1 or another assembly which drives A2A1. If the keycode is correct, continue with step 2.
2. Mount the A2A1 assembly on an extender board. Monitor U17 (PIA) pin 40 with a logic probe. Press a key and note the response on the logic probe. Pin 40 is the interrupt input to the PIA and normally the logic probe would show a negative going pulse coming from U12A. This pulse occurs because pin 39 of the PIA issues a reset signal to U12A when the data has been read by the processor board. If the data isn't read, U12A isn't reset and the output of U12A isn't a pulse. In this case U12A will toggle everytime a key is pressed. Thus if U12A toggles it is likely that all the circuitry driving U12A is good. If U12A stays in one state when a key is pressed, there is a problem with U12A or the circuitry driving it. If U12A toggles, then the problem is with the PIA or circuitry associated with the data bus buffers. The PIA is programmed by the processor during initialization and will not function unless this programming is accomplished. Therefore, the only way to effectively troubleshoot the PIA is to use signature analysis. The following signature analysis keycode stimulus program initializes the PIA and stimulates all modes so the problem can be found.
3. Grounding any of the inputs of the malfunction detectors (U23 and U24 on service sheet 4) should produce the corresponding code at the M inputs to U15. When the codes at the M and N inputs of U15 are different, the "M=N" output of U15 (pin 6) should be low and U6 pin 12 should be low. In normal operation the N inputs to U15 come from the PIA (U17) and are the same as the M inputs. Then the "M=N" output of U15 should be high and U6 pin 12 should be high.

Use the following signature analysis to troubleshoot if these simple checks don't uncover the problem.

Signature Analysis Set-up

1. Turn on the signal generator and wait for the STATUS light to stop indicating error code #12 (insufficient warm-up time). Disconnect the white reverse power connector cable at J1 of the A3A1 assembly (top of signal generator). Switch on the internal reference button (back panel). At this point, error code #9 should be indicated by the STATUS light.
2. Turn off the Generator. Remove all boards from the DCU section except A2A6, A2A2, and A2A1. Place A2A1 on an extender.
3. Set the Signature Analyzer pushbutton switches as follows:

SERVICE SHEET 3 (Cont'd)

START BUTTON	⎍ (OUT)
STOP BUTTON	⎍ (IN)
CLOCK BUTTON	Positive edge (⎍) or negative edge (⎍), depending on device being tested*
HOLD BUTTON	(OUT)
SELF-TEST BUTTON	(OUT)

* Explicit instructions for the position of the clock button will be provided next to the reference designator of the device being tested.

4. Connect the Signature Analyzer to the microprocessor assembly (A2A6) as follows:

Signature Analyzer	A2A6 Assembly
START LEAD	TP2 ("ST")
STOP LEAD	TP2 ("ST")
CLOCK LEAD	TP1 ("SA, CK")
GROUND LEAD	TP6 ("GND")

5. Connect a ground lead between the ground pin (near the tip of the Signature Analyzer probe) and A2A6TP6.
6. Plug the 10 pin shorting connector at the top of A2A6. Connect a jumper between A2A6TP4 and A2A6TP6 and set A2A6U5 (diagnostic routine select switch) to position 3 (between 2 and 4).
7. Remove the screws at the top and bottom front of the Signal Generator. Pull the front panel forward and down. Looking at the Signal Generator from the front, disconnect the W48 ribbon cable at the DCU Motherboard (i.e., disconnect W48 at A2A10J2). Disconnect the W49 ribbon cable (on the left) at the front panel (i.e., disconnect W49 at A1A2J1). Connect W49 at A2A10J2. This re-routes the keyboard display signals that originate at the Sweep Board, sending them back to the DCU to simulate keyboard inputs.
8. On A2A1, install jumper J1 and leave jumper J2 open. Slide the switch (A2A1S1A) to the TEST position. Turn on the Generator.

Pretest Procedure

1. Turn on the Signature Analyzer. Touch the probe to any convenient +5Vdc pin, push the RESET button on the probe and then release. The display should indicate "0000" and then "6F90". If this does not occur, go back and re-check all connections and switch positions as outlined in the preceding setup procedure. Also, the UNSTABLE SIGNATURE lamp on the Signature Analyzer should be OFF and the GATE lamp should be flashing.
2. For this test, all annunciators should be glowing dimly. The +1 digit 1 (left hand digit of the amplitude display) and HP-IB indicator lamps (2) should be on. Any other digit display is meaningless.
3. Except for the CLOCK button on the Signature Analyzer, no other button, switch or connection should be altered in the course of taking signatures on the Keycode Board (A2A1).

SERVICE SHEET 3 (Cont'd)

NOTE

In the Signature listings the reference designator for each device is followed by a + or − sign; or each pin number is preceded by a + or − sign. A + sign indicates the CLOCK button on the Signature Analyzer should be set to take signatures on the positive edge of the reference CLOCK pulse (CLOCK button OUT). A − indicates a negative or trailing edge signature reading (CLOCK button IN).

In the Signature listings some devices have a dashed line (----) substituted for the signature. The dash line indicates there is no valid Signature for that pin.

Keycode Board (P/O A2A1) Signatures

U1+	1	H65C	U5+	1	512F	U12+	1	U823	U16+	1	C244
	2	HA9C		2	56P9		2	8922		2	HPH4
	3	H65C		3	6C55		3	AA91		3	6C55
	4	47P8		4	512F		4	6F90		4	07F5
	5	U934		5	6211		5	P5C2		5	8P74
	6	H24F		6	5UAH		6	8922		6	P2P4
	7	0000		7	0000		7	0000		7	0000
	8	71CH		8	C244		8	53A5		8	U9A7
	9	3U35		9	FPU1		9	3U35		9	9537
	10	U82A		10	1025		10	6F90		10	AUH9
	11	----		11	P302		11	P557		11	F349
	12	----		12	76A6		12	U82A		12	333H
	13	----		13	U934		13	U934		13	5UAH
	14	6F90		14	6F90		14	6F90		14	6F90
			U6+	1	ACF8						
U2+	1	783H		2	3C13	U13+	1	H8UU	U17	+1	0000
	2	14AH		3	F349		2	1P41		+2	C244
	3	CAFC		4	9537		3	545F		+3	5UAH
	4	H65C		5	2C78		4	62P6		+4	6C55
	5	C60C		6	783H		5	0000		+5	8P74
	6	HA9C		7	0000		6	56P9		+6	P349
	7	0000		8	617P		7	6211		+7	9537
	8	ACF8		9	UHPP		8	0000		+8	783H
	9	F758		10	H95U		9	FPU1		+9	0000
	10	U82A		11	H5F2		10	C1FF		+10	6F90
	11	94CA		12	HP44		11	3C91		+11	6F90
	12	U934		13	P557		12	81HP		+12	6F90
	13	95A4		14	6F90		13	9C74		+13	6F90
	14	6F90					14	47P8		+14	5F3U
			U7+	1	391U		15	2C78		+15	12PU
U3+	1	F758		2	391U		16	6F90		+16	A9U4
	2	P557		3	558U					+17	U69C
	3	3C13				U14+	1	P557		18	----
	4	3C13					2	89H2		+19	HP44
	5	ACF8	U11+	1	H65C		3	H98A		+20	6F90
	6	F758		2	U934		4	9006		−21	391U
	7	0000		3	617P		5	H24F		−22	75HF
	8	CAFC		4	6F90		6	9537		−23	CUF6
	9	47P8		5	95A4		7	F349		−24	4U9H
	10	UH23		6	U934		8	0000		−25	6F90
	11	95A4		7	0000		9	8P74		−26	F36H
	12	6F90		8	A5AU		10	P173		−27	7H83
	13	U934		9	P93U		11	P302		−28	PAFU
	14	6F90		10	6F90		12	586F		−29	P703
				11	C870		13	9P36		−30	9U90
				12	A5AU		14	94CA		−31	977A
				13	B65C		15	2A66		−32	AHP8
				14	6F90		16	6F90		−33	H8AH
										−34	6F90

Left Keyboard A1A2 SERVICE SHEET 2

Keycode Board (P/O A2A1) Signatures (Cont'd)

U17	−35	1925	U20+	1	P93U	U21+	13	6F90	U25+	1	94CA
	−36	6169		2	9H33		14	UHPP		2	53A5
	−37	6C2P		3	H95U		15	617P		3	C6A2
	−38	6C2P		4	U934		16	6F90		4	----
	+39	UH23		5	53A5					5	0000
	+40	8922		6	AA91					6	6F90
				7	0000	U22+	1	H65C		7	0000
				8	C870		2	----		8	6F90
U18−	1	UU53		9	5A7A		3	----		9	0000
	2	H8AH		10	9H33		4	----		10	----
	3	969A		11	H5F2		5	H95U		11	6F90
	4	A4PB		12	5A7A		6	1025		12	0000
	5	815A		13	P93U		7	----		13	----
	6	977A		14	6F90		8	0000		14	6F90
	7	A607					9	AA91			
	8	9U90					10	----			
	9	OCP2	U21+	1	6F90		11	512F	U26−	1	558U
	10	0000		2	6F90		12	6F90		2	6F90
	11	9U90		3	6F90		13	6F90		3	969A
	12	OCP2		4	6F90		14	512F		4	6F90
	13	977A		5	0000		15	----		5	815A
	14	A607		6	6F90		16	6F90		6	6F90
	15	A4PB		7	6F90					7	A607
	16	815A		8	0000					8	6F90
	17	H8AH		9	H95U					9	OCP2
	18	969A		10	H5F2					10	0000
	19	2P05		11	H95U					11	9FCF
	20	6F90		12	6F90					12	6F90

U26−	13	AC07	U27−	14	C6M4	U28−	1	CUF6			
	14	6F90		15	FAFU		2	CUF6			
	15	C6A4		16	AC07		3	UU53			
	16	6F90		17	4C18		4	4U9H			
				18	9FCF		5	H356			
				19	08HU		6	2P05			
				20	6F90		7	0000			
U27−	1	UU53					8	UU53			
	2	P703					9	391U			
	3	9FCF					10	H356			
	4	FAFU					11	4U9H			
	5	AC07					12	CUF6			
	6	7H83					13	C6M4			
	7	C6A4					14	6F90			
	8	F36H									
	9	4C18									
	10	0000									
	11	F36H									
	12	4C18									
	13	7H83									

P/O A2A1 ASSEMBLY

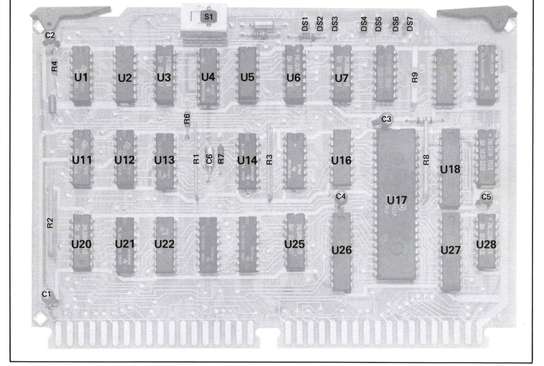


Figure 8-307. P/O A2A1 Keycode Board Component Locations

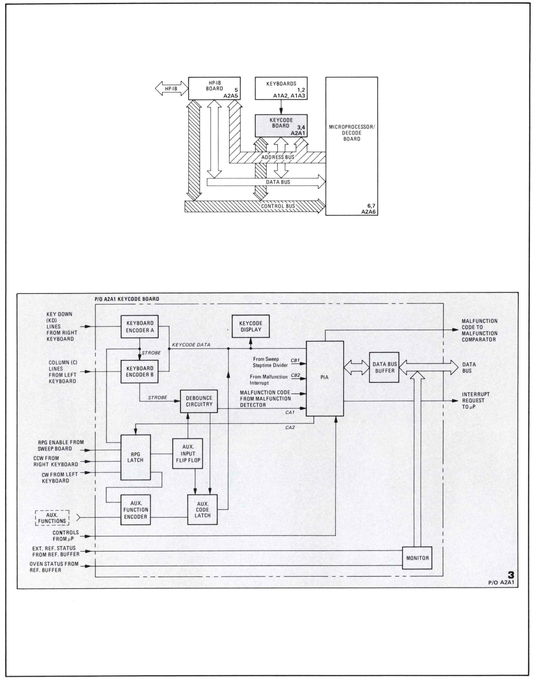
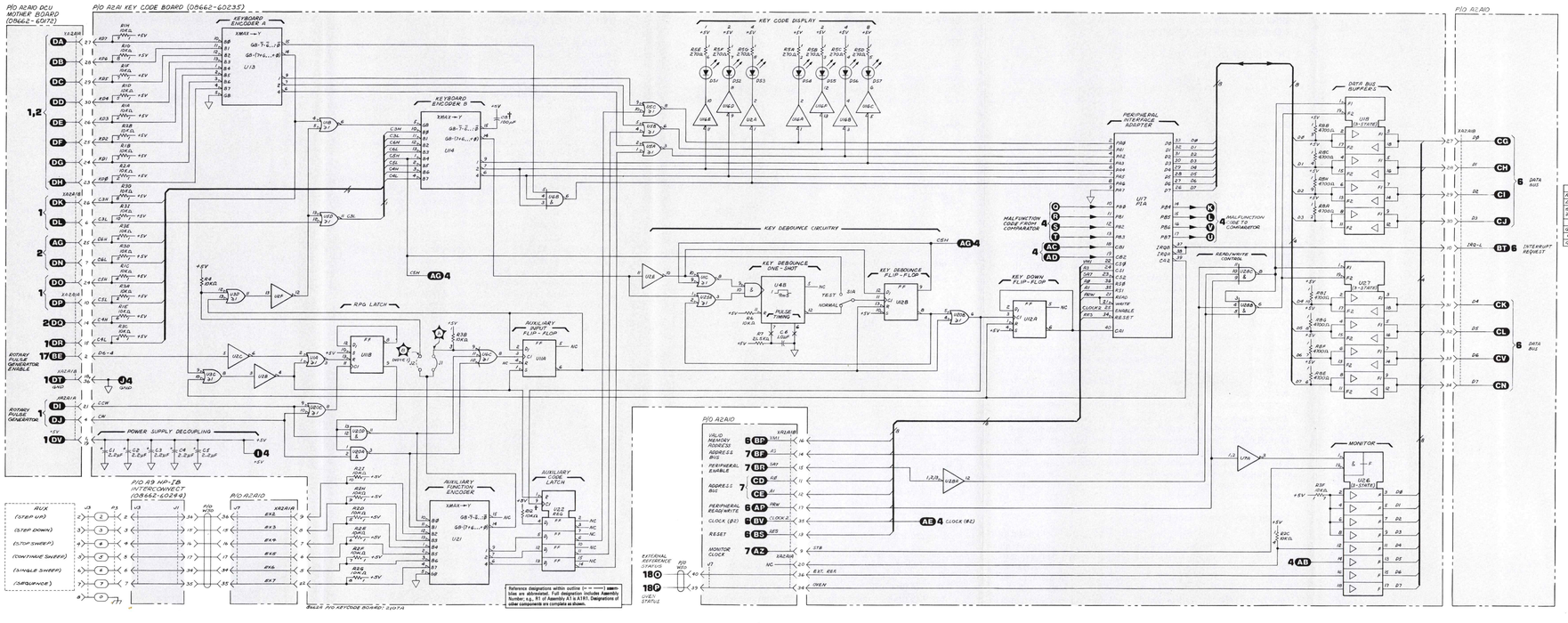


Figure 8-308. P/O A2A1 Keycode Board Block Diagrams



NOTE

1. IF THE CABLE TO THE REAR PANEL AUX CONNECTOR REQUIRES CONTACT DEBOUNCING, CONNECT JUMPER TO TEST POINT 35.

† INDICATES INFORMATION IN SECTION VIII.

REFERENCE DESIGNATIONS

NO PREFIX	A2A10
V3 W10	XA2A1A, B
A2A1	A3
C1, 6-9, CR1-7, E11-9, 11 S14 (S-7, 11-14, 16-18, 20-22, 27-34)	U1, 3

LOGIC LEVELS

LOGIC	TTL	ECL	FECL	CMOS
HIGH (1)	2V	-0.8V	-0.97V	70%VDD
LOW (0)	≤0.8V	≤-1.63V	≤-1.94V	≤0.3V

0 = EQUAL TO OR MORE NEGATIVE THAN
1 = EQUAL TO OR MORE POSITIVE THAN

INPUT	TTL	ECL	FECL	CMOS
GROUND	LOW(0)	HIGH(1)	HIGH(1)	LOW(0)
OPEN	HIGH(1)	LOW(0)	LOW(0)	A

A=GROUND→0V; X=UNDEFINED

INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
U1,2	1820-1200
U3-16	1990-1199
U3, 7, 9, 15	1820-1197
U4, 5, 8	1820-1625
U6, 28	1820-1202
U10, 12	1820-1112
U13, 14, 21	1820-1213
U17	1820-2081
U18, 27	1820-1759
U24	1820-1196
U26	1820-1756

INTEGRATED CIRCUIT VCC, VEE, AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U1-3, 7-10, 12, 14, 15, 17, 28	+5V - 14 GND - 7
U4, 13, 19, 21, 22	+5V - 16 GND - 8
U17	+5V - 40 GND - 1
U18, 24, 27	+5V - 20 GND - 10

R1-8 BOTTOM VIEW

1	2	3	4	5	6	7	8	9	10
+5V	A	B	C	D	E	F	G	H	I

R9 BOTTOM VIEW

1	2	3	4	5	6	7	8
+5V	A	B	C	D	E	F	G

3
P/O A2A1

Figure 8-309. P/O A2A1 Keycode Board Schematic

SERVICE SHEET 4
P/O A2A1 KEYCODE ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram B
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

This portion of the Keycode Board contains the malfunction detection and sweep step-time divider circuitry. The malfunction circuitry encodes error messages sent to it from throughout the instrument and generates interrupts which are sent to the microprocessor (service sheet 6). The sweep step-time divider circuitry generates signals which are sent to both the peripheral interface adapter (service sheet 3) and the Sweep D/A Board (service sheet 17).

† Malfunction Detection Circuitry

Fourteen error messages are sent to the Keycode Board from different points throughout the instrument. These error signals enter the board by way of pins 2-5, 12, 17, 20-23, 31-33, and 35, and are sent to malfunction encoders U23 and U24. Error codes generated by U23 and 24 are sent to pins 10-13 of the peripheral interface adapter (service sheet 3) and pins 10, 12, 13, and 15 of comparator U15. The code sent to the PIA is used by the microprocessor to address an error/malfunction code table in ROM.

A 4-bit code from the error code table is sent to the PIA. The PIA directs the code back to pins 9, 11, 14, and 1 of comparator U15 on the Keycode Board, where it is compared against the original malfunction code. If the two codes are not equal, the output of U15 (pin 6) goes LO, triggering the one-shot formed by U4A to produce a 190ms pulse. If the code at pins 9, 11, 14 and 1 persists for more than 190ms, an interrupt is generated at pin 12 of U6A. This interrupt is sent to the PIA.

When the microprocessor sees the interrupt, it reads the 4-bit code from the error code table and sends this code, by way of the PIA, to pins 9, 11, 14 and 1 of U15. This causes the two 4-bit codes at comparator U15 to be equal, ending stimulus to the malfunction interrupt circuitry. The microprocessor then evaluates the input code to determine what message to generate. When the code from the priority encoders changes, a new interrupt is generated, and the new code is reinterpreted through the same process.

Sweep Step-Time Divider Circuitry

Divider U8, U9, and U10 act to divide the 1.5 MHz Ø2 clock signal into three different frequencies. These frequencies are 5 kHz (200 μs period), 1 kHz (1 ms period), and 100 Hz (10 ms period). The 5 kHz is generated for use by the sweep-marker generator on the Sweep Board (service sheet 16). The 1 kHz and 100 Hz clocks are used by the microprocessor for sweep-step timing. The sweep clock select signal at pin 1 of the Keycode Board selects a 1 ms period for 0.5, 1, and 2 ms sweep-time-per-step keys, and 10 ms for the 10 ms and 100 ms keys. These two selected outputs interrupt the microprocessor through pin 18 (CB1) of the PIA when enabled under software control.

SERVICE SHEET 4 (Cont'd)

TROUBLESHOOTING

Refer to service sheet 3 for troubleshooting the Keycode Board (A2A1). After completing the procedures in service sheet 3 Signature Analysis can be used to troubleshoot the A2A1 assembly. The instructions for using this technique are given in this service sheet and service sheet 3.

Set-up

1. Turn on the signal generator and wait for the STATUS light to stop indicating error code #12 (insufficient warm-up time). Disconnect the white reverse power connector cable at J1 of the A3A1 assembly (top of signal generator). Switch on the internal reference button (back panel). At this point, error code #9 should be indicated by the STATUS light.
2. Turn off the Generator. Remove all boards from the DCU section except A2A6, A2A2, and A2A1. Place A2A1 on an extender.
3. Plug the 10 pin shorting connector at the top of A2A6. Connect a jumper between A2A6TP4 and A2A6TP6 and set A2A6U5 (diagnostic routine select switch) to position 3 (between 2 and 4).
4. Set the Signature Analyzer pushbutton switches as follows:

START BUTTON	(OUT)
STOP BUTTON	(IN)
CLOCK BUTTON	Positive edge (⌐) or negative edge (¬), depending on device being tested*
HOLD BUTTON	(OUT)
SELF-TEST BUTTON	(OUT)

* Explicit instructions for the position of the clock button will be provided next to the reference designator of the device being tested.

5. Connect the Signature Analyzer to the microprocessor assembly (A2A6) as follows:

Signature Analyzer	A2A6 Assembly
START LEAD	TP2 ("ST")
STOP LEAD	TP2 ("ST")
CLOCK LEAD	TP1 ("SA, CK")
GROUND LEAD	TP6 ("GND")

6. Connect a ground lead between the ground pin (near the tip of the Signature Analyzer probe) and A2A6TP6.
7. Remove the screws at the top and bottom front of the Signal Generator. Pull the front panel forward and down. Looking at the Signal Generator from the front, disconnect the W48 ribbon cable at the DCU Motherboard (i.e., disconnect W48 at A2A10J2). Disconnect the W49 ribbon cable (on the left) at the front panel (i.e., disconnect W49 at A1A2J1). Connect W49 at A2A10J2. This re-routes the keyboard display signals that originate at the Sweep Board, sending them back to the DCU to simulate keyboard inputs.

SERVICE SHEET 4 (Cont'd)

8. On A2A1, install jumper J1 and leave jumper J2 open. Slide the switch (A2A1S1A) to the TEST position. Turn on the Generator.

Pretest Procedure

1. Turn on the Signature Analyzer. Touch the probe to any convenient +5Vdc pin, push the RESET button on the probe and then release. The display should indicate "0000" and then "6F90". If this does not occur, go back and re-check all connections and switch positions as outlined in the preceding setup procedure. Also, the UNSTABLE SIGNATURE lamp on the Signature Analyzer should be OFF and the GATE lamp should be flashing.
2. For this test, all annunciators should be glowing dimly. The + digit (left hand digit of the amplitude display) and HP-IB indicator lamps (2) should be on. Any other digit display is meaningless.
3. Except for the CLOCK button on the Signature Analyzer, no other button, switch or connection should be altered in the course of taking signatures on the Keycode Board (A2A1).

NOTE

In the Signature listings the reference designator for each device is followed by a + or − sign; or each pin number is preceded by a + or − sign. A + sign indicates the CLOCK button on the Signature Analyzer should be set to take signatures on the positive edge of the reference CLOCK pulse (CLOCK button OUT). A − indicates a negative or trailing edge signature reading (CLOCK button IN).

In the Signature listings some devices have a dashed line (----) substituted for the signature. The dash line indicates there is no valid Signature for that pin.

SERVICE SHEET 4 (Cont'd)

Keycode Board (P/O A2A1) Signatures

U1+	1	H65C	U3+	1	F758	U15+	1	U69C	U24+	1	----
	2	HA9C		2	F557		2	0000		2	----
	3	H65C		3	3C13		3	6F90		3	----
	4	47P8		4	3C13		4	0000		4	0000
	5	U934		5	ACP8		5	----		5	0000
	6	H24F		6	F758		6	F758		6	0000
	7	0000		7	0000		7	----		7	0000
	8	71CH		8	CAPC		8	0000		8	0000
	9	3U35		9	47P8		9	5F3U		9	0000
	10	U82A		10	UH23		10	6F90		10	----
	11	----		11	95A4		11	12PU		11	----
	12	----		12	6F90		12	6F90		12	----
	13	----		13	U934		13	6F90		13	----
	14	6F90		14	6F90		14	A9U4		14	----
							15	6F90		15	6F90
							16	6F90		16	6F90
U2+	1	783H	U6+	1	ACF8						
	2	14AH		2	3C13						
	3	CAPC		3	F349	U23+	1	----	U25+	1	94CA
	4	H65C		4	9537		2	----		2	53A5
	5	C6DC		5	2C78		3	----		3	C6A2
	6	HA9C		6	783H		4	----		4	----
	7	0000		7	0000		5	----		5	0000
	8	ACP8		8	617P		6	----		6	6P90
	9	F758		9	0HPP		7	----		7	0000
	10	U82A		10	H95U		8	----		8	6P90
	11	94CA		11	H5F2		9	----		9	0000
	12	U934		12	HP44		10	----		10	----
	13	95A4		13	P557		11	----		11	6P90
	14	6F90		14	6F90		12	----		12	0000
							13	----		13	----
			U7+	1	391U		14	----		14	6P90
				2	391U		15	----			
				3	558U		16	----			

P/O Keycode Board A2A1 SERVICE SHEET 3

P/O A2A1 ASSEMBLY

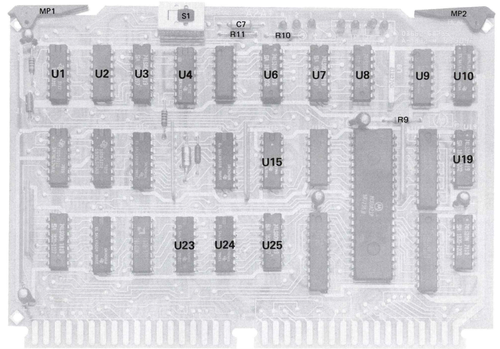


Figure 8-310. P/O A2A1 Keycode Board Component Locations

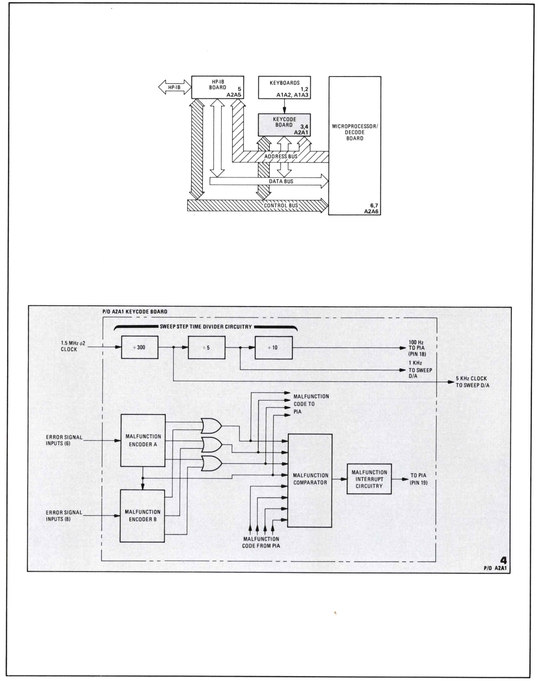
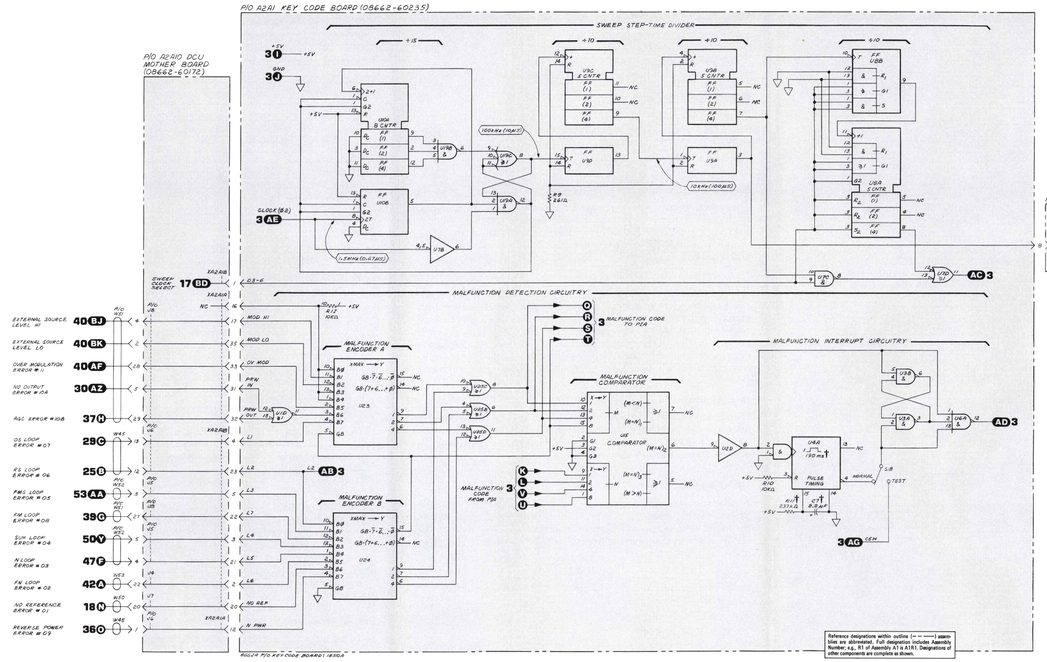


Figure 8-311. P/O A2A1 Keycode Board Block Diagrams



† BACKDATING INFORMATION IN SECTION VIII.

NOTES

REFERENCE DESIGNATIONS

NO PREFIX	A2A10
U1-U5, U6, U8-U13	U1-U8 1A2A10-U9
A2A1	
Q1 R1, 11 3-18 U1-U5, 6, 8-10, 11-13, 23-28	

LOGIC LEVELS

LOGIC	TTL	ECL	4ECL	CMOS
HIGH (1)	2.4V	-0.8 to -1.0 V	-0.81V	70% VDD
LOW (0)	0.8V	-1.6 to -1.5 V	-1.49 V	30% VDD

0 = FIGURE TO OR MORE NEGATIVE THAN
1 = FIGURE TO OR MORE POSITIVE THAN

INPUT	TTL	ECL	4ECL	CMOS
GROUND	LOW (0)	HIGH (1)	HIGH (1)	LOW (0)
OPEN	HIGH (1)	LOW (0)	LOW (0)	X

GROUND = 0V, X = UNDEFINED

INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
U1	1820-1200
U2	1820-1199
U3, 7, 15	1820-1197
U4	1820-1423
U6, 9	1820-1202
U8	1820-1201
U10	1820-1198
U13	1820-1193
U16	1820-1194
U23, 24	1820-1423

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS		
U1-3, 6-9, 10, 12, 25	+5V	—	14
	▽	—	7
U4, 5, 13, 23, 24	+5V	—	16
	▽	—	8

A1 BOTTOM VIEW

1	2	3	4	5	6	7	8	9	10
KEY	A	B	C	D	E	F	G	H	J

4
P/O A2A1

Figure 8-312. P/O A2A1 Keycode Board Schematic

SERVICE SHEET 5
A2A5 HP-IB ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram B
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The HP-IB Board interfaces the Signal Generator to the Hewlett-Packard Interface Bus, allowing the instrument to be remotely operated by an automated controller.

General Purpose Interface Adapter (GPIA)

The system microprocessor receives, processes, and sends messages to the HP-IB through U7, the general purpose interface adapter (GPIA). The GPIA handles many interface operations, including complete handshake protocol, command detection, local disabling, and serial polling.

HP-IB Transceivers

U5, U6, U8, and U9 are quad bi-directional transcievers used for matching the MOS GPIA to the 16 HP-IB bus lines. Each transceiver has back-to-back driver and receiver elements plus the required bus terminations. Direction of data flow is controlled by enabling the desired driver or receiver element. A pullup enable input at each transceiver allows selection of either an open-collector or 3-state driver mode.

Read Only Memory (ROM)

The read-only memory contains all of the software routines needed to interface the instrument to the HP-IB. The ROM on this board, although physically removed from main memory, is addressed by the microprocessor through the same address lines.

HP-IB Address Select

At the top of the HP-IB board are two BCD thumbwheel switches. These switches allow the user to set the address to which he wishes the instrument to respond when programmed remotely through the HP-IB. Address designations from 00 to 30 can be used. Any address above 30 is invalid.

NOTE

The Signal Generator is shipped with the HP-IB address select switch set at 19.

TROUBLESHOOTING

Run the HP-IB I/O check in section III. If this check fails, there is most likely a problem with the A2A5 HP-IB assembly. There are several tests which must be made to fully check the HP-IB assembly. Following is a recommended sequence for performing these tests:

SERVICE SHEET 5 (Cont'd)

† 1. Perform the ROM test by selecting special function 83. This tests ROM U11 and the associated data buffers and address decoders. Error 01 indicates U11. If the ROM test passes (00 displayed), these parts of A2A5 are normal.

2. Run the HP-IB talk-only diagnostic. Follow the instructions on service sheet B1. This diagnostic checks the HP-IB address select switch and buffer and the parts of the GPIA (U7) and HP-IB transceivers that perform the talk function. The controller diagnostic program listed on the service sheet analyzes the data that the HP-IB assembly puts on the bus.

3. Signature analysis can be used to troubleshoot with the talk-only diagnostic. If the controller diagnostic program indicates an error, follow the instructions on service sheet B1 and the signature analysis section below.

Set-up

1. Remove all boards from the DCU section except A2A6 and A2A5. Place the HP-IB board on an extender.
2. Plug the 10 pin shorting connector at the top of A2A6. Connect a jumper between A2A6TP4 and A2A6TP6 and set A2A6U5 (diagnostic routine select switch) to position 2.
3. Set the Signature Analysis pushbutton switches as follows:

START BUTTON	⎍ (OUT)
STOP BUTTON	⎍ (IN)
CLOCK BUTTON	⎍ (IN)
HOLD BUTTON	(OUT)
SELF-TEST BUTTON	(OUT)

4. Connect the Signature Analyzer to the microprocessor assembly (A2A6) as follows:

Signature Analyzer	A2A6 Assembly
START LEAD	TP2 ("ST")
STOP LEAD	TP2 ("ST")
CLOCK LEAD	TP1 ("SA, CK")
GROUND LEAD	TP6 ("GND")

5. Connect a ground lead between the ground pin (near the tip of the Signature Analyzer probe) and A2A6TP6.
6. Disconnect any devices on the HP-IB (at the rear panel connector). Set the HP-IB address switches (S1A and S1B) on the HP-IB board to 19.

Pretest Procedure

1. Turn on the Signal Generator and the Signature Analyzer. Touch the Signature Analyzer probe to any convenient +5Vdc pin, push the RESET button on the Signature Analyzer probe and then release. The Signature Analyzer display should indicate "0000" and then "H12H". If this does not occur, go back and re-check all

SERVICE SHEET 5 (Cont'd)

connections and switch positions as outlined in the preceding setup procedure. Also, the UNSTABLE SIGNATURE lamp on the Signature Analyzer should be OFF and the GATE lamp should be flashing.

2. For this test, ignore anything displayed on the front panel of the Signal Generator. Any display is meaningless.
3. No button, switch or connection should be altered in the course of taking signatures on the HP-IB Board (A2A5).

NOTE

In the Signature listings the reference designator for each device is followed by a + or − sign; or each pin number is preceded by a + or − sign. A + sign indicates the CLOCK button on the Signature Analyzer should be set to take signatures on the positive edge of the reference CLOCK pulse (CLOCK button OUT). A − indicates a negative or trailing edge signature reading (CLOCK button IN).

In the Signature listings some devices have a dashed line (----) substituted for the signature. The dash line indicates there is no valid Signature for that pin.

SERVICE SHEET 5 (Cont'd)

† HP-IB Board (A2A5) Signatures

```
U1-  1  PPC1        U4-  14 0000        U7-  17 H12H        U12- 1  6AC9
     2  H12H             15 P662             18 H12H             2  19A8
     3  H12H             16 0000             19 H12H             3  U1UH
     4  H12H             17 954H             20 H12H             4  PP7L
     5  H12H             18 H12H             21 H12H             5  H579
     6  H12H             19 58P3             22 H12H             6  7999
     7  0000             20 H12H             23 H12H             7  07F6
     8  6AC9                                 24 ----             8  7A5A
     9  58C6                                 25 PPC1             9  2P7U
     10 66U7        U5-  1  95U4             26 H12H             10 0000
     11 H12H             2  PAH3             27 95U4             11 7A5A
     12 H12H             3  PAH3             28 95U4             12 2P7U
     13 H12H             4  H12H             29 9P83             13 7999
     14 H12H             5  P7C9             30 747U             14 07F6
                         6  P7C9             31 15CH             15 PP7L
                         7  95U4             32 C00P             16 H579
U2-  1  66U7             8  0000             33 2731             17 19A8
     2  899C             9  95U4             34 0315             18 U1UH
     3  58C6             10 8315             35 P7C9             19 P322
     4  H12H             11 8315             36 PAH3             20 H12H
     5  H12H             12 H12H             37 ----
     6  899C             13 2731             38 ----        U13- 1  6AC9
     7  0000             14 2731             39 ----             2  7288
     8  58C6             15 95U4             40 2172             3  954H
     9  7945             16 H12H                                 4  F6H9
     10 2980                                 U8-  1  95U4        5  P662
     11 899C        U6-  1  0000             2  C00P             6  AF7F
     12 P322             2  H12H             3  C00P             7  2659
     13 66U7             3  H12H             4  H12H             8  CACF
     14 H12H             4  0000             5  15CH             9  0C8A
                         5  H12H             6  15CH             10 0000
U3-  1  95U4             6  H12H             7  95U4             11 CACF
     2  44H9             7  0000             8  0000             12 0C8A
     3  58C6             8  0000             9  95U4             13 AF7F
     4  899C             9  0000             10 747U             14 2659
     5  899C             10 H12H             11 747U             15 F6H9
     6  58C6             11 H12H             12 H12H             16 P662
     7  0000             12 0000             13 9P83             17 7288
     8  ----             13 H12H             14 9P83             18 954H
     9  ----             14 H12H             15 95U4             19 P322
     10 ----             15 H12H             16 H12H             20 H12H
     11 ----             16 H12H
     12 95U4                             U9-  1  44H9
     13 44H9                             2  H12H
     14 H12H        U7-  1  0000             3  H12H
                         2  0000             4  0000
U4-  1  58P3             3  58C6             5  H12H
     2  0000             4  58P3             6  H12H
     3  2P7U             5  66U7             7  44H9
     4  0000             6  0000             8  0000
     5  07F6             7  954H             9  95U4
     6  0000             8  P662             10 H12H
     7  H579             9  2659             11 H12H
     8  H12H             10 0C8A             12 H12H
     9  U1UH             11 U1UH             13 PPC1
     10 0000             12 H579             14 PPC1
     11 0C8A             13 07F6             15 95U4
     12 H12H             14 2P7U             16 H12H
     13 2659             15 ----
                         16 H12H
```

P/O Keycode Board A2A1 SERVICE SHEET 4

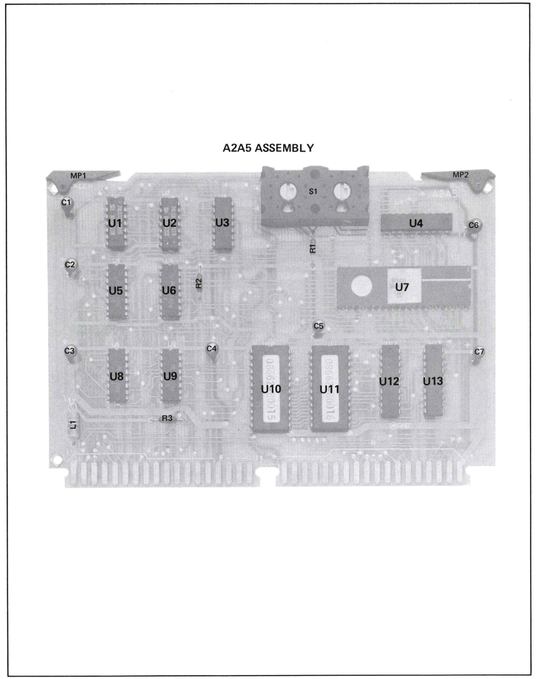
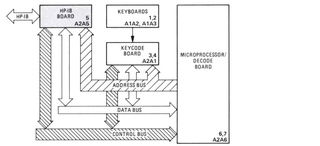


Figure 8-313. A2A5 HP-IB Board Component Locations



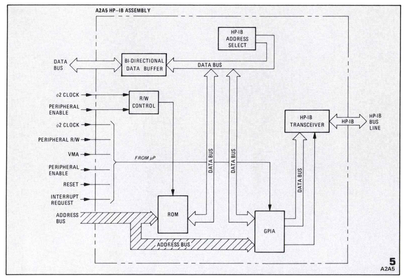
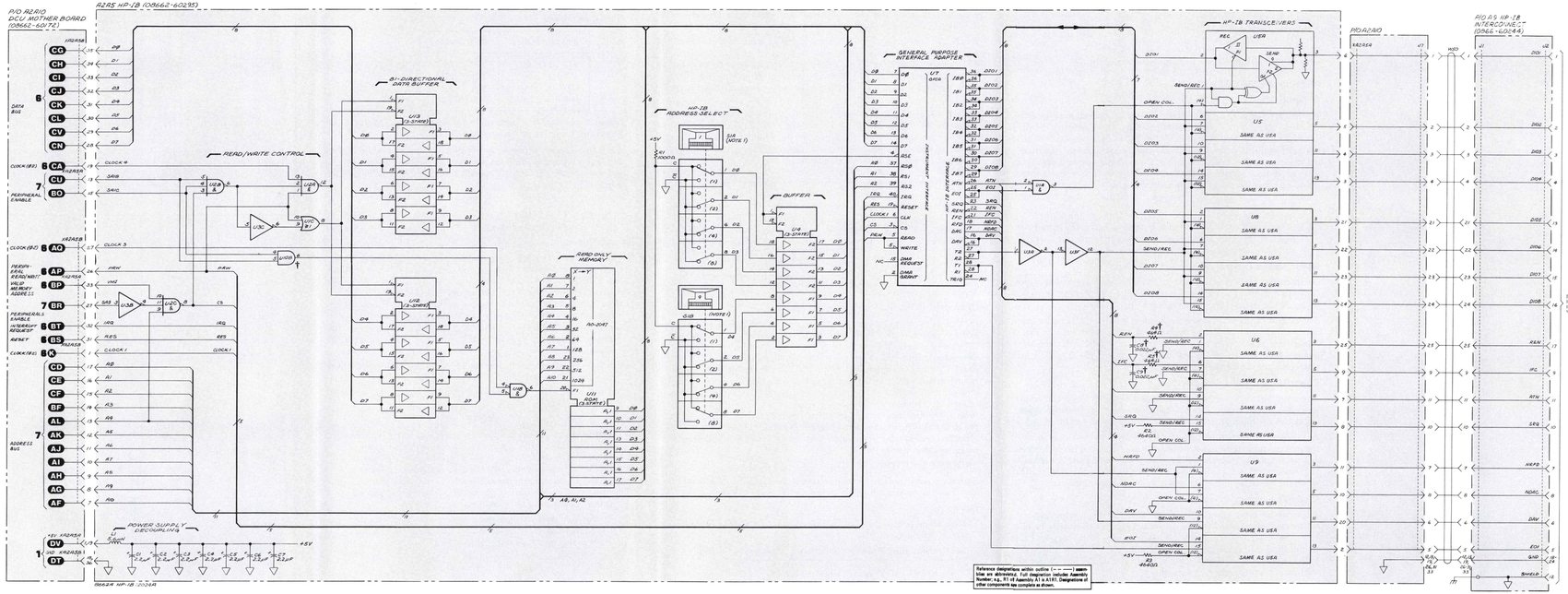


Figure 8-314. A2A5 HP-IB Block Diagrams



NOTES

1. S1/S.A THUMBWHEEL ROTARY SWITCH. THE OUTPUT OF WHICH IS A BCD EQUIVALENT OF THE SELECTED DECIMAL NUMBER.

2. ORIENTING INFORMATION IN DOTTED LINE BOX.

REFERENCE DESIGNATIONS

NO PREFIX	A2A10
W30	J1 A10A3, B
A2A5	A9
C1-9 R1 S1 R1-5 U11-13	U1,2

LOGIC LEVELS

LOGIC	TTL	ECL	PECL	CMOS
HIGH(1)	2-5V	3-4.5V	2-4.5V	70-100%
LOW(0)	0.0-.8V	1.5-2V	1.5-2.5V	0-30%
1=EQUAL TO OR MORE NEGATIVE THAN 2=EQUAL TO OR MORE POSITIVE THAN				
INPUT	TTL	ECL	PECL	CMOS
GROUND (GND)	HIGH(1)	HIGH(1)	HIGH(1)	LOW(0)
OPEN	HIGH(1)	LOW(0)	LOW(0)	A
GROUND =0V; X = UNDEFINED				

INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATION	PART NUMBER
U1	1820-2208
U2	1820-2212
U3	1820-1378
U4,12,13	1820-1378
U5,6,8,9	1820-2068
U7	1820-2511
U10	1820-2511
U11	08662-80067

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATION	PIN NUMBERS
U1-3	+5V - 14 GND - 7
U4	+5V - 20 GND - 10
U5,6,8,9	+5V - 16 GND - 8
U7	+5V - 20 GND - 1
U10	+5V - 14 GND - 7
U11	+5V - 28 GND - 14

BOTTOM VIEW

S1A S1B

1 4 2 3 5

Figure 8-315. A2A5 HP-IB Board Schematic

SERVICE SHEET 6
P/O A2A6 MICROPROCESSOR/DECODER ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram B
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The Microprocessor/Decoder Board directs the operation of the DCU which, in turn, controls the instrument. We will not go into a detailed description of the operation of the MC68A08P microprocessor chip. If more information is desired, refer to the component manufacturer's information of the chip. The bulk of the microprocessor assembly is shown on this service sheet. Service sheet 7 depicts the address decoding scheme for the hardware-select logic.

NOTE

The DCU does not monitor the RF output of the Signal Generator. The DCU only sends control signals to the signal generating (mainframe) portion of the instrument; it does not make corrections when the output is in error.

6 MHz Master Clock

Oscillator U1 is the master clock for the DCU; its frequency is crystal controlled. If this clock fails, the microprocessor will shut down due to the action of the clock-fail detector.

The output of the master system clock is 6 MHz. The master clock output is fed directly to the microprocessor, which contains a divide-by-four circuit that converts the clock frequency to 1.5 MHz. This frequency becomes the phase two (Ø2) clock, at pin 37 (E) of U13, and provides clocking for the rest of the system.

Power-up and Reset Circuitry

The reset circuitry signals the microprocessor to begin the restart sequence. A reset signal, generated during power-up of the instrument, initializes the microprocessor from the power-down condition.

At power-up, the microprocessor is not allowed to read or write until the power supply remains at +4.75 volts for at least eight clock cycles. After eight clock cycles the valid memory address (VMA) line is pulled LO, assuring that no false read or write pulses reach RAM or ROM while the memory address lines are in an undetermined state.

Clock-Fail and Power-Fail Detector

The clock-fail detector monitors the Ø2 system clock (E output at pin 37 of the microprocessor). If this clock drops out momentarily or falls below 540 kHz, a reset signal is issued. When the reset line goes LO it re-initializes the machine by directing the program counter to locations FFFE and FFFF. These locations, found in ROM, are where the initialization program is contained.

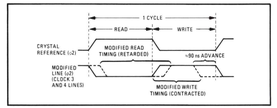
Clock Timing Shift Circuitry

The Ø2 (E) clock at the microprocessor is conditioned and modified by circuitry found on the Microprocessor Board. Timing shifts for both the "read" and "write" cycles are initiated to counteract the combined

propagation delays introduced by devices connected between the Ø2 (E) output of the Microprocessor Board and the peripheral boards.

When U13 is reading data from memory or a peripheral, the "read" portion of the Ø2 clock cycle is retarded from its reference position. This ensures that data received by the microprocessor (from other boards in the DCU) is read from the data bus while still valid. The clock is retarded through the combined propagation delay times of U9 and U10.

When the Ø2 clock is in the "write" portion of the cycle, latch U2 creates approximately 90 ns of timing advance on most Ø2 clock lines, contracting the write cycle as shown in the following figure. This advanced write pulse ensures that the memory and peripherals accept valid data from the microprocessor before the end of the Ø2 clock cycle.



Modified Ø2-Line Timing Shift

Diagnostic ROM and Routine Select Switch

ROM U6 contains diagnostic programs for troubleshooting. The address inputs to this ROM connect to the microprocessor, but the ROMs data outputs are not connected to the data bus unless a shorting connector is installed at the top of the Microprocessor Board. When ROM U6 is being used, test point 4 (TP4) on the Microprocessor Board must be grounded. Grounding this pin sets U23 and U24 in a write-only mode. The microprocessor then reads a code from the data bus which is composed of the switch settings on U5 and the lower four lines of the data bus (which are tied alternately HI and LO creating the code "5"). The diagnostic code is always 5X, where X is the switch code. The code is interpreted and used to call up one of nine diagnostic programs stored in ROM U6.

TROUBLESHOOTING

Signature Analysis can be used to troubleshoot the A2A6 assembly. The instructions for using this technique are given below.

Set-up

1. Remove all boards from the DCU section except A2A6. Place A2A6 on an extender.
2. Set the Signature Analyzer pushbutton switches as follows:

START BUTTON	(OUT)
STOP BUTTON	(IN)
CLOCK BUTTON	(IN)
HOLD BUTTON	(OUT)
SELF-TEST BUTTON	(OUT)

3. Connect the Signature Analyzer to the Microprocessor Assembly (A2A6) as follows:

Signature Analyzer	A2A6 Assembly
START LEAD	TP2 ("ST")
STOP LEAD	TP2 ("ST")
CLOCK LEAD	TP1 ("SA, CK")
GROUND LEAD	TP6 ("GND")

4. Connect a ground lead between the ground pin (near the tip of the Signature Analyzer probe) and A2A6TP6.
5. On A2A6, connect a jumper between A2A6TP4 and A2A6TP6. If the 10 pin shorting connector is plugged into the top of the Microprocessor Board, remove it. This puts the microprocessor board into a FREE RUN mode.

NOTE

In this FREE-RUN test, the diagnostic ROM (A2A6U6) itself is actually being checked.

Pretest Procedure

1. Turn on the Signal Generator and the Signature Analyzer. Touch the Signature Analyzer probe to any convenient +5 Vdc pin, push the RESET button on the Signature Analyzer probe and then release. The Signature Analyzer display should indicate "0000" and then "0001". If this does not occur, go back and re-check all connections and switch positions as outlined in the preceding setup procedure. Also, the UNSTABLE SIGNATURE lamp on the Signature Analyzer should be OFF and the GATE lamp should be flashing.
2. For this test, ignore anything displayed on the front panel of the Signal Generator. Any display is meaningless.
3. No button, switch or connection should be altered in the course of taking signatures on A2A6.

NOTE

In the Signature listings the reference designator for each device is followed by a + or − sign; or each pin number is preceeded by a + or − sign. A + indicates the CLOCK button on the Signature Analyzer should be set to take signatures on the positive edge of the reference CLOCK pulse (CLOCK button OUT). A − indicates a negative or trailing edge signature reading (CLOCK button IN).

In the Signature listings some devices have a dashed line (---) substituted for the signature. The dash line indicates there is no valid Signature for that pin.

Microprocessor Board (P/O A2A6) Signatures

U4-	1	----	U6-	5	5H21	U13-	1	----	U13-	21	0000
	2	----		6	7F7F		2	----		22	3C96
	3	8P4F		7	CCCC		3	----		23	3B27
	4	8P4U		8	5555		4	----		24	755U
	5	----		9	4CU8		5	----		25	0001
	6	----		10	233A		6	----		26	0000
	7	----		11	U995		7	----		27	0001
	8	----		12	0000		8	----		28	0000
	9	----		13	65H0		9	5555		29	0001
	10	----		14	1820		10	CCCC		30	----
	11	----		15	P2A0		11	7F7F		31	----
	12	----		16	U191		12	5H21		32	----
	13	----		17	5765		13	UAPA		33	----
	14	----		18	0000		14	UPFH		34	----
				19	0000		15	52P8		35	----
				20	----		16	HC89		36	----
U6-	1	HC89		21	0001		17	2H70		37	----
	2	52P8		22	HPP0		18	HPP0		38	----
	3	UPFH		23	2H70		19	1293		39	----
	4	UAPA		24	0001		20	HAP7		40	----

HP-IB Board A2A5 SERVICE SHEET 5

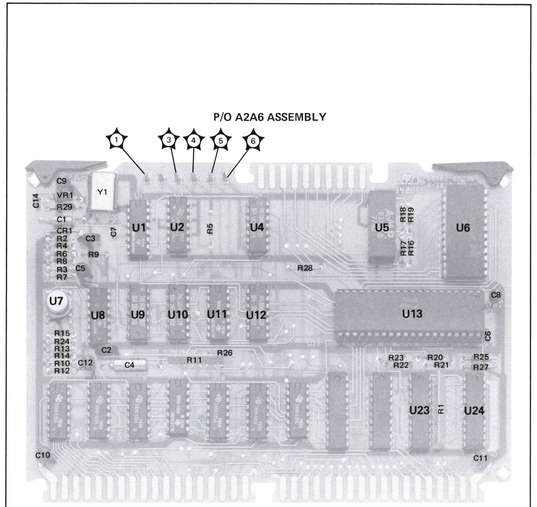
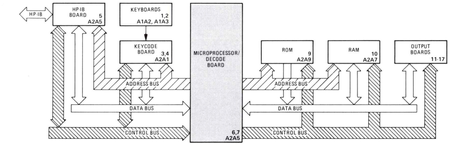


Figure 8-316. P/O A2A6 Microprocessor/Decoder Component Locations



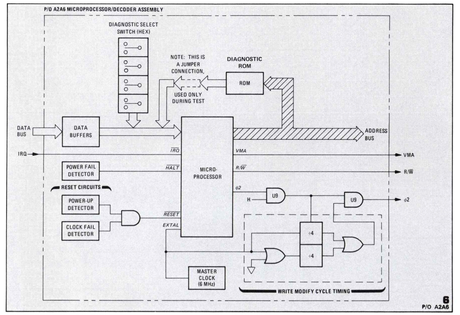
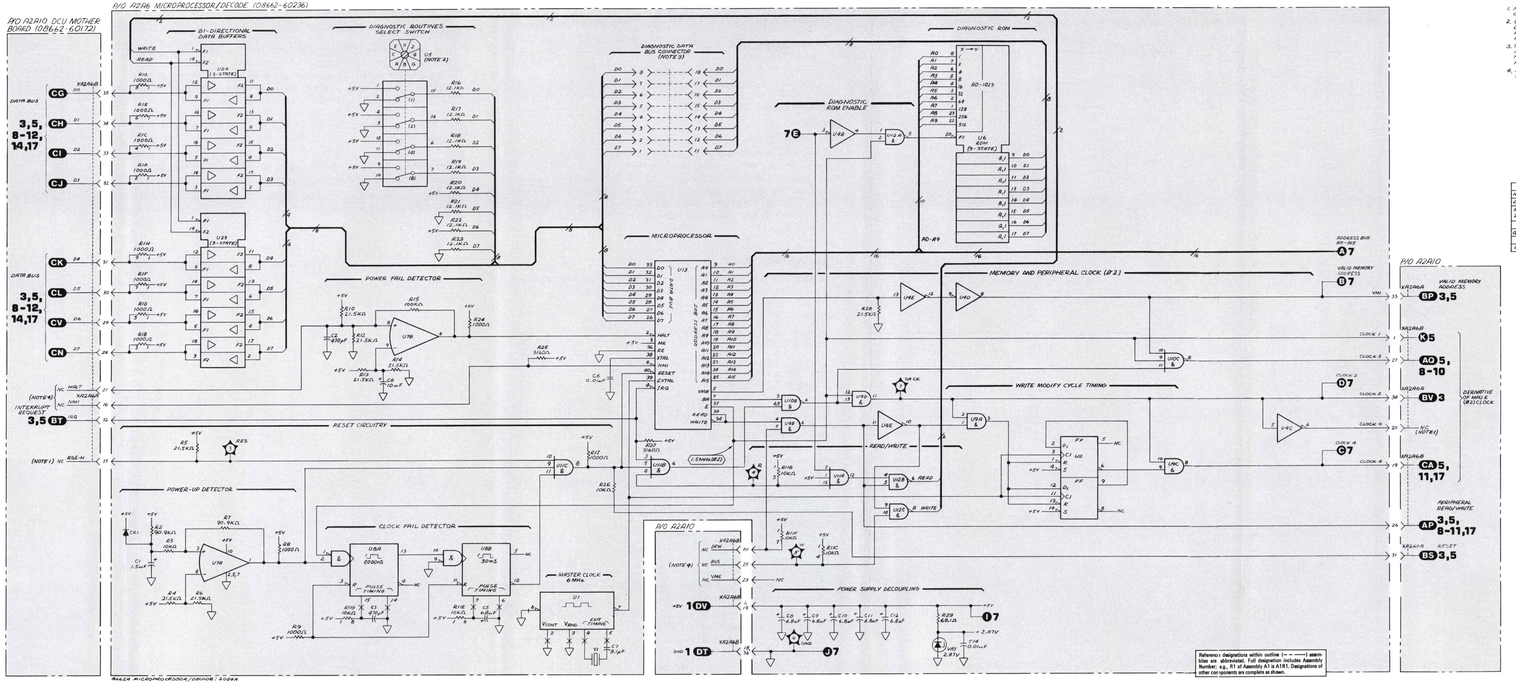


Figure 8-317. P/O A2A6 Microprocessor/Decoder Block Diagrams



NOTES

1. NON-FUNCTIONING LINE. TIEDES TERMINATE TO PANEL.
2. U7 IS A HEXADECIMAL ROTARY SWITCH. THE OUTPUT OF WHICH IS THE BINARY EQUIVALENT OF THE SELECTED HEXADECIMAL NUMBER.
3. THE DIAGNOSTIC DATA BUS CONNECTOR IS INSTALLED FOR TROUBLESHOOTING ONLY. IT IS NOT USED DURING NORMAL OPERATION IN THE SERVICE KIT.
4. NON-FUNCTIONING LINE. TRACE RUNS THROUGH MOTHERBOARD TO A2J5.

REFERENCE DESIGNATIONS

A2J4	A2J10
C1-14 CR1 R1-23 TP1,3-6 U1,2,4-13 U15,26 W1 Y1	XA2A6, 8

LOGIC LEVELS

LOGIC	TTL	ECL	ECL	CMOS
HIGH(1)	≥ 2V	≥ -1.6V	≥ -1.9V	≥ VDD
LOW(0)	≤ 0.8V	≤ -1.5V	≤ -1.9V	≤ 0.1V
X = EQUAL TO OR MORE NEGATIVE THAN 2= EQUAL TO OR MORE POSITIVE THAN				
INPUT	TTL	ECL	ECL	CMOS
GROUND	LOW(0)	HIGH(1)	HIGH(1)	LOW(0)
OPEN	HIGH(1)	LOW(0)	LOW(0)	X
GROUND = OPEN X = UNSPECIFIED				

INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
U1	1820-1824
U2	1820-1112
U3	1820-1144
U4	1820-1198
U5	1820-2086
U7	1826-0291
U8	1820-1825
U9	1820-1201
U10	1820-1202
U11	1820-1203
U12	1820-1197
U13	1820-2740
U23,24	1820-1359

NOT ASSIGNED: U3

INTEGRATED CIRCUIT POWER AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U1	+5V - 16 +5.2V - 8,9
U2,4,9-12	+5V - 28 GND - 7
U8	+5V - 40 GND - 8
U6	+5V - 28 GND - 12
U13	+8V - 8,35 GND - 1,21
U23,24	+5V - 20 GND - 10

XA1A2,8A BOTTOM VIEW

1	2	3	4	5	6	7	8	9	10
MFX	A	B	C	D	E	F	G	H	I

Figure 8-318. P/O A2A6 Microprocessor/Decoder Schematic

SERVICE SHEET 7
P/O A2A6 MICROPROCESOR/DECODER ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram B
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

This section of the Microprocessor Board decodes information on the address lines and uses it to generate register control and monitor clock signals for use at the Keycode Board, HP-IB, Readout, Level/Modulation, Frequency, and Sweep D/A Boards. The address decoders found on this service sheet are 8-to-1 demultiplexors (U14-U16, U18-U20). Lines from the decoders are sent to all DCU boards except RAM and ROM. Address lines to memory come directly from address buffers U21 and U22.

TROUBLESHOOTING

Signature Analysis can be used to troubleshoot the A2A6 assembly. The instructions for using this technique are given below.

Set-up

1. Remove all boards from the DCU section except A2A6. Place A2A6 on an extender.
2. Set the Signature Analyzer pushbutton switches as follows:

START BUTTON	(OUT)
STOP BUTTON	(IN)
CLOCK BUTTON	(IN)
HOLD BUTTON	(OUT)
SELF-TEST BUTTON	(OUT)

3. Connect the Signature Analyzer to the Microprocessor Assembly (A2A6) as follows:

Signature Analyzer	A2A6 Assembly
START LEAD	TP2 ("ST")
STOP LEAD	TP2 ("ST")
CLOCK LEAD	TP1 ("SA, CK")
GROUND LEAD	TP6 ("GND")

4. Connect a ground lead between the ground pin (near the tip of the Signature Analyzer probe) and A2A6TP6.
5. On A2A6, connect a jumper between A2A6TP4 and A2A6TP6. If the 10 pin shorting connector is plugged into the top of the Microprocessor Board, remove it. This puts the microprocessor board into a FREE RUN mode.

NOTE

In this FREE-RUN test, the diagnostic ROM (A2A6U6) itself is actually being checked.

SERVICE SHEET 7 (Cont'd)

Pretest Procedure

1. Turn on the Signal Generator and the Signature Analyzer. Touch the Signature Analyzer probe to any convenient +5 Vdc pin, push the RESET button on the Signature Analyzer probe and then release. The Signature Analyzer display should indicate "0000" and the "0001". If this does not occur, go back and re-check all connections and switch positions as outlined in the preceding setup procedure. Also, the UNSTABLE SIGNATURE lamp on the Signature Analyzer should be OFF and the GATE lamp should be flashing.
2. For this test, ignore anything displayed on the front panel of the Signal Generator. Any display is meaningless.
3. No button, switch or connection should be altered in the course of taking signatures on A2A6.

SERVICE SHEET 7 (Cont'd)

Microprocessor Board (P/O A2A6) Signatures

U14-	1	5555	U17-	1	F764	U19-	1	1293	U21-	1	0000
	2	CCCC		2	F764		2	HAP7		2	3C96
	3	7F7F		3	98HP		3	3C96		3	3C96
	4	U68U		4	P636		4	3827		4	3827
	5	2828		5	C98F		5	755U		5	3827
	6	0001		6	F764		6	0001		6	755U
	7	0851		7	0000		7	A68C		7	755U
	8	0000		8	131F		8	0000		8	0001
	9	2141		9	P6P7		9	A277		9	0001
	10	8501		10	9C99		10	9840		10	0000
	11	1400		11	6P62		11	8P4P		11	HAP7
	12	5004		12	H479		12	5P1B		12	HAP7
	13	4014		13	131F		13	2828		13	1293
	14	0054		14	0001		14	02H7		14	1293
	15	0157					15	3APF		15	HPP0
	16	0001					16	0001		16	HPP0
			U18-	1	5H21					17	2H70
				2	0AFA					18	2H70
U15-	1	5555		3	UPFH	U20-	1	52P8		19	0000
	2	CCCC		4	0000		2	HC89		20	0001
	3	7F7F		5	0000		3	2H70			
	4	U4P6		6	----		4	HPP0			
	5	2828		7	H9BA		5	3APF	U22-	1	0000
	6	0001		8	0000		6	0001		2	0AFA
	7	2205		9	1U8C		7	9947		3	0AFA
	8	0000		10	CA59		8	0000		4	UPFH
	9	8811		11	8295		9	CCU9		5	UPFH
	10	2041		12	P82H		10	94P3		6	52P8
	11	8103		13	U4P6		11	956C		7	52P8
	12	0409		14	U68U		12	64U8		8	HC89
	13	1020		15	P488		13	P074		9	HC89
	14	4084		16	0001		14	0C68		10	0000
	15	0215					15	1H3H		11	5H21
	16	0001					16	0001		12	5H21
										13	7F7F
										14	7F7F
										15	CCCC
										16	CCCC
										17	5555
										18	5555
										19	0000
										20	0001

P/O A2A6 ASSEMBLY

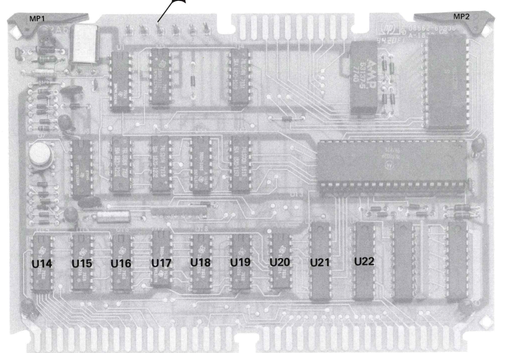
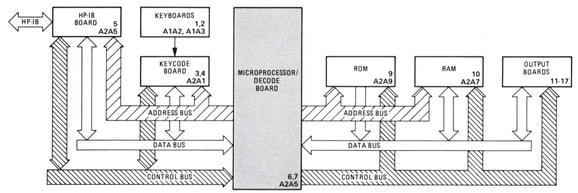


Figure 8-319. P/O A2A6 Microprocessor/Decoder Component Locations



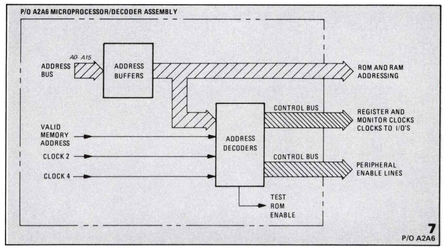
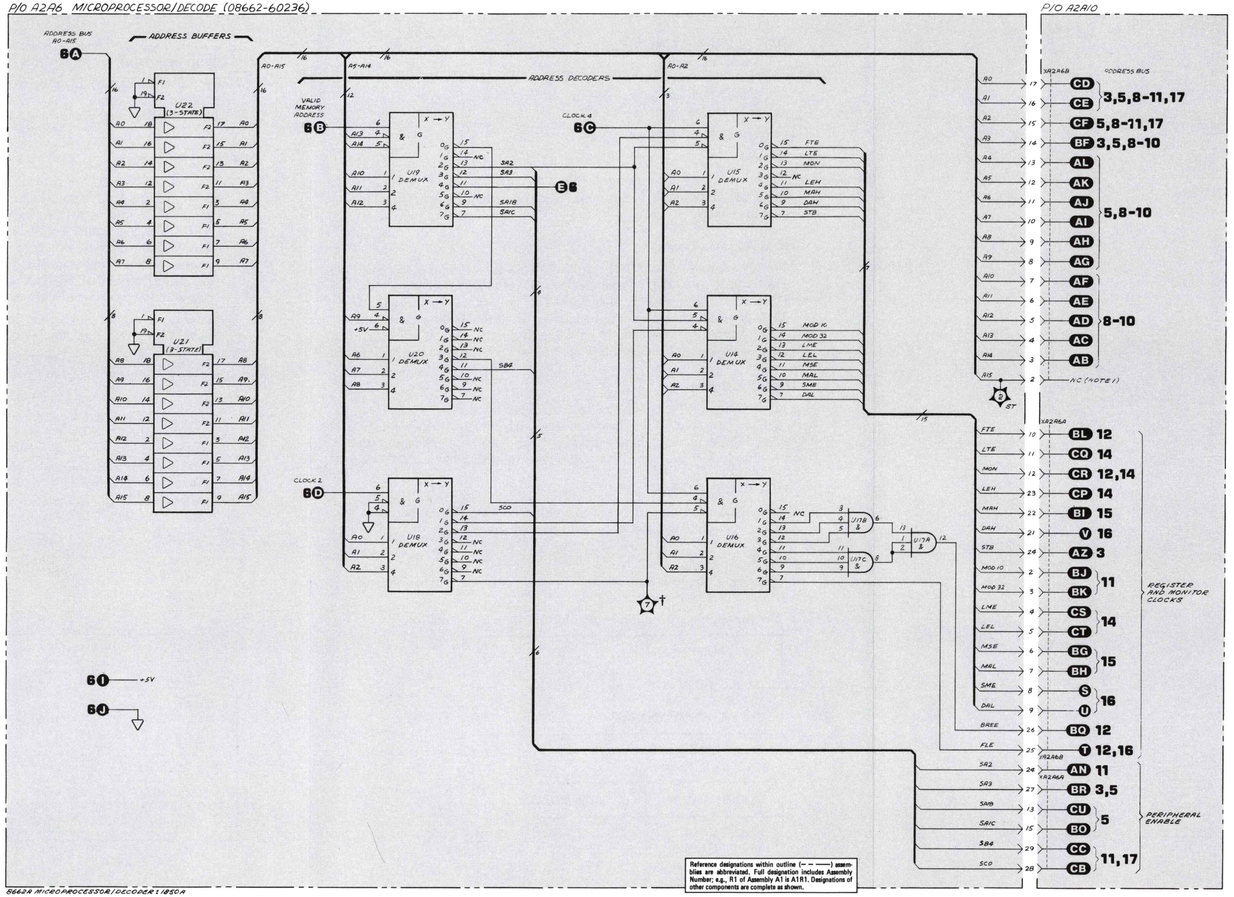


Figure 8-320. P/O A2A6 Microprocessor/Decoder Block Diagrams



NOTES

1. NON FUNCTIONING LINE. PC TRACE RUNS THROUGH A2A6 TO A2A5, A2A7, A2A8 AND A2A9.

† BACKDATING INFORMATION IN SECTION VII

REFERENCE DESIGNATIONS

	A2A6	A2A10
†	TP2, 7 U14 - 22	XA2A6A/B

LOGIC LEVELS

LOGIC	TTL	ECL	EECL	CMOS
HIGH (1)	≥ 2V	≥ -1.0V	≥ +3.7V	≥ VDD
LOW (0)	≤ 0.8V	≤ -1.5V	≤ +4.4V	≤ 0.1V
≤ = EQUAL TO OR MORE NEGATIVE THAN ≥ = EQUAL TO OR MORE POSITIVE THAN				
INPUT	TTL	ECL	EECL	CMOS
GROUND	LOW (0)	HIGH (1)	HIGH (1)	LOW (0)
OPEN	HIGH (1)	LOW (0)	LOW (0)	X
GROUND = 0V; X = UNDEFINED				

INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
U14-16, 18-20 U17 U21, 22	1820-1216 1820-1203 1820-1759

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U14-16, 18-20	+5V = 16, ▽ = 8
U17	+5V = 14, ▽ = 7
U21, 22	+5V = 20, ▽ = 10

7 P/O A2A6

Figure 8-321. P/O A2A6 Microprocessor/Decoder Schematic

SERVICE SHEET 9
A2A9 ROM 2 ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram B
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

† PRINCIPLES OF OPERATION

General

There is one read-only memory (ROM) board in the DCU. The board yields 24 kilobytes of permanent memory, enough to contain the machine control program.

ROM Address Decoding

Memory address lines A0-A10 (pins 7-17) from the microprocessor feed directly to ROMs U1-U2. Address lines A11-A14 go to decoders U14, U15 and U16. The outputs of the decoders are sent to the individual ROMs as select lines. The peripheral read/write (PRW) line enters the board at pin 26 and is used to enable and disable U14. U14 in turn controls the state of U15 and U16, as well as U17, the data bus buffer.

Data Bus Buffer

The data bus buffer is enabled and disabled by a signal from U14. When the line goes HI, the buffer is enabled and data flows from the selected ROM, through board pins 28-35, and onto the external data bus. The clock 3 line (pin 27) provides clocking for the board.

TROUBLESHOOTING

Signature Analysis can be used to troubleshoot the A2A9 assembly. The instructions for using this technique are given below.

Set-up

1. Remove all boards from the DCU section except A2A6 and A2A9. Place the A2A9 on an extender.
2. Set the Signature Analyzer pushbutton switches as follows:

START BUTTON	(OUT)
STOP BUTTON	(IN)
CLOCK BUTTON	(IN)
HOLD BUTTON	(OUT)
SELF-TEST BUTTON	(OUT)

3. Connect the Signature Analyzer to the microprocessor assembly (A2A6) as follows:

Signature Analyzer	A2A6 Assembly
START LEAD	TP2 ("ST")
STOP LEAD	TP2 ("ST")
CLOCK LEAD	TP1 ("SA, CK")
GROUND LEAD	TP6 ("GND")

SERVICE SHEET 9 (Cont'd)

4. Connect a ground lead between the ground pin (near the tip of the Signature Analyzer probe) and A2A6TP6.
5. On A2A6, connect a jumper between A2A6TP4 and A2A6TP6. If the 10 pin shorting connector is plugged into the top of A2A6, remove it. This puts the microprocessor board into a FREE RUN mode.

Pretest Procedure

1. Turn on the Signal Generator and the Signature Analyzer. Touch the Signature Analyzer probe to any convenient +5 Vdc pin, push the RESET button on the Signature Analyzer probe and then release. The Signature Analyzer should indicate "0000" and then "0001". If this does not occur, go back and re-check all connections and switch positions as outlined in the preceding setup procedure. Also, the UNSTABLE SIGNATURE lamp on the Signature Analyzer should be OFF and the GATE lamp should be flashing.
2. For this test, ignore anything displayed on the front panel of the Signal Generator. Any display is meaningless.
3. No button, switch or connection should be altered in the course of taking signatures on the ROM 2 board (A2A9).

NOTE

In the Signature listings the reference designator for each device is followed by a + or − sign; or each pin number is preceeded by a + or − sign. A + indicates the CLOCK button on the Signature Analyzer should be set to take signatures on the positive edge of the reference CLOCK pulse (CLOCK button OUT). A − indicates a negative or trailing edge signature reading (CLOCK button IN).

In the Signature listings some devices have a dashed line (----) substituted for the signature. The dash line indicates there is no valid Signature for that pin.

† ROM 2 (A2A9) Signatures

U13-		U14-		U15-		U16-	
1	----	1	3827	1	HAP7	1	HAP7
2	----	2	755U	2	3C96	2	3C96
3	----	3	0000	3	755U	3	0000
4	----	4	---	4	4H79	4	1181
5	----	5	0000	5	---	5	---
6	----	6	---	6	---	6	0001
7	0000	7	0001	7	AA6A	7	0001
8	4H79	8	0000	8	0000	8	0000
9	64HP	9	0001	9	A3UH	9	0001
10	29A6	10	0001	10	H759	10	0001
11	5FU9	11	0001	11	CA11	11	0001
12	1181	12	1181	12	546U	12	826U
13	4H79	13	64HP	13	96F8	13	603C
14	0001	14	29A6	14	57HH	14	54F5
		15	5FU8	15	CFHH	15	A711
		16	0001	16	0001	16	0001

P/O Microprocessor/Decoder A2A6 SERVICE SHEET 7

A2A9 ASSEMBLY

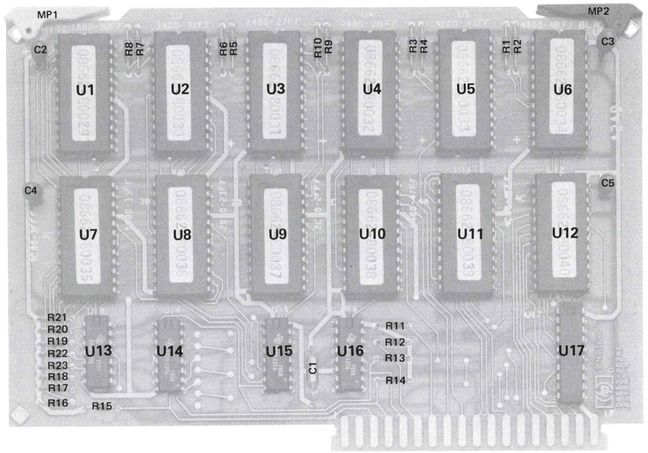
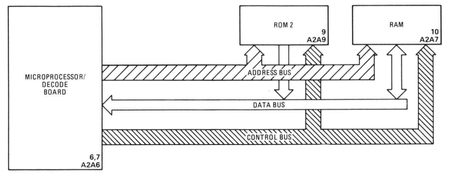


Figure 8-325. A2A9 ROM 2 Component Locations

SERVICE SHEET 8
ROM 1
A2A8

The A2A8 ROM 1 assembly exists only on instruments with serial number prefixes 2021A and below. Therefore, Service Sheet 8, with documentation for the A2A8 assembly, is in the Manual Changes — Part 2 section of this manual.



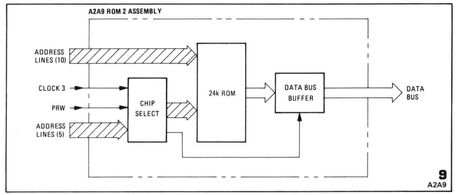
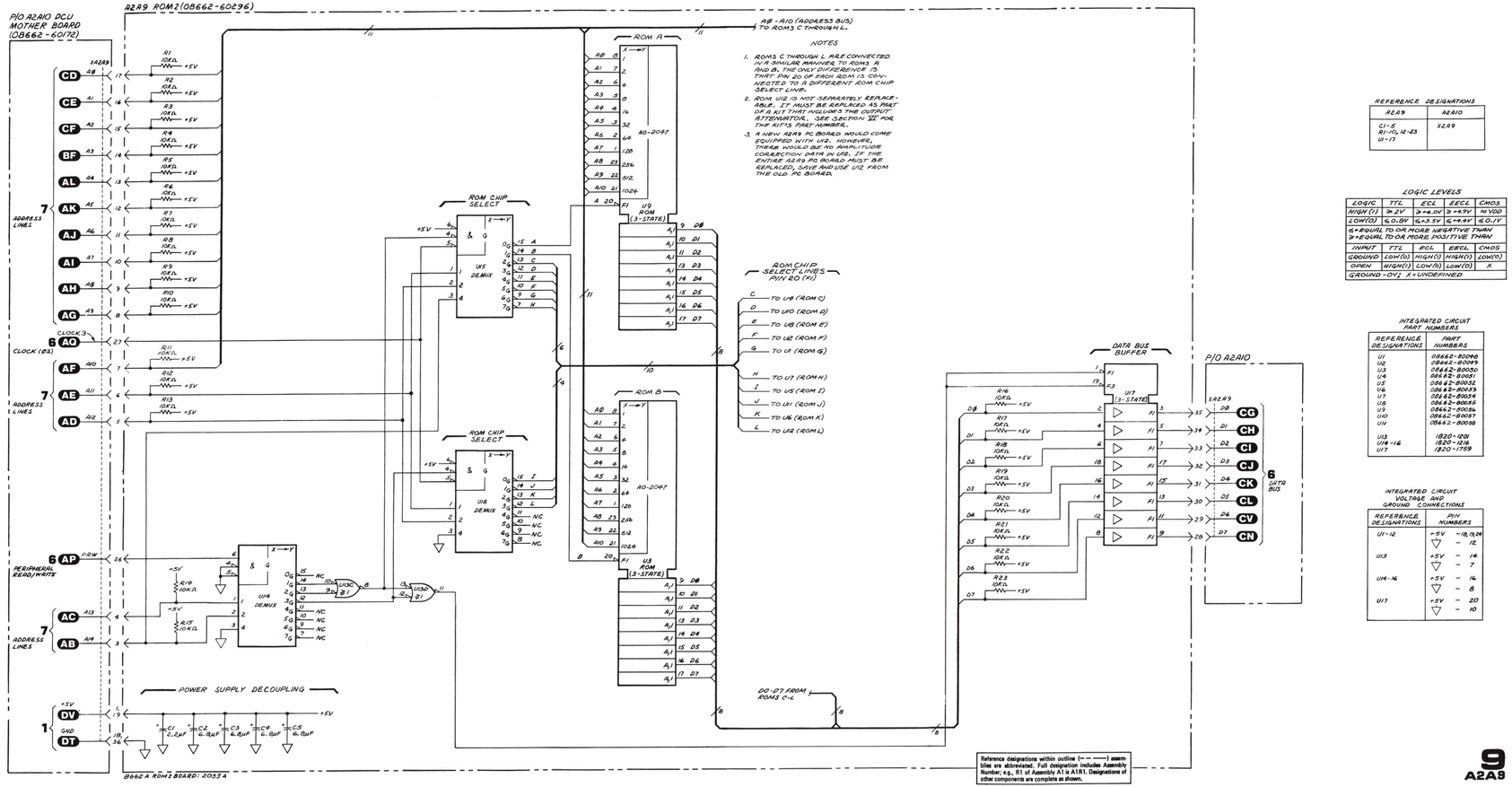


Figure 8-326. A2A9 ROM 2 Block Diagrams



REFERENCE DESIGNATIONS

A2A9	A2A10
C1-5 R1-10, 12-23 U1-17	A2A9

LOGIC LEVELS

LOGIC	TTL	ECL	EECL	CMOS
HIGH (1)	≥ 2V	≥ −1.0V	≥ −1.3V	≥ VDD
LOW (0)	≤ 0.8V	≤ −1.5V	≤ −1.6V	≤ 0.1V

≤ = EQUAL TO OR MORE NEGATIVE THAN
≥ = EQUAL TO OR MORE POSITIVE THAN

INPUT	TTL	ECL	EECL	CMOS
GROUND	LOW (0)	HIGH (1)	HIGH (1)	LOW (0)
OPEN	HIGH (1)	LOW (0)	LOW (0)	X

GROUND = 0V; X = UNDEFINED

INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
U1	08662-80098
U2	08662-80099
U3	08662-80050
U4	08662-80051
U5	08662-80052
U6	08662-80053
U7	08662-80054
U8	08662-80055
U9	08662-80056
U10	08662-80057
U11	08662-80058
U13	1820-1201
U14-16	1820-1216
U17	1820-1759

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U1-12	+5V − 18, 19 ▽ − 12
U13	+5V − 14 ▽ − 7
U14-16	+5V − 16 ▽ − 8
U17	+5V − 20 ▽ − 10

Figure 8-327. A2A9 ROM 2 Schematic

SERVICE SHEET 10
A2A7 CMOS RAM ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram B
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

† PRINCIPLES OF OPERATION

General

The CMOS RAM Board is a two kilobyte memory. The memory is organized into half-byte chunks; the most significant half-byte (MSHB) and the least significant half-byte (LSHB). Examples of MSHB RAM devices are U15, U13, U11, and U9. Examples of LSHB RAM devices are U16, U14, U12, and U10. It takes a MSHB and a LSHB to complete a data pair. For example, U15 and U16 form a data pair, as do U14 and U13.

Read/Write Control and RAM Chip Select

Signal address lines A11 through A14 are decoded to produce the read/write control signals for the bi-directional data bus and to supply a decode signal to the RAM chip select line. RAM selection is implemented by U18 and U20 or U21.

Address and Bi-Directional Data Bus Buffers

The address bus buffer, U23, is uni-directional. Address data flows onto the board through this buffer. Data bus buffer U22 is bi-directional. The direction of the data flowing through the data buffers is determined by the peripheral read/write line (PRW). When the read/write line is in the write mode, data flows onto the board from the external data bus. When the PRW is in the read mode, data flows off the board and onto the external data bus. The data bus is connected to the data bus buffer at board pins 28 through 35.

RAM Power-Up Detector and Standby Mode Switch

The power-up detector (delay) circuit is composed of C3, R7, and R8. This circuit prevents power from coming up too rapidly on the CMOS RAM Board. The standby mode switch formed by Q4, Q5, and Q6 provides gain for the power-up delay and power-fail circuitry. The RAM power supply enable/disable gate (Q3) is turned ON and OFF by the standby mode switch.

Power-Fail Detection Circuitry

The RAM power-fail detector is composed of U17 and associated circuitry. The power-fail reference circuitry is composed of C2, R4, R5, and R9. C2 acts as a noise bypass and the resistors provide a reference voltage level of .4.75 volts. Pin 6 of U17 is normally HI. When the power fails, pin 6 goes LO (at less than .4.75 volts).

Q2, Q1, R14 and R15 form the power-fail threshold latch. This latch guarantees that the collector of Q1 will be LO as long as the voltage at pin 6 of U17 remains below that of the back-up battery pack (which is about 4 volts).

SERVICE SHEET 10 (Cont'd)

Battery Back-up

The CMOS RAM power supply enable and battery charging circuit is composed of Q3 and R19. The battery is charged through R19; the collector of Q3 supplies power to the CMOS RAM as long as V_{CC} is up. When the power goes down, Q3 is effectively turned off and the back-up batteries take over, keeping the memory intact.

TROUBLESHOOTING

Signature Analysis can be used to troubleshoot the A2A7 assembly. The instructions for using this technique are given below.

Set-up

1. Remove all boards from the DCU section except A2A6 and A2A7. Place A2A7 on an extender.
2. Set the Signature Analyzer pushbutton switches as follows:

START BUTTON	(OUT)
STOP BUTTON	(IN)
CLOCK BUTTON	(IN)
HOLD BUTTON	(OUT)
SELF-TEST BUTTON	(OUT)

3. Connect the Signature Analyzer to the microprocessor assembly (A2A6) as follows:

Signature Analyzer	A2A6 Assembly
START LEAD	TP2 ("ST")
STOP LEAD	TP2 ("ST")
CLOCK LEAD	TP1 ("SA, CK")
GROUND LEAD	TP6 ("GND")

4. Connect a ground lead between the ground pin (near the tip of the Signature Analyzer probe) and A2A6TP6.
5. On A2A6, connect a jumper between A2A6TP4 and A2A6TP6. If the 10-pin shorting connector is plugged into the top of A2A6, remove it. This puts the microprocessor board into a FREE RUN mode.

Pretest Procedure

1. Turn on the Signal Generator and the Signature Analyzer. Touch the Signature Analyzer probe to any convenient +5 Vdc pin, push the RESET button on the Signature Analyzer probe and then release. The Signature Analyzer display should indicate "0000" and then "0001". If this does not occur, go back and re-check all connections and switch positions as outlined in the preceding setup procedure. Also, the UNSTABLE SIGNATURE lamp on the Signature Analyzer should be off and the GATE lamp should be flashing.

SERVICE SHEET 10 (Cont'd)

2. For this test, ignore anything displayed on the front panel of the signal generator. Any display is meaningless.
3. No button, switch or connection should be altered in the course of taking signatures on the RAM Board (A2A7).

NOTE

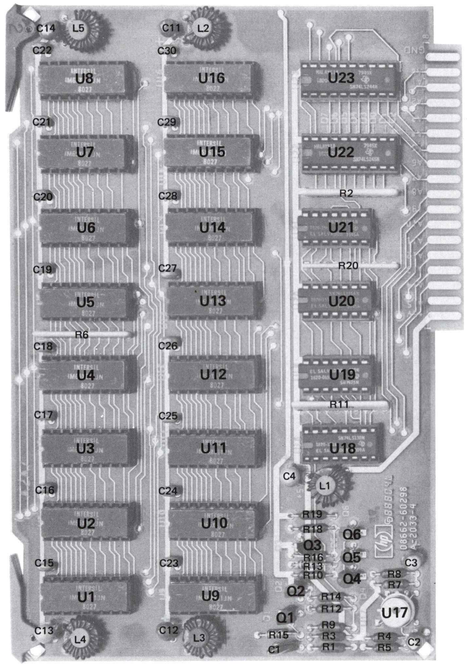
In the Signature listings the reference designator for each device is followed by a + or − sign; or each pin number is preceded by a + or − sign. A + indicates the CLOCK button on the Signature Analyzer should be set to take signatures on the positive edge of the reference CLOCK pulse (CLOCK button OUT). A − indicates a negative or trailing edge signature reading (CLOCK button IN).

In the Signature listings some devices have a dashed line (----) substituted for the signature. The dash line indicates there is no valid Signature for that pin.

† **RAM Board (A2A7) Signatures**

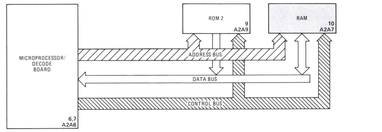
U18-		U19-		U20-		U21-		U23-	
1	2H70	1	0000	1	A756	1	7528	1	383A
2	HPP0	2	0000	2	----	2	----	2	7F7F
3	1293	3	0001	3	A756	3	7528	3	C01U
4	0000	4	0000	4	UHUF	4	2317	4	5H21
5	0000	5	383C	5	----	5	----	5	PF91
6	383C	6	383A	6	UHUF	6	2317	6	5555
7	UHUF	7	0000	7	0000	7	0000	7	3039
8	0000	8	383C	8	OP63	8	72H8	8	CCCC
9	A756	9	HAP7	9	----	9	----	9	90F5
10	7528	10	3C96	10	OP63	10	72H8	10	0000
11	2H54	11	0001	11	6541	11	2H54	11	UPFH
12	OP63	12	3827	12	----	12	----	12	9128
13	6541	13	755U	13	6541	13	2H54	13	52F8
14	2317	14	0001	14	0001	14	0001	14	3562
15	72H8							15	HC89
16	0001							16	P262
								17	OAFA
								18	CA80
								19	383A
								20	0001

A2A7 ASSEMBLY



† Figure 8-328. A2A7 RAM Component Locations

ROM 2
A2A9
SERVICE SHEET 9



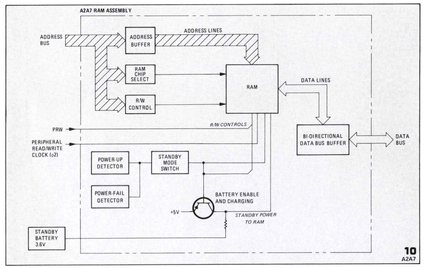
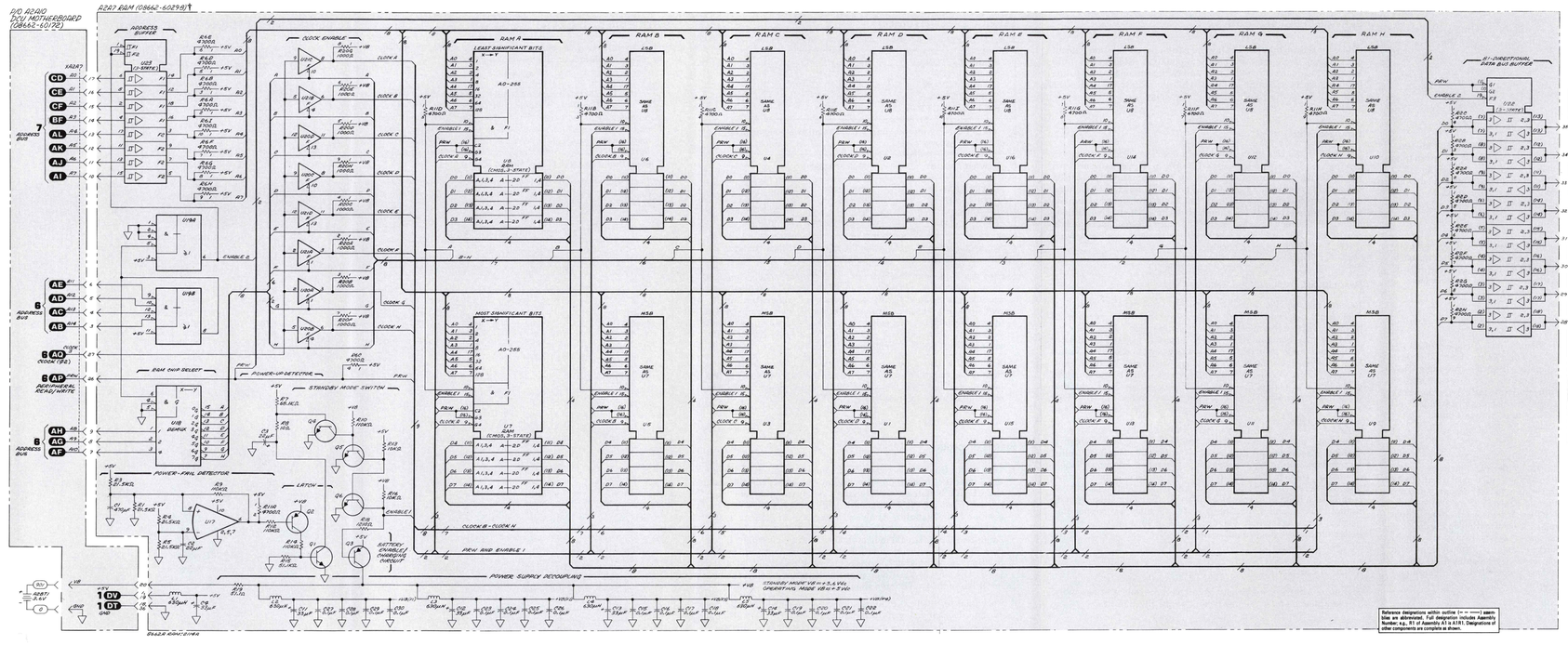


Figure 8-329. A2A7 RAM Block Diagrams



†BACKGROUND INFORMATION IN SECTION VII

REFERENCE DESIGNATIONS

A2	A2 A10
RP1	XA2A10
A2A7	
C1-9, 11-30	
J1-4	
U1-4	
U7-14, 18-20	
U1-23	

DISCRETES: C9-10, D6, D10, R17

LOGIC LEVELS

LOGIC	TTL	ECL	ECL	CMOS
HIGH (1)	≥ 2V	≥ -1.0V	≥ -4.5V	≥ VDD
LOW (0)	≤ 0.8V	≤ -1.5V	≤ -5.2V	≤ 0.1V

X = EQUAL TO OR MORE NEGATIVE THAN
≥ = EQUAL TO OR MORE POSITIVE THAN

INPUT	TTL	ECL	ECL	CMOS
GROUND (GND)	GND	HIGH (1)	HIGH (1)	GND
OPEN	HIGH (1)	LOW (0)	LOW (0)	X
(GROUND -0V)	X = UNDEFINED			

A2, A3, A5 BOTTOM VIEW

1	2	3	4	5	6	7	8	9	10
COMMON	A	B	C	D	E	F	G	H	I

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1,4-6	1854-0071
Q2,3	1853-0091
Q7,8	1853-0098
U13	1826-0361
U18	1820-1216
U19	1820-1495
U20,21	1820-1848
U22	1820-2078
U23	1820-2024

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U1-9	+VB(FS) - 18 ▽ - 8
U5-8	+VB(F4) - 18 ▽ - 8
U9-12	+VB(F2) - 18 ▽ - 8
U13-16	+VB(F1) - 18 ▽ - 8
U18	+5V - 14 ▽ - 6
U19-21	+5V - 14 ▽ - 7
U22,23	+5V - 20 ▽ - 10

Reference designations within outline (+ - - - +) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

10 A2A7

Figure 8-330. A2A7 RAM Schematic

SERVICE SHEET 11
A1A1 READOUT ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram B
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The front panel Readout Board contains the frequency, modulation level, amplitude level, and annunciator readouts. The displays (as well as the single lamp indicators) are driven from the data bus. Each individual numeric readout has its own integral storage latch and BCD decoder. Information is systematically taken off the bus, latched, and displayed. A software control program stored in ROM assures that information is properly formatted.

Data Bus Buffer

Data from the data bus enters the Readout Board through data bus buffer U25, providing information for the numeric readouts. Data enters the board as an 8-bit byte and is directed to a pair of readouts in the form of two 4-bit BCD digits. This BCD data is stored in the internal latches of the readouts for subsequent decoding and display. Data from the data bus also control the 16 individual incandescent annunciator lamps.

Frequency Readouts

There are eleven digits in the front panel frequency readout, allowing display of all frequencies, in 0.1 Hz steps, to the upper capability of 1.280 GHz. The digits are tied to the bus in groups of two (starting from the right), for a total of 5½ digit pairs. Within each grouping of two digits, the one on the right is controlled by the four least significant bits (LSB) of the 8-bit data bus; the one on the left is controlled by the four most significant bits (MSB). An example of a pair of frequency digits is U12 and U13. U3 is the only digit which is not paired; it stands alone. The least significant bits (LSB) of the data bus feed BCD information to this digit.

Frequency Display Latching

As the 8-bit BCD display information is placed on the data bus by the microprocessor, signals are generated which cause the data to be latched into the appropriate pair of digits. These latch signals come from U19, a 1-of-8 decoder. A 3-bit code is input to U19 through pins 9, 22, and 24 from the microprocessor. The output line which is stimulated (1-of-8) depends on the binary value of this 3-bit code. For instance, if a binary 4 (100) is presented at the input, output line #4 (pin 12) of U19 will go LO. By successively placing BCD information on the data bus and supplying address information to U19, all digits of the frequency display are latched and displayed. Latching progresses from the least significant digit to the most significant digit. U19 also provides latching pulses to the three digits of the level display. This display is supplied with the proper clock and readout select enable signals via readout board pins 11, 12, and 25.

Modulation and Level (Amplitude) Readouts

The BCD information for driving the modulation and level digits is taken from the 8-bit data bus in the same manner as the frequency display data. Latching for the level digits also comes from U19, except for the most significant ± 1 digit (which will be discussed later). Latching

SERVICE SHEET 11 (Cont'd)

pulses for the modulation display come from the modulation readout clock on the microprocessor board. Modulation readout clock lines enter the Readout Board via pins 13 and 26. Signals on the mod 10 line latch the two least significant digits, while the mod 32 line latches the most significant digit of the modulation display.

Lamp Registers

Latches U2 and U15 latch information from the data bus for use in driving the 16 incandescent lamps (DS3-DS18). These lamps are used behind the display window for nomenclature illumination. The outputs of U2 and U15 are connected to buffer/drivers U1 and U5. These lamp drivers deliver 90 mA to each lamp. Latching is controlled by signals from demultiplexor U20. The same address lines which drive U19 also drive U20. The register-select enable line enters the Readout Board via pin 10. U2, U15, and U26 are enabled by the peripheral read/write (PRW) line which enters the board via pin 23.

Readout and Decimal Point Register

Readout register U26 is also tied to the data bus. Its clock is derived from demultiplexor U20. U20 performs several tasks, however its primary function is control of readout display U21, which is the ± 1 indicator in the amplitude display. The latch drives this device directly without clocking. Resistors R2-R5 limit current to the LEDs within U21. The two front panel HP-IB indicators (labeled "address" and "remote") are controlled by U26. Signals from pins 6, 9, and 15 of U26 control decimal points. The right and left frequency display decimal points are controlled by signals from pins 6 and 9. Pin 15 of U26 controls the right decimal point inputs of the modulation and amplitude pairs.

A decimal point is latched when the pair of digits to which it corresponds are clocked. Placement of the decimal point is controlled by software. The program is written so that when a decimal point is desired on the left of a display pair, the left decimal point line is enabled, and when it is desired on the right, the right decimal point line is enabled. Once a line is enabled, BCD display information is put on the data bus and the appropriate pair of digits, and the corresponding decimal point, is latched. The decimal point lines must be cleared before the other digits can be latched.

TROUBLESHOOTING

Signature Analysis can be used to troubleshoot the A1A1 assembly. The instructions for using this technique are given below.

Set-up

1. Remove all boards from the DCU section except A2A6.

SERVICE SHEET 11 (Cont'd)

2. Set the Signature Analyzer pushbutton switches as follows:

START BUTTON	(OUT)
STOP BUTTON	(IN)
CLOCK BUTTON	(IN)
HOLD BUTTON	(OUT)
SELF-TEST BUTTON	(OUT)

3. Connect the Signature Analyzer to the microprocessor assembly (A2A6) as follows:

Signature Analyzer	A2A6 Assembly
START LEAD	TP2 ("ST")
STOP LEAD	TP2 ("ST")
CLOCK LEAD	TP1 ("SA, CK")
GROUND LEAD	TP6 ("GND")

4. Connect a ground lead between the ground pin (near the tip of the Signature Analyzer probe) and A2A6TP6.
5. Plug the 10-pin shorting connector at the top of A2A6. Connect a jumper between A2A6TP4 and A2A6TP6. Two different diagnostic routines are required to take a complete set of signatures of the readout board. These routines are selected by switching A2A6U5 (diagnostic routine select switch) to position 3 or position 4. Position 4 tests the digit displays; position 3 allows for checking of the annunciators, the +1 indicator, and HP-IB lamps.
6. Remove the screws (located at the top and bottom front of the Signal Generator) and pull the front panel forward and down. The back side of the front panel Readout Board is now exposed and signatures can be easily taken.

Pretest Procedure

1. Turn on the Signal Generator and the Signature Analyzer. Touch the Signature Analyzer probe to any convenient +5 Vdc pin, push the RESET button on the Signature Analyzer probe and then release. When A2A6U5 (diagnostic routine select switch) is set to position 3, the Signature Analyzer display should indicate "0000" and then "6F90". When A2A6U5 is set to position 4, the Signature Analyzer display should indicate "0000" and then "P02". If this does not occur, go back and re-check all connections and switch positions as outlined in the preceding setup procedure. Also, the UNSTABLE SIGNATURE lamp on the Signature Analzyer should be OFF and the GATE lamp should be flashing.
2. For signature test 3, all annunciators should be glowing dimly. The +1 digit (left-hand side of the amplitude display) and HP-IB indicator lamps (2) should be on. Any other digit display is meaningless. For signature test 4, all front panel digit displays (except +1 and the decimal points) should show flashing 0's. If the flashing 0's don't appear, a malfunction exists.

SERVICE SHEET 11 (Cont'd)

3. No button, switch or connection should be altered in the course of taking signatures on the Readout Board (A1A1).

NOTE

In the Signature listings the reference designator for each device is followed by a + or − sign; or each pin number is preceded by a + or − sign. A + indicates the CLOCK button on the Signature Analyzer should be set to take signatures on the positive edge of the reference CLOCK pulse (CLOCK button OUT). A − indicates a negative or trailing edge signature reading (CLOCK button IN).

In the Signature listings, some devices have a dashed line (----) substituted for the signature. The dash line indicates there is no valid Signature for that pin.

Readout Board (A1A1, Test 3) Signatures

U1-	1	----	U14-	1	----	U20-	1	6169	U25-	13	0988
	2	8826		2	7636		2	1925		14	0988
	3	U513		3	C374		3	P8U1		15	6PA2
	4	----		4	----		4	P572		16	6PA2
	5	----		5	----		5	798A		17	UA60
	6	3845		6	2C71		6	391U		18	UA60
	7	----		7	----		7	6P90		19	0000
	8	90C1		8	U3C5		8	0000		20	6P90
	9	0000		9	0000		9	6P90			
	10	----		10	----		10	6P90			
	11	9013		11	84C5		11	6P90	U26-	1	391U
	12	----		12	----		12	6P90		2	93H1
	13	6836		13	405F		13	6P90		3	0988
	14	----		14	----		14	6P90		4	H752
	15	H57P		15	395U		15	6P90		5	U059
	16	----		16	----		16	6P90		6	1445
	17	4A0U		17	U5A4					7	P0A4
	18	6P90		18	6P90					8	5C15
						U21-	1	6P90		9	A6AU
U2-	1	391U	U15-	1	391U		2	6P90		10	0000
	2	4A0U		2	U5A4		3	6P90		11	6P90
	3	H752		3	H752		4	6P90		12	226U
	4	6680		4	6680		5	6P90		13	UA60
	5	H57P		5	395U		6	0000		14	6680
	6	6836		6	C374		7	6P90		15	C63P
	7	0988		7	UA60		8	6P90		16	0069
	8	5C15		8	F14U					17	F14U
	9	90C1		9	U3C5	U25-	1	0000		18	6PA2
	10	0000		10	0000		2	5C15		19	P5U6
	11	6P90		11	6P90		3	5C15		20	6P90
	12	9013		12	84C5		4	6680			
	13	UA60		13	0988		5	6680			
	14	P0A4		14	5C15		6	P0A4			
	15	3845		15	2C71		7	P0A4			
	16	U513		16	405F		8	F14U			
	17	6PA2		17	6PA2		9	F14U			
	18	P14U		18	P0A4		10	0000			
	19	8826		19	7636		11	H752			
	20	6P90		20	6P90		12	H752			

SERVICE SHEET 11 (Cont'd)

Readout Board (A1A1, Test 4) Signatures

U3-	1	A275	U9-	1	A275	U17-	1	P14P	U24-	1	A275
	2	U373		2	U373		2	FUH8		2	U373
	3	616U		3	616U		3	14P0		3	616U
	4	----		4	----		4	----		4	----
	5	PP02		5	PP02		5	PP02		5	PP02
	6	0000		6	0000		6	0000		6	0000
	7	PP02		7	PP02		7	PP02		7	PP02
	8	F28C		8	F28C		8	U10U		8	F28C
U4-	1	P14P	U10-	1	P14P	U18-	1	A275	U25-	1	0000
	2	FUH8		2	FUH8		2	U373		2	F28C
	3	14P0		3	14P0		3	616U		3	F28C
	4	----		4	----		4	----		4	P14P
	5	PP02		5	PP02		5	PP02		5	P14P
	6	0000		6	0000		6	0000		6	A275
	7	PP02		7	PP02		7	PP02		7	A275
	8	U10U		8	U10U		8	F28C		8	616U
										9	616U
										10	0000
U5-	1	A275	U11-	1	A275	U19-	1	U923		11	FUH8
	2	U373		2	U373		2	0F9A		12	FUH8
	3	616U		3	616U		3	U7AU		13	14P0
	4	----		4	----		4	3510		14	14P0
	5	PP02		5	PP02		5	23P9		15	U373
	6	0000		6	0000		6	9214		16	U373
	7	PP02		7	PP02		7	PP02		17	U10U
	8	F28C		8	F28C		8	0000		18	U10U
							9	PP02		19	0000
							10	PP02		20	PP02
U6-	1	P14P	U12-	1	P14P		11	PP02			
	2	FUH8		2	FUH8		12	PP02			
	3	14P0		3	14P0		13	PP02			
	4	----		4	----		14	PP02			
	5	PP02		5	PP02		15	PP02			
	6	0000		6	0000		16	PP02			
	7	PP02		7	PP02						
	8	U10U		8	U10U						
						U22-	1	A275			
							2	U373			
U7-	1	A275	U13-	1	A275		3	616U			
	2	U373		2	U373		4	----			
	3	616U		3	616U		5	PP02			
	4	----		4	----		6	0000			
	5	PP02		5	PP02		7	PP02			
	6	0000		6	0000		8	F28C			
	7	PP02		7	PP02						
	8	F28C		8	F28C						
						U23-	1	P14P			
							2	FUH8			
U8-	1	P14P	U16-	1	A275		3	14P0			
	2	FUH8		2	U373		4	----			
	3	14P0		3	616U		5	PP02			
	4	----		4	----		6	0000			
	5	PP02		5	PP02		7	PP02			
	6	0000		6	0000		8	U10U			
	7	PP02		7	PP02						
	8	U10U		8	F28C						

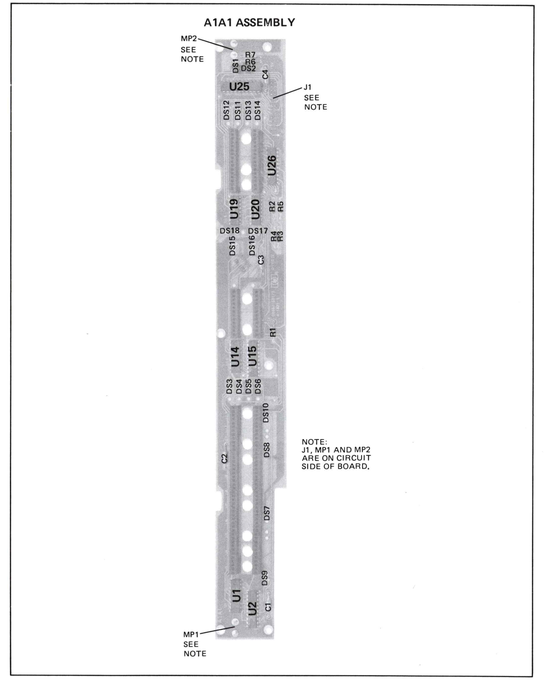
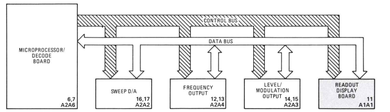


Figure 8-331. A1A1 Readout Board Component Locations



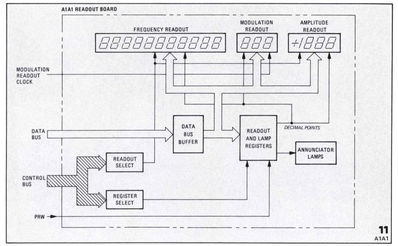


Figure 8-332. A1A1 Readout Board Block Diagrams

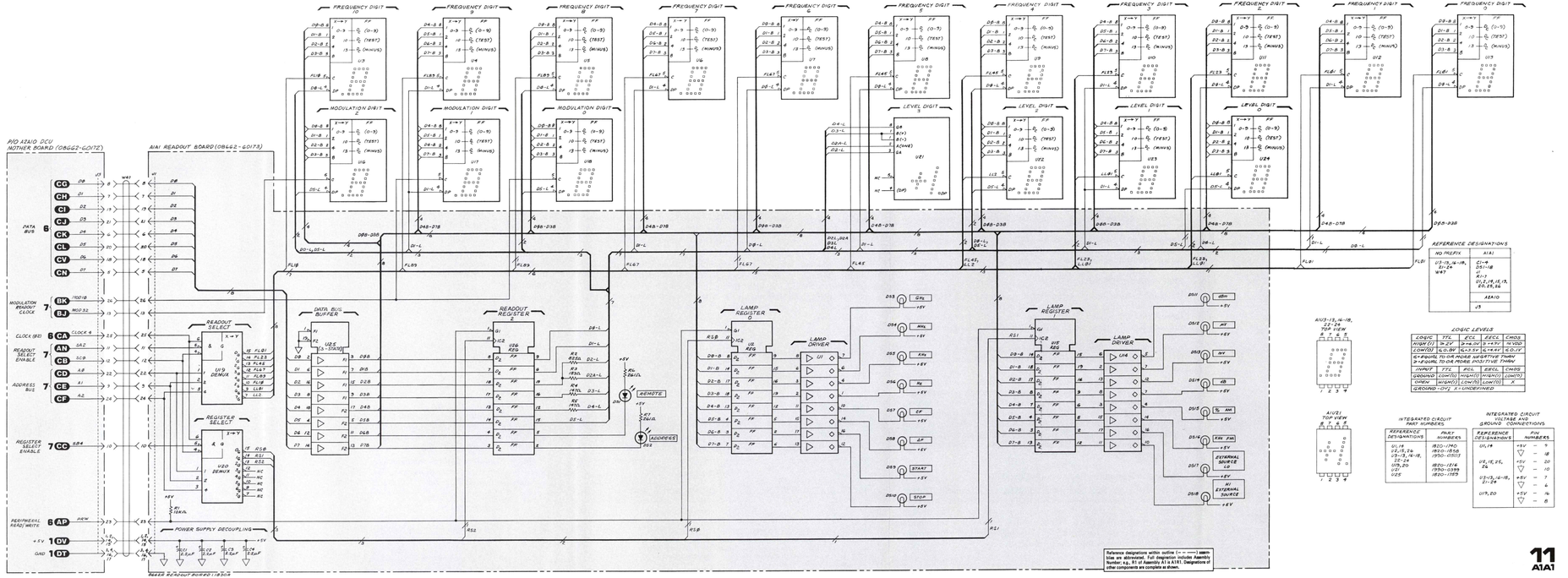


Figure 8-333. A1A1 Readout Board Schematic

SERVICE SHEET 12
P/O A2A4 FREQUENCY OUTPUT ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram B
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The Frequency Output Board latches and stores frequency and range select data. Frequency and range select data from the data bus is loaded serially into each shift register. When all shift registers are full, they are simultaneously unloaded in response to a pulse on the register clock signal line. Simultaneous clocking of this BCD information ensures that all of the phase lock loop circuits change status at the same instant. This cuts conversion time and minimizes spurious signals which occur during frequency and level shifts.

The Frequency Output Board is found on service sheets 20 and 21. Service sheet 20 contains all of the data bus input shift registers, the monitor select control and three frequency registers and their associated output monitors. Service sheet 21 contains the range select control circuitry, the BCD to binary converter and two frequency registers (and their associated monitors).

Shift Registers (DØ through D7)

Information from the data bus enters the board via pins 9 through 16 and is loaded serially into the eight 6-bit shift registers (DØ-D7). Each of these eight shift registers is associated with one bit of the 8-bit byte on the data bus. Common to the shift registers is a clock line at pin 17 (BREE). During operation, data is put on the data bus and the BREE line is pulsed LO within a half period of the system clock. Each LO to HI transition clocks one bit of information from the data bus into the shift registers.

A succession of six bytes of information from the data bus is clocked into the shift registers. Consequently, the information moves through each shift register from D-F, through D-E, D-D, D-C, and D-B to D-A. The range information is the last byte to be clocked into the shift registers and occupies the D-A outputs. All of the D-A outputs (from shift registers DØ through D7) are sent to range register U16. The D-B outputs are sent to U18, the D-C outputs to U20, and so on through the D-F outputs, which go to U17.

Range and Frequency Registers (A, E, and F)

Three of the six 8-bit storage latches on the Frequency Output Assembly are found on service sheet 12. They are U16, U17, and U18. Information from the shift registers is clocked into these storage latches by the register clock signal at pin 6. This clock is common to every latch and ensures that all the phase lock loops in the instrument are reprogrammed at the same instant.

Monitors

U7, U8, and U9 are the monitor buffers. The inputs to these monitors come from the outputs of latches U16, U17, and U18; the monitor

SERVICE SHEET 12 (Cont'd)

outputs are tied together at the data bus. U1, an 8-bit latch, selects one of the monitors, which in turn re-routes the output of its corresponding latch back to the microprocessor for self-check purposes.

Let's assume that monitor U7 (which has inputs for the 0.1 Hz and 1.0 Hz digits) is enabled to read information onto the data bus. Under program control, this information is compared to the information that was originally sent out to Frequency Register A (U16). The information should always compare. Should the program find that there is a difference, then a malfunction has occurred and the program will cause the front panel STATUS light to flash, indicating that a problem exists.

Monitor Select Latch

The 8-bit latch (U1) is used as a select device. It is controlled by software in the following manner. When the monitor routine is running, latch U1 enables one of the monitor devices. The software program then causes the chosen monitor to latch information from its respective register when the clock at pin 17 pulses LO. All of the monitor buffers are clocked, but only the enabled monitor will respond by latching data and putting it onto the data bus. Once the information is on the bus, it can be read by the microprocessor.

When the comparison sequence is complete, the program controlling the monitoring routine concludes by putting the U1 latch back into the non-select mode. That is, all of its monitors are put in a HI state again so that they are not selected. If the monitor select latch is left in the select mode it will interfere with any other device that writes onto the data bus.

TROUBLESHOOTING

Signature Analysis can be used to troubleshoot the A2A4 assembly. The instructions for using this technique are given below.

Set-up

1. Remove all boards except A2A6 and A2A4. Place A2A4 on an extender.
2. Set the Signature Analyzer pushbutton switches as follows:

START BUTTON	⎍ (OUT)
STOP BUTTON	⎎ (IN)
CLOCK BUTTON	Positive edge (⎍) or negative edge (⎎), depending on device being tested*
HOLD BUTTON	(OUT)
SELF-TEST BUTTON	(OUT)

*Explicit instructions for the position of the clock button will be provided in the table of signatures next to the reference designator of the device being tested.

3. Connect the Signature Analyzer to the microprocessor assembly (A2A6) as follows:

SERVICE SHEET 12 (Cont'd)

Signature Analyzer	A2A6 Assembly
START LEAD	TP2 ("ST")
STOP LEAD	TP2 ("ST")
CLOCK LEAD	TP1 ("SA, CK")
GROUND LEAD	TP6 ("GND")

4. Connect a ground lead between the ground pin (near the tip of the Signature Analyzer probe) and A2A6TP6.
5. Plug the 10-pin shorting connector at the top of A2A6. Connect a jumper between A2A6TP4 and A2A6TP6 and set A2A6U5 (diagnostic routine select switch) to position 4.

Pretest Procedure

1. Turn on the Signal Generator and the Signature Analyzer. Touch the Signature Analyzer probe to any convenient +5 Vdc pin, push the RESET button on the Signature Analyzer probe and then release. The Signature Analyzer display should indicate "0000" and then "PP02". If this does not occur, go back and re-check all connections and switch positions as outlined in the preceding setup procedure. Also, the UNSTABLE SIGNATURE lamp on the Signature Analyzer should be OFF and the GATE lamp should be flashing.
2. For this test, all front panel digit displays (except the +1 digit and decimal points) should show flashing 0's. If the flashing 0's don't appear, a malfunction exists.
3. Except for the clock button on the Signature Analyzer, no other button, switch, or connection should be altered in the course of taking signatures on the Frequency Output Board (A2A4).

NOTE

In the Signature listings the reference designator for each device is followed by a + or − sign; or each pin number is preceded by a + or − sign. A + indicates the CLOCK button on the Signature Analyzer should be set to take signatures on the positive edge of the reference CLOCK pulse (CLOCK button OUT). A − indicates a negative or trailing edge signature reading (CLOCK button IN).

In the Signature listings some devices have a dashed line (----) substituted for the signature. The dash line indicates there is no valid Signature for that pin.

SERVICE SHEET 12 (Cont'd)

Frequency Output Board (P/O A2A4) Signatures

U1-	1	PP02	U7	+18	00FA	U14	+7	0000	U18+	1	PP02
	2	2827		+19	PP02		+8	PP02		2	1OA0
	3	PP31		+20	PP02		+9	PP02		3	1401
	4	5301					+10	HA7C		4	H977
	5	14UP	U8	+1	A0U7		+11	195U		5	26PC
	6	4CU8		+2	1162		12	----		6	9PPA
	7	AHUP		-3	2C3U		13	----		7	H950
	8	2C3U		+4	A180		+14	PP02		8	UC17
	9	0C90		-5	AHUP					9	10H8
	10	0000		+6	CC0H	U15	- 1	2C3U		10	0000
	11	PP02		-7	5301		- 2	2C3U		11	PP02
	12	4F79		+8	898A		+3	2F4P		12	UPB3
	13	8A88		-9	PP31		+4	6UP4		13	HA7C
	14	9P4P		+10	0000		+5	U5CL		14	HAA5
	15	73P8		-11	137F		+6	520C		15	86U5
	16	2C72		+12	C99F		+7	0000		16	4F74
	17	4929		-13	4929		+8	PP02		17	89BC
	18	137F		+14	505C		+9	PP02		18	HFCP
	19	791U		-15	9P4P		+10	UC17		19	26P5
	20	PP02		+16	AH8C		+11	1307		20	PP02
				-17	8A88		12	----			
U5	- 1	137F		+18	015P		13	----	U21	- 1	AHUP
	- 2	137F		+19	PP02		+14	PP02		- 2	AHUP
	+3	339A		+20	PP02					+3	300U
	+4	C3P3								+4	65F2
	+5	0178	U9	+1	137F	U16	+ 1	PP02		+5	U137
	+6	1005		+2	1UH8		2	F127		+6	9HHP
	+7	0000		-3	2C3U		3	24P1		+7	0000
	+8	PP02		+4	9PFA		4	9485		+8	PP02
	+9	PP02		-5	AHUP		5	UFA4		+9	PP02
	+10	HFCP		+6	26FC		6	7BU4		+10	H950
	+11	AU12		-7	5301		7	CP96		+11	CP96
	12	----		+8	10A0		8	1307		12	----
	13	----		-9	PP31		9	F898		13	----
	+14	PP02		+10	0000		10	0000		+14	PP02
				-11	137F		11	PP02			
U6	- 1	4929		+12	26P5		12	00FA			
	- 2	4929		-13	4929		13	195U	U22	- 1	5301
	+3	0C79		+14	4P74		14	FH6F		- 2	5301
	+4	1P9U		-15	9P4P		15	P66C		+3	61C2
	+5	AHUF		+16	86H5		16	PC5F		+4	9152
	+6	0861		-17	8A88		17	6C8H		+5	9UU0
	+7	0000		+18	UPH3		18	AU12		+6	2H69
	+8	PP02		+19	PP02		19	0H78		+7	0000
	+9	PP02		+20	PP02		20	PP02		+8	PP02
	+10	BP8C								+9	PP02
	+11	6C8H	U13	- 1	9P4P	U17	+ 1	PP02		+10	H977
	12	----		- 2	9P4P		2	898A		+11	9485
	13	----		+3	C174		3	3158		12	----
	+14	PP02		+4	AP9A		4	61C2		13	----
U7	+1	8HL0		+5	CPA0		5	CC0H		+14	PP02
	+2	F898		+6	6173		6	A180			
	-3	2C3U		+7	0000		7	300U	U23	- 1	PP31
	+4	7NU4		+8	PP02		8	2F4P		- 2	PP31
	-5	AHUP		+9	PP02		9	1162		+3	3158
	+6	UFA4		+10	HAA5		10	0000		+4	CHUP
	-7	5301		+11	FH6F		11	PP02		+5	U520
	+8	P127		12	----		12	015P		+6	CU6A
	-9	PP31		13	----		13	2CP0		+7	0000
	+10	0000		+14	PP02		14	C174		+8	PP02
	-11	137F					15	AH8C		+9	PP02
	+12	0H78	U14	- 1	8A88		16	505C		+10	1401
	-13	4929		- 2	8A88		17	0C79		+11	24P1
	+14	FC5F		+3	2CF0		18	339A		12	----
	-15	9P4P		+4	HP7P		19	C99F		13	----
	+16	P66C		+5	HHP5		20	PP02		+14	PP02
	-17	8A88		+6	6691						

P/O A2A4 ASSEMBLY

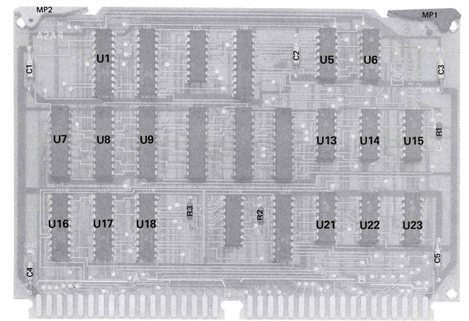
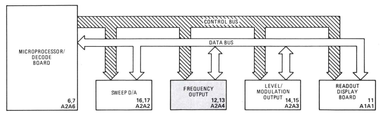


Figure 8-334. P/O A2A4 Frequency Output Board Component Locations



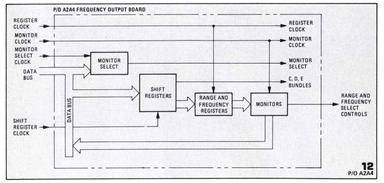
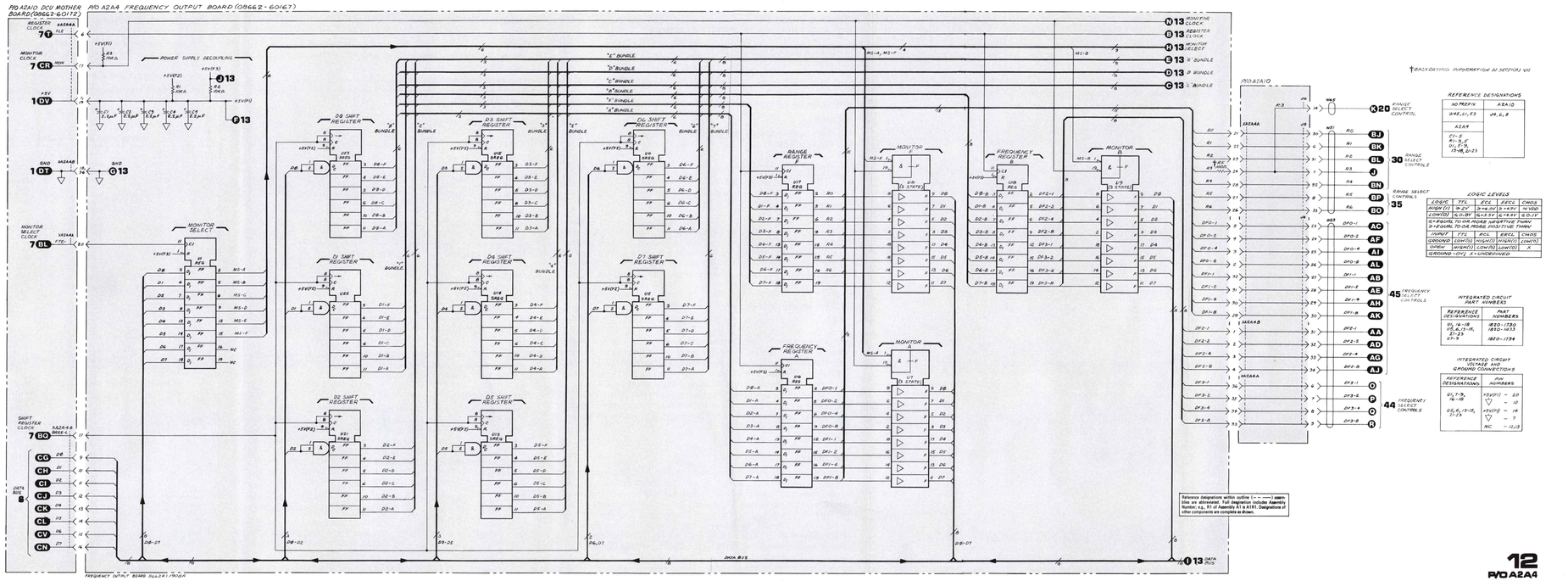


Figure 8-335. P/O A2A4 Frequency Output Board Block Diagrams



†BACKDATING INFORMATION IN SECTION VII

Figure 8-336. P/O A2A4 Frequency Output Board Schematic

SERVICE SHEET 13
P/O A2A4 FREQUENCY OUTPUT ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram B
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The Frequency Output Assembly latches and stores frequency data for the signal generating (mainframe) circuits. This assembly is shown on service sheets 12 and 13. Contained on this service sheet are the BCD to binary converters and three of the frequency registers (and their respective monitors).

Latching Resistors

Of the six 8-bit storage latches used on the Frequency Output Assembly, three are found on service sheet 13. These are U2, U4, and U20. Information from the shift registers is clocked into these latches by the register clock signal at pin 6. This clock is common to every latch and is used to clock the frequency information so that all of the phase lock loops in the instrument are reprogrammed at the same moment.

BCD-to-Binary Converters

The information which is output from service sheet 13 is only used for control of frequencies within the range of 320 MHz to 640 MHz; the range information (output from service sheet 12) is used for generating frequencies outside of this band. The frequency data taken off the data bus is stored in the register latches in the form of BCD digits. These digits span from the 0.1 Hz digit to the 100 MHz digit. The BCD information for the 1 MHz and 10 MHz digits, which comes from U2 and U4, goes to U3 and U19, the BCD-to-binary converters. The outputs of these converters are combined to produce lines which control circuits corresponding to the 1 MHz and 10 MHz digits. These lines are labeled DB7 (2, 4, 8) and DB8 (1, 2, 4).

Monitors

U10, U11, and U12 are the monitor buffers. The inputs to these buffers come from latches U2, U3, U4, U19, and U20. All monitor outputs are tied to the data bus. The monitors re-route the outputs of the frequency registers to the microprocessor so that the status of the output line can be determined. Under program control, information that is fed back is compared to the information originally sent out to the Frequency Output Board. Both should always compare. If a difference is detected, then a malfunction is indicated by the front panel STATUS light.

TROUBLESHOOTING

Signature Analysis can be used to troubleshoot the A2A4 assembly. The instructions for using this technique are given below.

SERVICE SHEET 13 (Cont'd)

Set-up

1. Remove all boards except A2A6 and A2A4. Place A2A4 on an extender.
2. Set the Signature Analyzer pushbutton switches as follows:

START BUTTON	(OUT)
STOP BUTTON	(IN)
CLOCK BUTTON	Positive edge ( ) or negative edge ( ), depending on device being tested*
HOLD BUTTON	(OUT)
SELF-TEST BUTTON	(OUT)

*Explicit instructions for the position of the clock button will be provided in the table of signatures next to the reference designator of the device being tested.

3. Connect the Signature Analyzer to the microprocessor assembly (A2A6) as follows:

Signature Analyzer	A2A6 Assembly
START LEAD	TP2 ("ST")
STOP LEAD	TP2 ("ST")
CLOCK LEAD	TP1 ("SA, CK")
GROUND LEAD	TP6 ("GND")

4. Connect a ground lead between the ground pin (near the tip of the signature analyzer probe) and A2A6TP6.
5. Plug the 10-pin shorting connector at the top of A2A6. Connect a jumper between A2A6TP4 and A2A6TP6 and set A2A6U5 (diagnostic routine select switch) to position 4.

Pretest Procedure

1. Turn on the Signal Generator and the Signature Analyzer. Touch the Signature Analyzer probe to any convenient +5 Vdc pin, push the RESET button on the Signature Analyzer probe and then release. The Signature Analyzer display should indicate "0000" and then "PP02". If this does not occur, go back and re-check all connections and switch positions as outlined in the preceding setup procedure. Also, the UNSTABLE SIGNATURE lamp on the Signature Analyzer should be OFF and the GATE lamp should be flashing.
2. For this test, all front panel digit displays (except the +1 digit and decimal points) should show flashing 0's. If the flashing 0's don't appear, a malfunction exists.
3. Except for the clock button on the Signature Analyzer, no other button, switch, or connection should be altered in the course of taking signatures on the Frequency Output Board (A2A4).

NOTE

In the Signature listings the reference designator for each device is followed by a + or − sign; or each pin number is preceded by a + or − sign. A + indicates the CLOCK button

SERVICE SHEET 13 (Cont'd)

on the Signature Analyzer should be set to take signatures on the positive edge of the reference CLOCK pulse (CLOCK button OUT). A − indicates a negative or trailing edge signature reading (CLOCK button IN).

In the Signature listings some devices have a dashed line (-···) substituted for the signature. The dash line indicates there is no valid Signature for that pin.

Frequency Output Board (P/O A2A4) Signatures

```
U2+   1  PP02      U4+   1  PP02      U11 +1  1FFC     U19+ 1 1705
      2  87A9            2  F5F7          +2  UUAH          2 FUU5
      3  U52U            3  C8UP          -3  2C3U          3  13AC
      4  9UU0            4  9152          +4  1789          4 P220
      5  FFUU            5  0F8A          -5  AHUP          5  ----
      6  1789            6  6C2P          +6  FFUU          6  ----
      7  U137            7  65F2          -7  5301          7  ----
      8  U5C1            8  6UP4          +8  87A9          8  0000
      9  UUAH            9  537U          -9  PP31          9  ----
     10  0000           10  0000         +10  0000         10  7F2C
     11  PP02           11  PP02           11  ----         11  9343
     12  6PPU           12  06U3           12  ----         12  3169
     13  HHP5           13  HP7P           13  ----         13  6C2P
     14  CPA0           14  AP9A           14  ----         14  537U
     15  FHU5           15  H574         -15  9P4P
     16  5H6U           16  ----         +16  H574
     17  AHUF           17  3P90         -17  8A88    U20+ 1  PP02
     18  0178           18  C3F3         +18  06U3         2  05UC
     19  H00C           19  ----         +19  PP02         3  CU6A
     20  PP02           20  PP02         +20  PP02         4  2H69
                                                          5  C96C
U3+   1 0832      U10 +1  CU3U     U12 +1  3FUU          6  14PP
      2 2780          +2  1705         +2  9A90          7  9HHP
      3  7F2C         -3  2C3U         -3  2C3U          8  52GC
      4  9343         +4  2780         +4  14PP          9  9A90
      5  3169         -5  AHUP         -5  AHUP         10  0000
      6  ----         +6  0832         +6  C96C         11  PP02
      7  ----         -7  5301         -7  5301         12  FC34
      8  0000         +8  6PPU         +8  05UC         13  6691
      9  ----         -9  PP31         -9  PP31         14  6173
     10  FHU5        +10  0000        +10  0000         15  CC0C
     11  5H6U        -11  137F        -11  137F         16  2843
     12  H00C        +12  0000        +12  6080         17  0861
     13  F5F7        -13  4929        -13  4929         18  1005
     14  0F6A        +14  P220        +14  2843         19  6080
                     -15  9P4P        -15  9P4P         20  PP02
                     +16  13AC        +16  CC0C
                     -17  8A88        -17  8A88
                     +18  FUU5        +18  FC34
                     +19  PP02        +19  PP02
                     +20  PP02        +20  PP02
```


P/O A2A4 ASSEMBLY

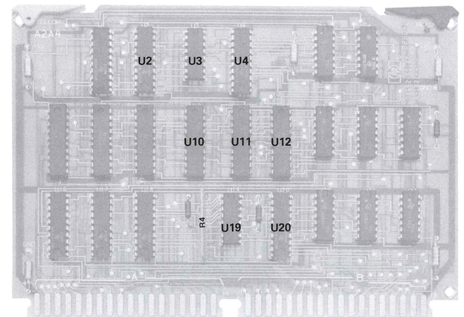
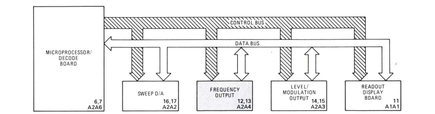


Figure 8-337. P/O A2A4 Frequency Output Board Component Locations



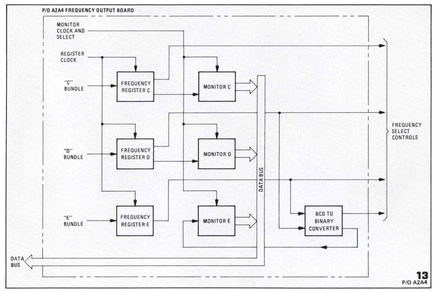
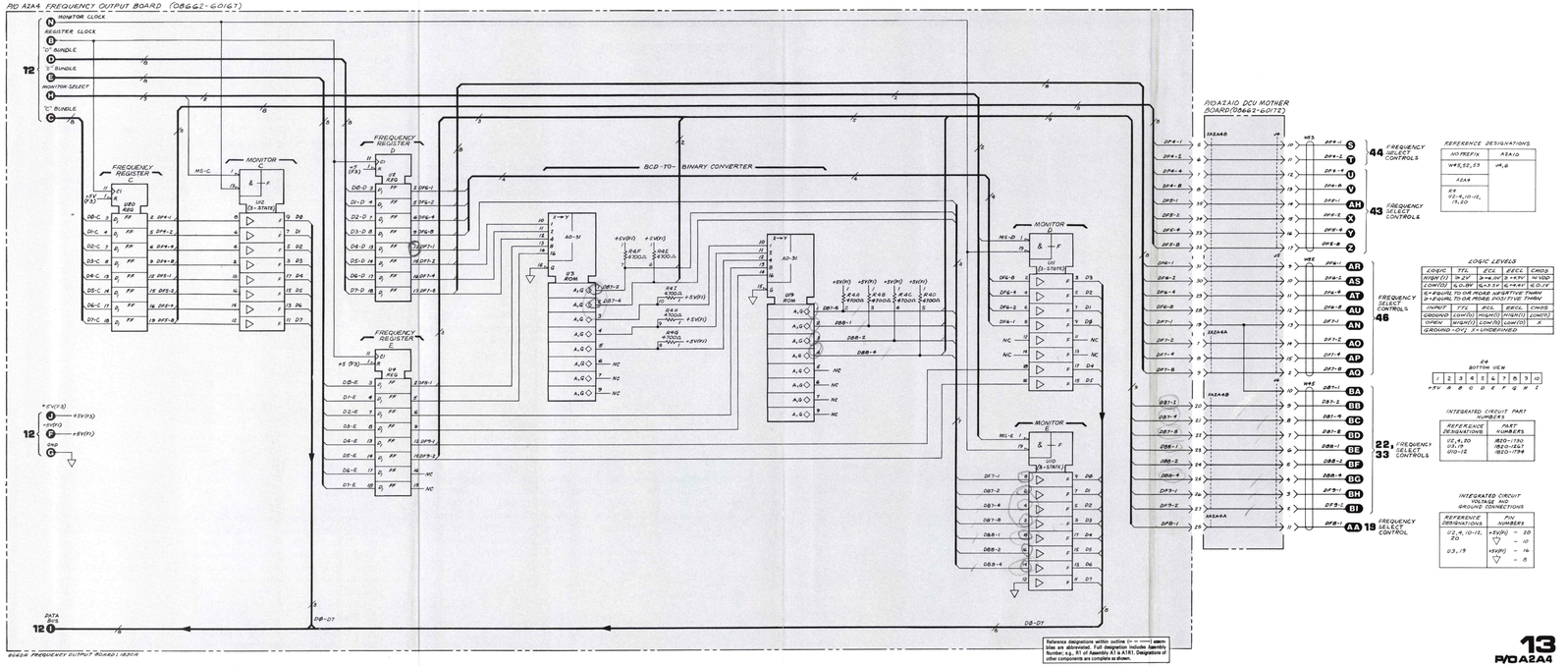


Figure 8-338. P/O A2A4 Frequency Output Board Block Diagrams



REFERENCE DESIGNATIONS

NO PREFIX	A2A10
W45,52,53	W100
A2A4	
C4 C2-9,10-12, 17,20	

LOGIC LEVELS

LOGIC	TTL	ECL	JEECL	CMOS
HIGH (1)	H ≥ 2V	H ≥ -0.8V (3 +47K)		H ≥ 0.7VDD
LOW (0)	L ≤ 0.8V	L ≤ -1.5V	(6 +47K)	L ≤ 0.3V

0 = EQUAL TO OR MORE NEGATIVE THAN -2.45VDC, TO OR MORE POSITIVE THAN -1.45VDC

INPUT	TTL	ECL	JEECL	CMOS
GROUND (0V)	LOW (0)	HIGH (1)	HIGH (1)	LOW (0)
OPEN	HIGH (1)	LOW (0)	LOW (0)	?

GROUND = 0V; X = UNDEFINED

J4 BOTTOM VIEW

1	2	3	4	5	6	7	8	9	10
+5V	A	B	C	D	E	F	G	H	I

INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
U2,4,20 U3,19 U10-12	1820-1190 1820-1621 1820-1794

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	P/O NUMBERS
U2,4,10-12, 20	+5V(P) - 20 ▽ - 10
U3,19	+5V(P) - 14 ▽ - 8

Figure 8-339. P/O A2A4 Frequency Output Board Schematic

SERVICE SHEET 14
P/O A2A3 LEVEL/MODULATION OUTPUT ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram B
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

Data for control of RF amplitude and modulation (both AM and FM) is latched on the Level/Modulation Board. Signals from this board control the output attenuator drive, RF level, amplitude modulation (AM), and FM/CW select. The monitors allow the microprocessor to perform self-checks.

This board is shown on service sheets 14 and 15. This service sheet contains the RF level circuitry.

Data Bus Buffer and Latching Registers

Data from the data bus enters the Level/Modulation Board via U8, an eight channel buffer. This buffer feeds latching registers U1 through U4. Latches U2, U3, and U4 are part of the RF level circuitry. The latches are clocked by inputs at pins A20, A21, and A22.

Monitors

At the outputs of the register latches U2, U3, and U4 are monitor circuits U9, U10, and U11. Eight-bit latch (U1) is used to select one of the monitors. The function of these monitors is to re-route the output of the latches back to the microprocessor for self-check purposes.

Let's say monitor U10 is enabled to read information from level register U3 and place this information on the data bus. The microprocessor will compare this new information to that originally sent to U3. The two should always match. If the microprocessor finds there is a difference, then a malfunction has occurred and the program will cause the front panel STATUS light to flash. A code will be generated, visible on the readout on demand, which will indicate the faulty register.

Attenuator Relay Drivers

Latch U2 drives a series of PNP transistors which in turn drive the mechanical attenuators at the RF output. The collector outputs of the transistors are clamped to ground with diodes in order to remove negative transients generated when the relays are shut off. The 10 kΩ resistors (R9 through R11 and R17 through R19) enable testing of the board when the attenuators are not being driven.

SERVICE SHEET 14 (Cont'd)

TROUBLESHOOTING

Signature Analysis can be used to troubleshoot the A2A3 assembly. The instructions for using this technique are given below.

Set-up

1. Remove all boards from the DCU section except A2A6 and A2A3. Place A2A3 on an extender.
2. Disconnect the attenuator relay drive cable (P4; service sheet 14) from the DCU Motherboard assembly at J9.
3. Set the Signature Analyzer pushbutton as follows:

START BUTTON	(OUT)
STOP BUTTON	(IN)
CLOCK BUTTON	(IN)
HOLD BUTTON	(OUT)
SELF-TEST BUTTON	(OUT)

4. Connect the Signature Analyzer to the Microprocessor assembly (A2A6) as follows:

Signature Analyzer	A2A6 Assembly
START LEAD	TP2 ("ST")
STOP LEAD	TP2 ("ST")
CLOCK LEAD	TP1 ("CA, CK")
GROUND LEAD	TP6 ("GND")

5. Connect a ground lead between the ground pin (near the tip of the Signature Analyzer probe) and A2A6TP6.
6. Plug the 10-pin shorting connector at the top of A2A6. Connect a jumper between A2A6TP4 and A2A6TP6 and set A2A6U5 (diagnostic routine select switch) to position 4.

Pretest Procedure

1. Turn on the Signal Generator and the Signature Analyzer. Touch the Signature Analyzer probe to any convenient +5 Vdc pin, push the RESET button on the Signature Analyzer probe and then release. The Signature Analyzer display should indicate "0000" and then "PP02". If this does not occur, go back and re-check all connections and switch positions as outlined in the preceding setup procedure. Also, the UNSTABLE SIGNATURE lamp on the Signature Analyzer should be OFF and the GATE lamp should be flashing.
2. For this test, all front panel digit displays (except the +1 digit and decimal points) should show flashing 0's. If the flashing 0's don't appear, a malfunction exists.
3. No button, switch or connection should be altered in the course of taking signatures on the Modulation/Level Board (A2A3).

SERVICE SHEET 14 (Cont'd.)

NOTE

In the Signature listings the reference designator for each device is followed by a + or − sign; or each pin number is preceded by a + or − sign. A + indicates the CLOCK button on the Signature Analyzer should be set to take signatures on the positive edge of the reference CLOCK pulse (CLOCK button OUT). A − indicates a negative or trailing edge signature reading (CLOCK button IN).

In the Signature listings some devices have a dashed line (----) substituted for the signature. The dash line indicates there is no valid Signature for that pin.

Modulation/Level Board (P/O A2A3) Signatures

U1-	1	PP02	U3-	1	PP02	U8-	1	0000	U10-	1	P76F
	2	P41P		2	4C3F		2	2AFH		2	4C3F
	3	2AFH		3	2AFH		3	2AFH		3	2AFH
	4	2984		4	2984		4	2984		4	60U7
	5	H746		5	60U7		5	2984		5	2984
	6	P284		6	4642		6	71AU		6	4642
	7	71AU		7	71AU		7	71AU		7	71AU
	8	1H1P		8	1H1P		8	1H1P		8	9HU6
	9	UC7P		9	9HU6		9	1H1P		9	1H1P
	10	0000		10	0000		10	0000		10	0000
	11	PP02		11	PP02		11	HPF5		11	HPF5
	12	P76F		12	71U8		12	HPF5		12	71U8
	13	HPF5		13	HPF5		13	3781		13	3781
	14	3781		14	3781		14	3781		14	P676
	15	0420		15	P676		15	018C		15	018C
	16	H46F		16	U14H		16	018C		16	U14H
	17	018C		17	018C		17	FCH0		17	FCH0
	18	FCH0		18	FCH0		18	FCH0		18	7400
	19	00CA		19	7400		19	0000		19	FP38
	20	PP02		20	PP02		20	PP02		20	PP02
U2-	1	PP02	U4-	1	PP02	U9-	1	UC7P	U11-	1	0420
	2	392C		2	A0F7		2	----		2	A0F7
	3	2AFH		3	2AFH		3	2AFH		3	2AFH
	4	2984		4	2984		4	----		4	A886
	5	392C		5	A886		5	2984		5	2984
	6	392C		6	3A07		6	----		6	3A07
	7	71AU		7	71AU		7	71AU		7	71AU
	8	1H1P		8	1H1P		8	----		8	84CP
	9	392C		9	84CP		9	1H1P		9	1H1P
	10	0000		10	0000		10	0000		10	0000
	11	PP02		11	PP02		11	HPF5		11	HPF5
	12	392C		12	7HP8		12	----		12	7HP8
	13	HPF5		13	HPF5		13	3781		13	3781
	14	3781		14	3781		14	----		14	C4A0
	15	392C		15	C4A0		15	018C		15	018C
	16	392C		16	29PA		16	392C		16	29PA
	17	018C		17	018C		17	FCH0		17	FCH0
	18	FCH0		18	FCH0		18	392C		18	0428
	19	392C		19	0428		19	FP38		19	FP38
	20	PP02		20	PP02		20	PP02		20	PP02

P/O Frequency Output Board A2A4 SERVICE SHEET 13

P/O A2A3 ASSEMBLY

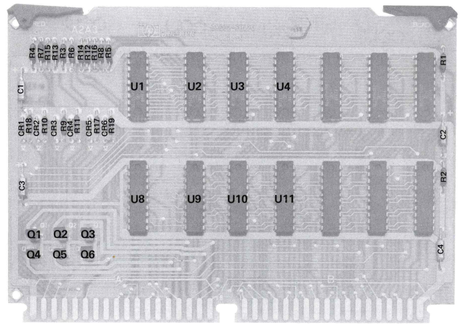


Figure 8-340. P/O A2A3 Level/Modulation Output Component Locations

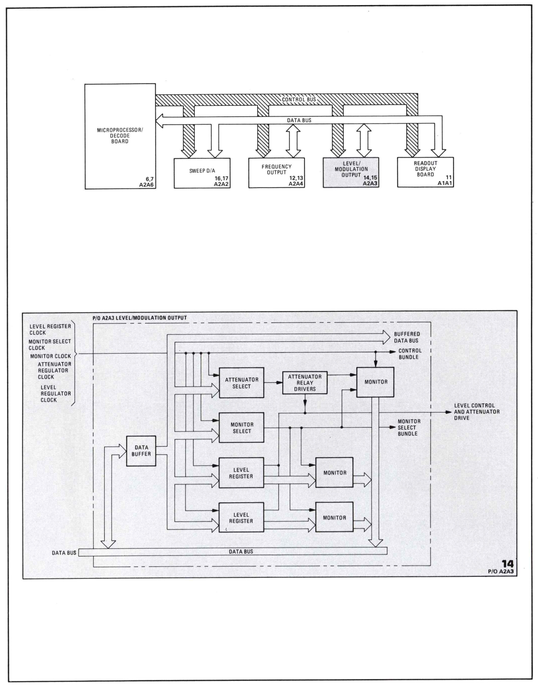
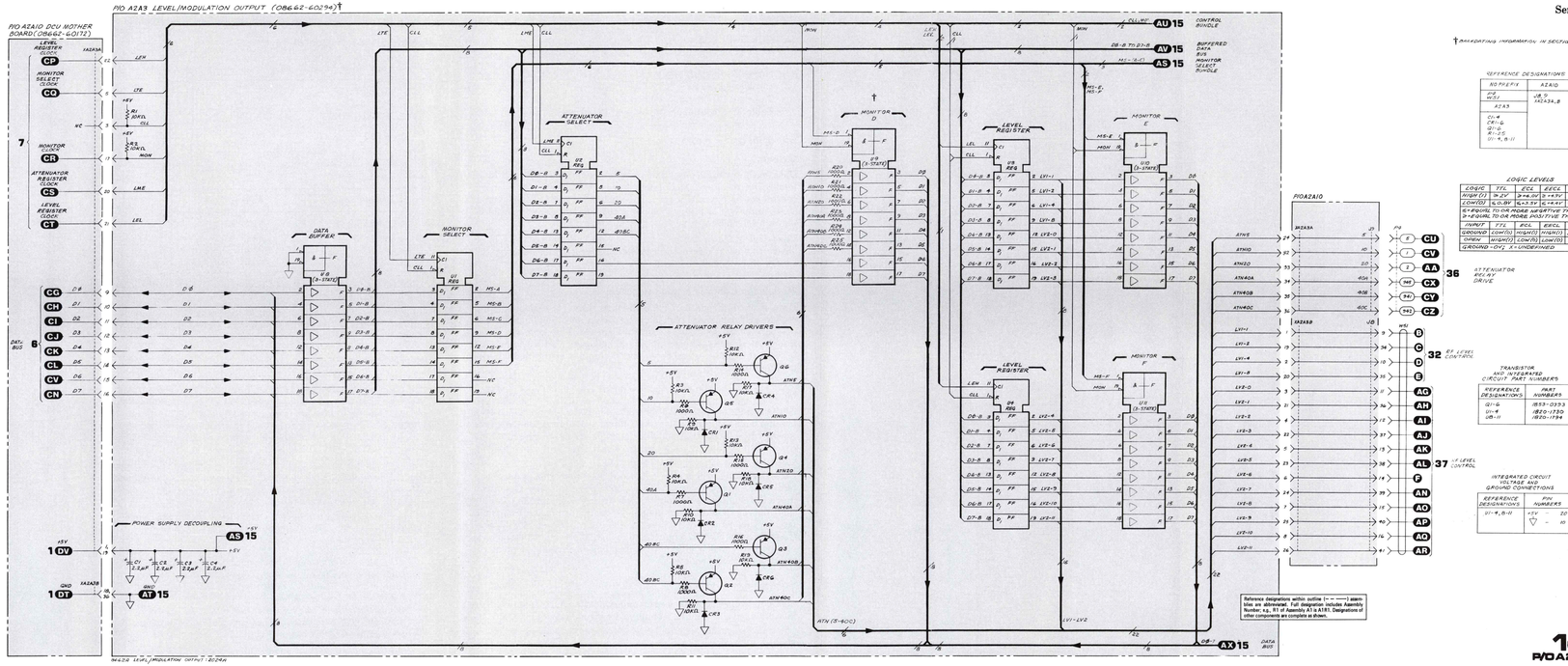


Figure 8-341. P/O A2A3 Level/Modulation Output Block Diagrams



†Annotation: Annotated information in Section VI

REFERENCE DESIGNATIONS

NO PREFIX	A2A10
-01 -M51	J8,9 TP34,35
A2A3	
C1-4 CR1-6 Q1-5 R1-25 U1-4,8,11	

LOGIC LEVELS

LOGIC	TTL	ECL	PECL	CMOS
HIGH (1)	≥ 2V	≥ -1.0V	≥ +4.1V	≥ 70%VDD
LOW (0)	≤ 0.8V	≤ -1.7V	≤ +3.4V	≤ 0.1V

0=GROUND, TTL OR CMOS NEGATIVE TRUTH
1=GROUND TTL OR CMOS POSITIVE TRUTH

INPUT	TTL	ECL	PECL	CMOS
GROUND	LOW(0)	HIGH(1)	HIGH(1)	LOW(0)
OPEN	HIGH(1)	LOW(0)	LOW(0)	X

GROUND =0V, X = UNDEFINED

ATTENUATOR REL-AT DRIVE

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1-5	1853-0353
U1-4 U8-11	1820-1320 1820-1194

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U1-4,8-11	+5V - 20 ▽ - 10

Reference designations within outline (– – – –) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A3 is A1R1. Designations of other components are complete as shown.

14
P/O A2A3

Figure 8-342. P/O A2A3 Level/Modulation Output Schematic

SERVICE SHEET 15
P/O A2A3 LEVEL/MODULATION OUTPUT ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram B
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

Data for control of RF amplitude and modulation (both AM and FM) is latched on the Level/Modulation Board. Signals from this board control the output attenuator drive, RF level, amplitude modulation (AM), and FM/CW select. The monitors allow the microprocessor to perform self-checks.

The Level/Modulation Board has been broken down into two service sheets, 14 and 15. Service sheet 14 contains the RF level circuitry, and service sheet 15 contains the level/modulation circuitry.

Modulation Control Latching Registers

Data from data bus buffer U8 (service sheet 14) enters latching registers U5, U6, and U7 (all found on service sheet 15). These latches are part of the modulation control circuitry. The program places information on the data bus and one of the registers is then stimulated to latch this information. From here the data is sent directly to the modulation section.

Monitors

At the outputs of modulation control registers U5, U6, and U7 are the monitor circuits formed by U12, U13, and U14. One monitor at a time is selected by U1, an eight-bit latch (service sheet 14). The monitors re-route the outputs of the latches back to the microprocessor for self-check purposes.

Let's say that U14 has been enabled to read data from modulation register U7 and place this information onto the data bus. The microprocessor compares this data to the data originally sent to U7. This information should always match. Should the program find a difference, then a malfunction has occurred and the program will cause the front panel STATUS light to indicate that an error exists. A code will be generated, visible on the readout on demand, which will indicate the faulty register.

TROUBLESHOOTING

Signature Analysis can be used to troubleshoot the A2A3 assembly. The instructions for using this technique are given below.

Set-up

1. Remove all boards from the DCU section except A2A6 and A2A3. Place A2A3 on an extender.
2. Disconnect the attenuator relay drive cable (P4; service sheet 14) from the DCU Motherboard assembly at J9.

SERVICE SHEET 15 (Cont'd)

3. Set the Signature Analyzer pushbutton switches as follows:

START BUTTON	(OUT)
STOP BUTTON	(IN)
CLOCK BUTTON	(IN)
HOLD BUTTON	(OUT)
SELF-TEST BUTTON	(OUT)

4. Connect the Signature Analyzer to the Microprocessor assembly (A2A6) as follows:

Signature Analyzer	A2A6 Assembly
START LEAD	TP2 ("ST")
STOP LEAD	TP2 ("ST")
CLOCK LEAD	TP1 ("CA, CK")
GROUND LEAD	TP6 ("GND")

5. Connect a ground lead between the ground pin (near the tip of the Signature Analyzer probe) and A2A6TP6.
6. Plug the 10-pin shorting connector at the top of A2A6. Connect a jumper between A2A6TP4 and A2A6TP6 and set A2A6U5 (diagnostic routine select switch) to position 4.

Pretest Procedure

1. Turn on the Signal Generator and the Signature Analyzer. Touch the Signature Analyzer probe to any convenient +5 Vdc pin, push the RESET button on the Signature Analyzer probe and then release. The Signature Analyzer should display "0000" and then "PP02". If this does not occur, go back and re-check all connections and switch positions as outlined in the preceding setup procedure. Also, the UNSTABLE SIGNATURE lamp on the Signature Analyzer should be OFF and the GATE lamp should be flashing.
2. For this test, all front panel digit displays (except the +1 digit and decimal points) should show flashing 0's. If the flashing 0's don't appear, a malfunction exists.
3. No button, switch or connection should be altered in the course of taking signatures on the Modulation/Level Board (A2A3).

NOTE

In the Signature listings the reference designator for each device is followed by a + or − sign; or each pin number is preceded by a + or − sign. A + indicates the CLOCK button on the Signature Analyzer should be set to take signatures on the positive edge of the reference CLOCK pulse (CLOCK button OUT). A − indicates a negative or trailing edge signature reading (CLOCK button IN).

In the Signature listings some devices have a dashed line (- - -) substituted for the signature. The dash line indicates there is no valid Signature for that pin.

SERVICE SHEET 15 (Cont'd)

Modulation/Level Board (P/O A2A3) Signatures

U5−	1	PP02	U7−	1	PP02	U13−	1	P41P	U6−	1	PP02
	2	7A2F		2	7455		2	U154		2	U154
	3	2AFH		3	2AFH		3	2AFH		3	2AFH
	4	2984		4	2984		4	2P6U		4	2984
	5	45UH		5	6CPH		5	2984		5	2P6U
	6	2030		6	5AF2		6	2H4A		6	2H4A
	7	71AU		7	71AU		7	71AU		7	71AU
	8	1H1P		8	1H1P		8	HF61		8	HF61
	9	5447		9	PH33		9	1H1P		9	1H1P
	10	0000		10	0000		10	0000		10	0000
	11	PP02		11	PP02		11	HPF5		11	HPF5
	12	PF76		12	7F1U		12	2604		12	26U4
	13	HPF5		13	HPF5		13	3781		13	HPF5
	14	3781		14	3781		14	5730		14	3781
	15	291A		15	488H		15	018C		15	5730
	16	1H9P		16	H323		16	FA71		16	FA71
	17	018C		17	018C		17	FCH0		17	018C
	18	FCH0		18	FCH0		18	F504		18	FCH0
	19	HFH1		19	10U9		19	PF38		19	F504
	20	PP02		20	PP02		20	PP02		20	PP02
U12−	1	P284	U14−	1	H746						
	2	7A2F		2	7455						
	3	2AFH		3	2AFH						
	4	45UH		4	6CPH						
	5	2984		5	2984						
	6	2030		6	5AF2						
	7	71AU		7	71AU						
	8	1H1P		8	PH33						
	9	HL1P		9	1H1P						
	10	0000		10	0000						
	11	HPF5		11	HPF5						
	12	PF76		12	7F1U						
	13	3781		13	3781						
	14	291A		14	488H						
	15	016C		15	016C						
	16	1H9P		16	H323						
	17	FCH0		17	FCH0						
	18	HFH1		18	10U9						
	19	FF36		19	FF38						
	20	PP02		20	PP02						

P/O Level/Modulation Output A2A3 SERVICE SHEET 14

P/O A2A3 ASSEMBLY

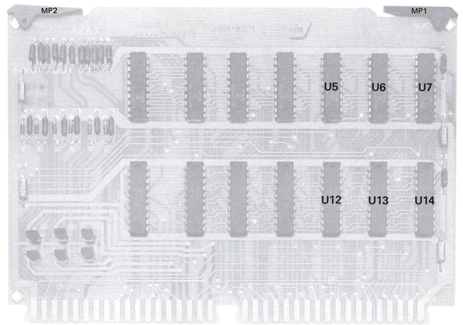
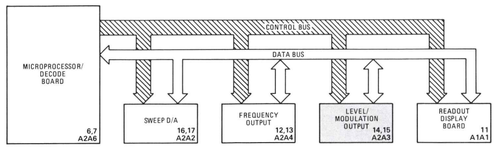


Figure 8-343. P/O A2A3 Level/Modulation Output Component Locations



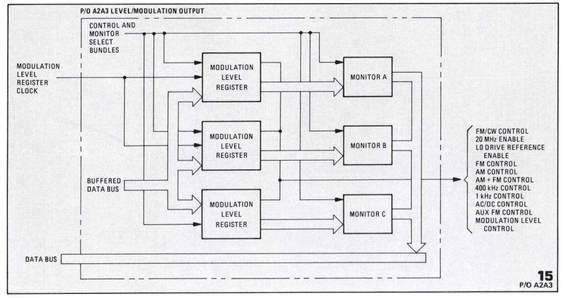


Figure 8-344. P/O A2A3 Level/Modulation Output Block Diagrams

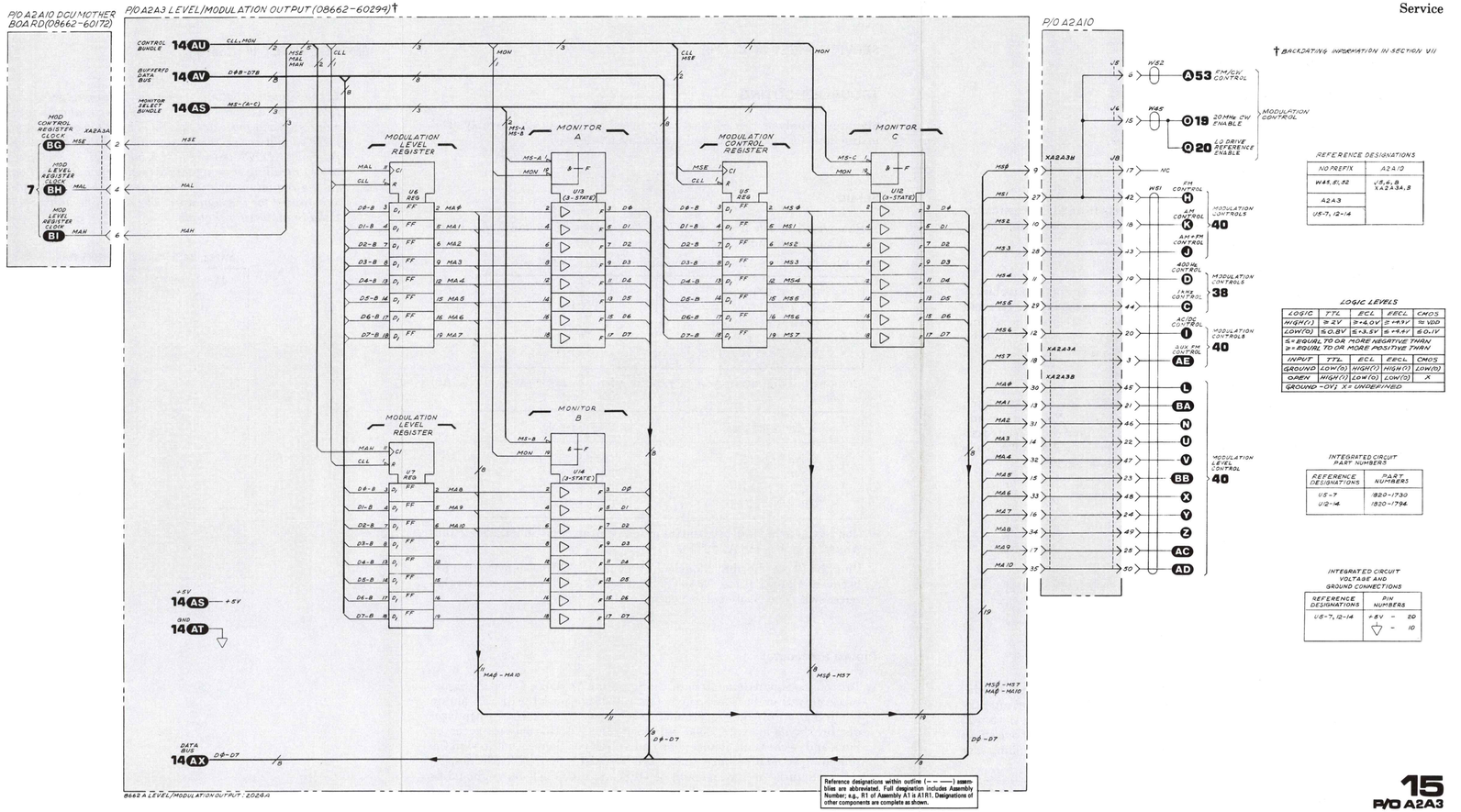


Figure 8-345. P/O A2A3 Level/Modulation Output Schematic

SERVICE SHEET 16
P/O A2A2 SWEEP D/A ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram B
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

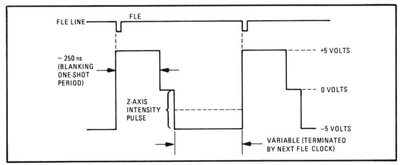
The Sweep D/A Assembly is shown on service sheets 16 and 17. The circuitry found on this service sheet generates the horizontal (X-axis) sweep-ramp signal, the Z-axis intensity marker, and the triangular marker.

D/A Sweep Ramp Generator

The sweep-ramp is controlled by the microprocessor by way of the data bus. A high-order byte and a low-order byte are clocked into sweep latches U14 and U11 by the DAH (D/A high byte) and DAL (D/A low byte) lines which come from data bus buffer U17 (service sheet 17). The MOS D/A converter (U7) then drives op-amp U2 to output a high resolution staircase sweep-ramp.

Frequency Blanking One-Shot

The frequency blanking one-shot (U1) is controlled by the frequency latch enable (FLE) line which enters the board at pin 26. This one-shot overrides any sweep marker enable (SME) pulses which come into U3 and its associated circuitry via pin 13. During a frequency change, a blanking pulse of +5 volts occurs at pin 27, regardless of sweep markers (see diagram below).



Z-Axis Blanking/Marker at Pin 27 of Sweep Board

Z-Axis Intensity Marker

The Z-axis intensity marker pulse (0 to −5 volts) is adjustable as the shaded area in the diagram indicates. The negative going pulse is created after the FLE line goes HI (the FLE line always overrides the SME line at the pin 27 output). After the FLE line goes HI and the frequency blanking one-shot's pulse drops, the SME line drives the output negative until the next falling edge of FLE occurs.

Triangular Marker Output

The marker output is controlled by the FLE and the SME lines. These lines are latched by U5A and U5D. When the SME line goes HI, FET Q5 is turned on and a 5 kHz pulse from the Keycode Board is gated into op-amp U6. This generates a triangular tone burst at pin 31. A tone burst is generated for each marker location stored in RAM.

SERVICE SHEET 16 (Cont'd)

TROUBLESHOOTING

Signature Analysis can be used to troubleshoot the A2A2 assembly. The instructions for using this technique are given below.

Set-up

1. Remove all boards from the DCU section except A2A6 and A2A2. Place A2A2 on an extender.
2. Set the Signature Analyzer pushbutton switches as follows:

START BUTTON	(OUT)
STOP BUTTON	(IN)
CLOCK BUTTON	(IN)
HOLD BUTTON	(OUT)
SELF-TEST BUTTON	(OUT)

3. Connect the Signature Analyzer to the microprocessor assembly (A2A6) as follows:

Signature Analyzer	A2A6 Assembly
START LEAD	TP2 ("ST")
STOP LEAD	TP2 ("ST")
CLOCK LEAD	TP1 ("SA, CK")
GROUND LEAD	TP6 ("GND")

4. Connect a ground lead between the ground pin (near the tip of the Signature Analyzer probe) and A2A6TP6.
5. Plug the 10-pin shorting connector at the top of A2A6. Connect a jumper between A2A6TP4 and A2A6TP6 and set A2A6U5 (diagnostic routine select switch) to position 3 (between 2 and 4).

Pretest Procedure

1. Turn on the Signal Generator and the Signature Analyzer. Touch the Signature Analyzer probe to any convenient +5 Vdc pin, push the RESET button on the Signature Analyzer probe and then release. The Signature Analyzer display should indicate "0000" and then "6F90". If this does not occur, go back and re-check all connections and switch positions as outlined in the preceding setup procedure. Also, the UNSTABLE SIGNATURE lamp on the Signature Analyzer should be OFF and the GATE lamp should be flashing.
2. For this test, all annunciators should be glowing dimly. The +1 digit (left-hand side of the amplitude display) and HP-IB indicator lamps (2) should be on. Any other digit display is meaningless.
3. No button, switch or connection should be altered in the course of taking signatures on the Sweep Board (A2A2).

SERVICE SHEET 16 (Cont'd.)

NOTE

In the Signature listings the reference designator for each device is followed by a + or − sign; or each pin number is preceded by a + or − sign. A + indicates the CLOCK button on the Signature Analyzer should be set to take signatures on the positive edge of the reference CLOCK pulse (CLOCK button OUT). A − indicates a negative or trailing edge signature reading (CLOCK button IN).
In the Signature listings some devices have a dashed line (----) substituted for the signature. The dash line indicates there is no valid Signature for that pin.

Sweep Board (P/O A2A2) Signatures

U11-	1	6F90	U14- 1 0000
	2	6F90	2 6F90
	3	----	3 5C15
	4	5C15	4 P0A4
	5	P0A4	5 6F90
	6	----	6 6F90
	7	6F90	7 6FA2
	8	0000	8 F14U
	9	6F90	9 6F90
	10	----	10 0000
	11	----	11 6F90
	12	6FA2	12 6F90
	13	F14U	13 UA60
	14	----	14 6680
	15	----	15 6F90
	16	6F90	16 6F90
			17 H752
			18 0988
			19 6F90
			20 6F90

P/O Level/Modulation Output A2A3 SERVICE SHEET 15

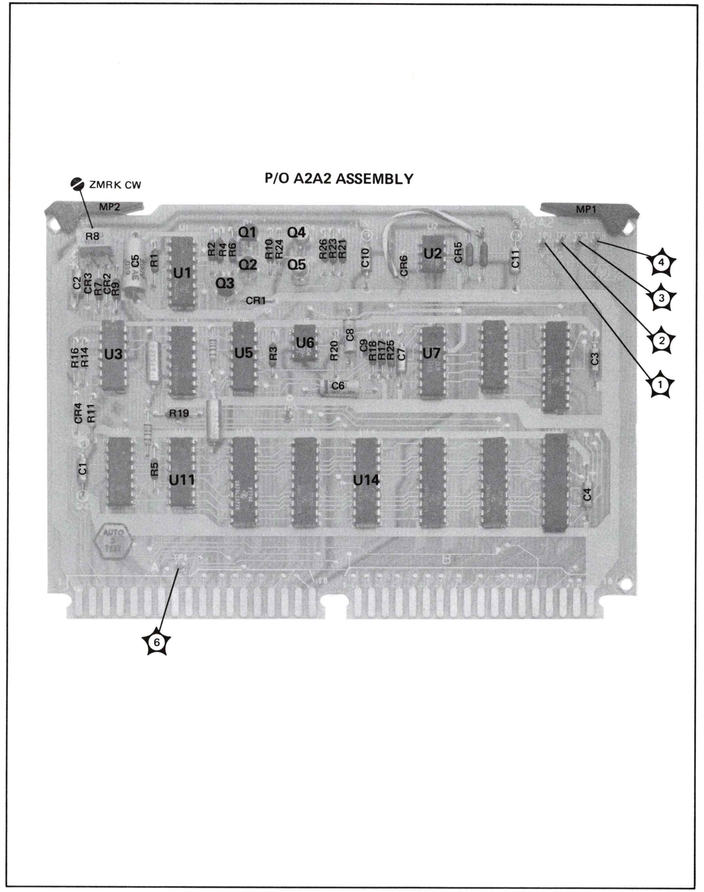
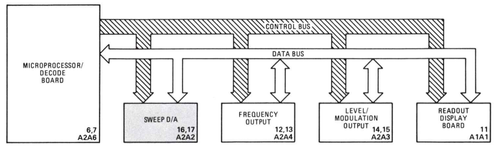


Figure 8-346. P/O A2A2 Sweep Board Component Locations



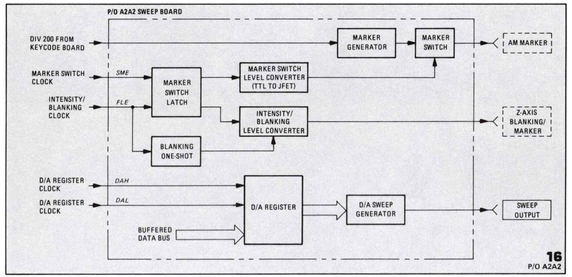
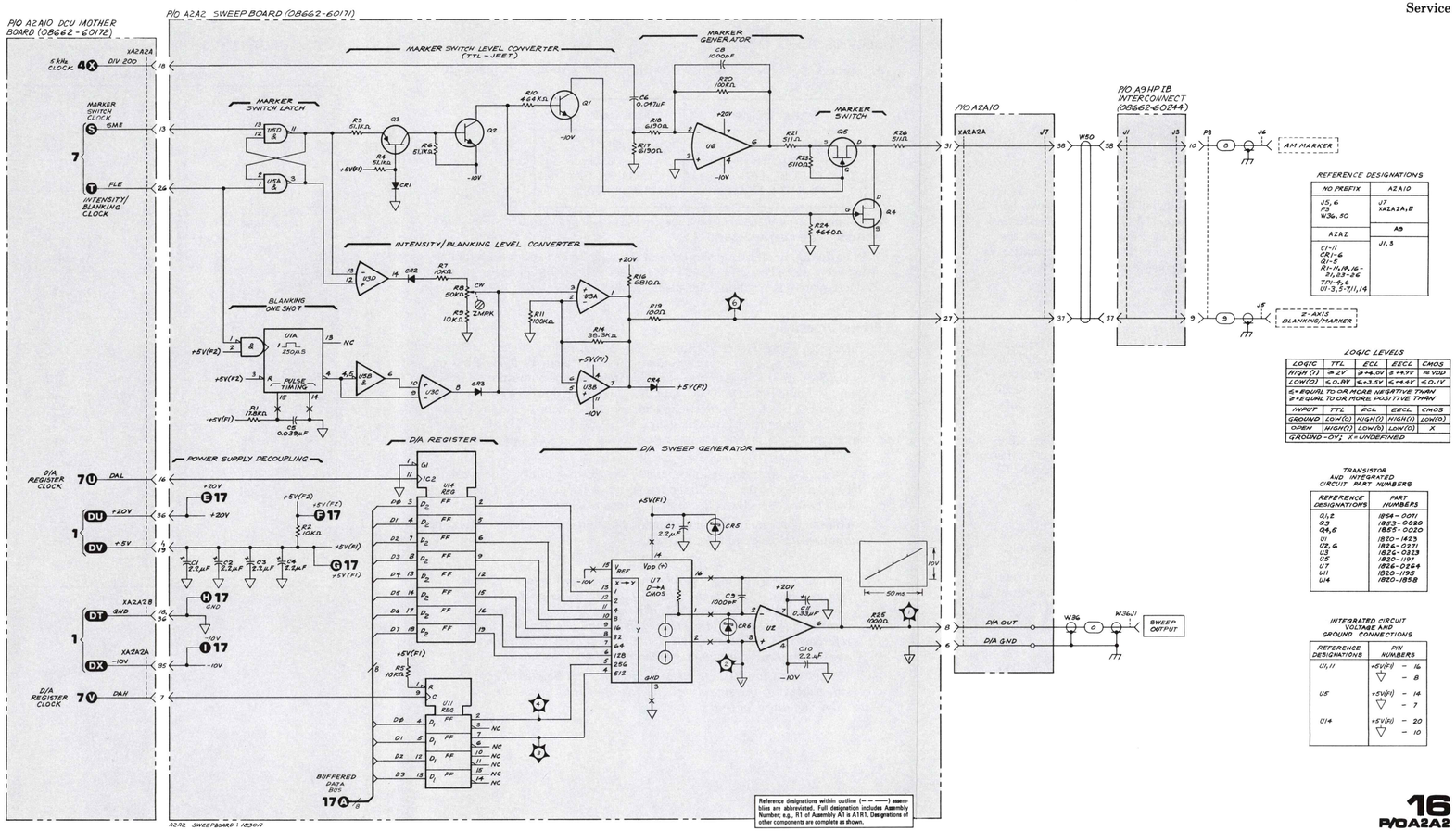


Figure 8-347. P/O A2A2 Sweep Board Block Diagrams



REFERENCE DESIGNATIONS

NO PREFIX	A2A10
J5, 6 P3 W36, 50	J7 XA2A2A,B
A2A2	A9 J1, 3
C1-11 CR1-16 Q1-5 R1-11,18,19, 21,23-26 TP1-4,6 U1,3,5-11,14	

LOGIC LEVELS

LOGIC	TTL	ECL	EECL	CMOS
HIGH (1)	≥ 2V	≥ -1.0V	≥ +4.3V	≈ VDD
LOW (0)	≤ 0.8V	≤ -1.5V	≤ +4.1V	≤ 0.1V

≤ = EQUAL TO OR MORE NEGATIVE THAN
≥ = EQUAL TO OR MORE POSITIVE THAN

INPUT	TTL	ECL	EECL	CMOS
GROUND	LOW (0)	HIGH (1)	HIGH (1)	LOW (0)
OPEN	HIGH (1)	LOW (0)	LOW (0)	X

GROUND = 0V; X = UNDEFINED

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1,2	1854-0071
Q3	1853-0020
Q4,5	1855-0020
U1	1820-1423
U2, 6	1826-0271
U3	1826-0213
U5	1820-1191
U7	1826-0244
U11	1820-1195
U14	1820-1858

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U1,11	+5V(F1) - 16 ▽ - 8
U5	+5V(F1) - 14 ▽ - 7
U14	+5V(R) - 20 ▽ - 10

16 P/O A2A2

Figure 8-348. P/O A2A2 Sweep Board Schematic

SERVICE SHEET 17
P/O A2A2 SWEEP D/A ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram B
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The Sweep D/A Assembly is shown on service sheets 16 and 17. The circuitry found on this service sheet contains the front panel LED indicator select lines and the status LED flash generator. This part of the assembly outputs the enable signal to the rotary pulse generator (RPG) and the auxiliary X-Y plotter. The outputs include the reverse-power-reset pulse and sweep clock select signal.

LED Indicator Select and LED Register Circuitry

Data from the microprocessor is buffered by U17 and latched by LED register latches U9, U12, U13, U15, and U16. Address bits A0, A1, and A2 at U10 determine the register to which the data is sent. U10 clocks the register specified by the data on the address lines and latches the data. U10 has no control over U11 or U14 (service sheet 16), although these D/A registers do obtain data from data bus buffer U17.

There are forty registers (latches) on this assembly. Twenty-nine of them store information used to control the key LEDs on the front panel keyboard. Of the remaining eleven latches, six are used for control functions, four are NOT connected, and one is used for activation of the STATUS LED flash generator.

STATUS LED Generator

The STATUS LED flash generator, composed of U4 and associated timing components R6, C10, R7 and C11, oscillates as long as pin 16 on U13 is LO. The period of this oscillator is approximately one second, with a 50% duty cycle. Register U13 produces either a steady-state or flashing signal which is output at OR gate U8D. This output is sent to the front panel STATUS LED.

TROUBLESHOOTING

Signature Analysis can be used to troubleshoot the A2A2 assembly. The instructions for using this technique are given below.

Set-up

1. Remove all boards from the DCU section except A2A6 and A2A2. Place A2A2 on an extender.
2. Set the Signature Analyzer pushbutton switches as follows:

START BUTTON	⌐ (OUT)
STOP BUTTON	¬ (IN)
CLOCK BUTTON	¬ (IN)
HOLD BUTTON	(OUT)
SELF-TEST BUTTON	(OUT)

SERVICE SHEET 17 (Cont'd)

3. Connect the Signature Analyzer to the microprocessor assembly (A2A6) as follows:

Signature Analyzer	A2A6 Assembly
START LEAD	TP2 ("ST")
STOP LEAD	TP2 ("ST")
CLOCK LEAD	TP1 ("SA, CK")
GROUND LEAD	TP6 ("GND")

4. Connect a ground lead between the ground pin (near the tip of the Signature Analyzer probe) and A2A6TP6.
5. Plug the 10-pin shorting connector at the top of A2A6. Connect a jumper between A2A6TP4 and A2A6TP6 and set A2A6U5 (diagnostic routine select switch) to position 3 (between 2 and 4).

Pretest Procedure

1. Turn on the Signal Generator and the Signature Analyzer. Touch the Signature Analyzer probe to any convenient +5 Vdc pin, push the RESET button on the Signature Analyzer probe and then release. The Signature Analyzer display should indicate "0000" and then "6F90". If this does not occur, go back and re-check all connections and switch positions as outlined in the preceding setup procedure. Also, the UNSTABLE SIGNATURE lamp on the Signature Analyzer should be OFF and the GATE lamp should be flashing.
2. For this test, all annunciators should be glowing dimly. The +1 digit (left-hand side of the amplitude display) and HP-IB indicator lamps (2) should be on. Any other digit display is meaningless.
3. No button, switch or connection should be altered in the course of taking signatures on the Sweep Board (A2A2).

NOTE

In the Signature listings the reference designator for each device is followed by a + or − sign; or each pin number is preceded by a + or − sign. A + indicates the CLOCK button on the Signature Analyzer should be set to take signatures on the positive edge of the reference CLOCK pulse (CLOCK button OUT). A − indicates a negative or trailing edge signature reading (CLOCK button IN).

In the Signature listings some devices have a dashed line (----) substituted for the signature. The dash line indicates there is no valid Signature for that pin.

SERVICE SHEET 17 (Cont'd)

† Sweep Board (P/O A2A2) Signatures

U8-	1	3C97	U10-	1	----	U13-	1	391U	U16-	1	391U
	2	3C97		2	----		2	43UU		2	U11U
	3	3C97		3	----		3	5C15		3	5C15
	4	----		4	----		4	P0A4		4	P0A4
	5	----		5	798A		5	H2H2		5	5U82
	6	----		6	391U		6	P200		6	58UH
	7	0000		7	6F90		7	6FA2		7	6FA2
	8	1P56		8	0000		8	F14U		8	F14U
	9	1P56		9	6F90		9	HP80		9	7756
	10	1P56		10	6F90		10	0000		10	0000
	11	06A4		11	6F90		11	6F90		11	6F90
	12	06A4		12	6F90		12	H9A6		12	95CF
	13	6F90		13	6F90		13	UA60		13	UA60
	14	6F90		14	6F90		14	6680		14	6680
				15	6F90		15	06A4		15	8UH6
				16	6F90		16	918C		16	0145
U9-	1	391U		17	6F90		17	H752		17	H752
	2	9CU5		18	6F90		18	0988		18	0988
	3	5C15		19	6F90		19	P044		19	3C97
	4	P0A4		20	6F90		20	6F90		20	6F90
	5	7U17									
	6	0984									
	7	6FA2	U12-	1	391U	U15-	1	391U	U17-	1	0000
	8	F14U		2	A307		2	707F		2	5C15
	9	A615		3	5C15		3	5C15		3	5C15
	10	0000		4	P0A4		4	P0A4		4	P0A4
	11	6F90		5	PAF1		5	1H08		5	P0A4
	12	7U1P		6	89HH		6	8H33		6	6FA2
	13	UA60		7	6FA2		7	6FA2		7	6FA2
	14	6680		8	F14U		8	F14U		8	F14U
	15	1P56		9	0569		9	044P		9	F14U
	16	3HH4		10	0000		10	0000		10	0000
	17	H752		11	6F90		11	6F90		11	UA60
	18	0988		12	CUC9		12	8359		12	UA60
	19	867F		13	UA60		13	UA60		13	6680
	20	6F90		14	6680		14	6680		14	6680
				15	833A		15	C60F		15	H752
				16	H02U		16	F293		16	H752
				17	H752		17	H752		17	0988
				18	0988		18	0988		18	0988
				19	PFUA		19	H628		19	0000
				20	6F90		20	6F90		20	6F90

P/O Sweep Board A2A2 SERVICE SHEET 16

P/O A2A2 ASSEMBLY

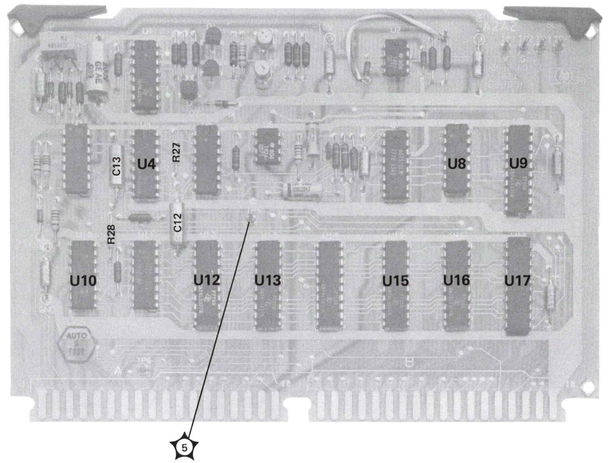
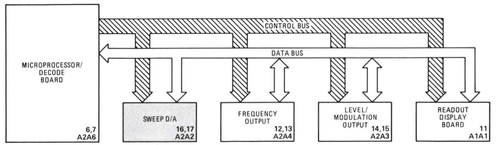


Figure 8-349. P/O A2A2 Sweep Board Component Locations



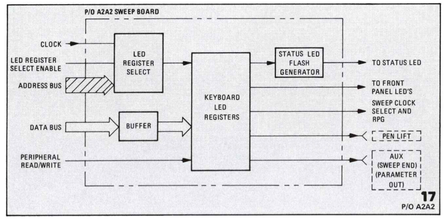
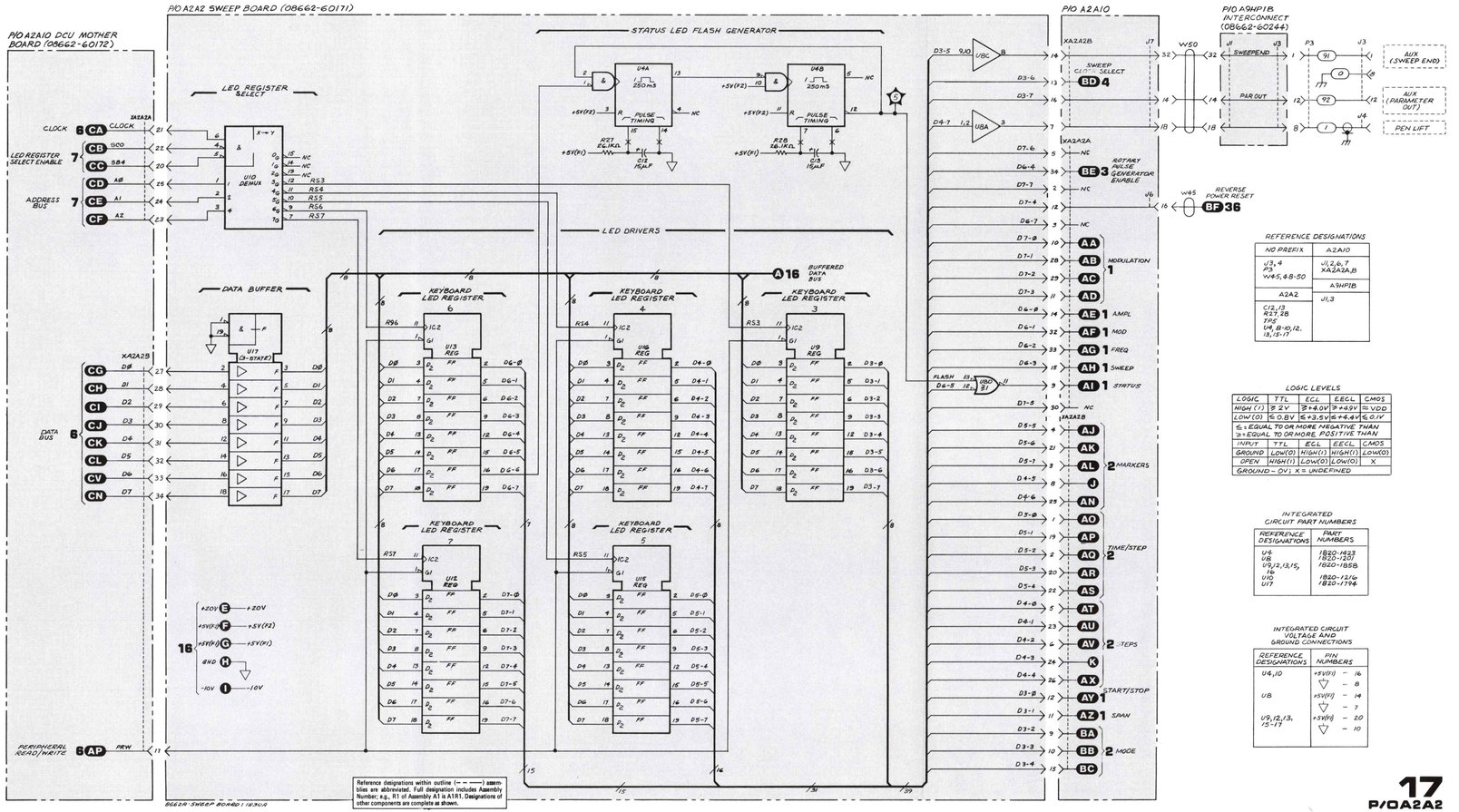


Figure 8-350. P/O A2A2 Sweep Board Block Diagrams



REFERENCE DESIGNATIONS

NO PREFIX	A2A10
U3, 4 P3 W45, 48-50	U1, 2, 6, 7 XA2A2A, B
	A9HP1B
A2A2	U1, 3
C12, 13 R27, 28 TP5 U4, 8-10, 12, 13, 15-17	

LOGIC LEVELS

LOGIC	TTL	ECL	EECL	CMOS
HIGH (1)	≥ 2 V	≥ +4.6V	≥ +4.9V	= VDD
LOW (0)	≤ 0.8V	≤ +3.5V	≤ +4.4V	≤ 0.1V
≤ = EQUAL TO OR MORE NEGATIVE THAN ≥ = EQUAL TO OR MORE POSITIVE THAN				
INPUT	TTL	ECL	EECL	CMOS
GROUND	LOW(0)	HIGH(1)	HIGH(1)	LOW(0)
OPEN	HIGH(1)	LOW(0)	LOW(0)	X
GROUND – 0V; X = UNDEFINED				

INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
U4 U8 U9, 12, 13, 15, 16 U10 U17	1820-1423 1820-1201 1820-1858 1820-1216 1820-1794

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U4, 10	+5V(1) – 16 ▽ – 8
U8	+5V(1) – 14 ▽ – 7
U9, 12, 13, 15-17	+5V(1) – 20 ▽ – 10

17
P/O A2A2

Figure 8-351. P/O A2A2 Sweep Board Schematic



Printed in U.S.A.

SERVICE MANUAL

8662A Synthesized Signal Generator

10 kHz — 1280 MHz



P/O Section VIII
Service Sheets

18-29

Reference Section
High Frequency Loops

HP Part Number 08662-90044
Printed January 1980
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SERVICE SHEET 18
A8A3 AND A8A4 10 MHz REFERENCE OSCILLATOR AND REFERENCE BUFFER ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram C
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The Reference Buffer amplifies and distributes the reference source signal to the rest of the instrument. The reference source can be the internal 10 MHz Reference Oscillator (A8A3) or an external frequency standard of 5 or 10 MHz. The outputs from the Reference Buffer are always 10 MHz, even when an external frequency standard of 5 MHz is selected. The internal reference oscillator is a high stability, temperature controlled, 10 MHz quartz oscillator.

Doubler Circuit

When an external frequency standard of 5 MHz is used, the 5 MHz signal is passed through a frequency doubler circuit. The doubler circuit is a full-wave rectifier, consisting of a center-tapped transformer (T1) and two Schottky diodes (CR1 and CR2). Following the doubler circuit is a 10 MHz bandpass amplifier which minimizes the feed through of the fundamental frequency (5 MHz).

Power Splitters

Transformers T2 through T9 and associated circuitry form a five-way power splitter. The 10 MHz input signal is applied to the primary of transformer T2. The resistors across the secondary windings of T4, T7, T8, and T9 provide a 50 ohm impedance match and also increase isolation between the five output ports.

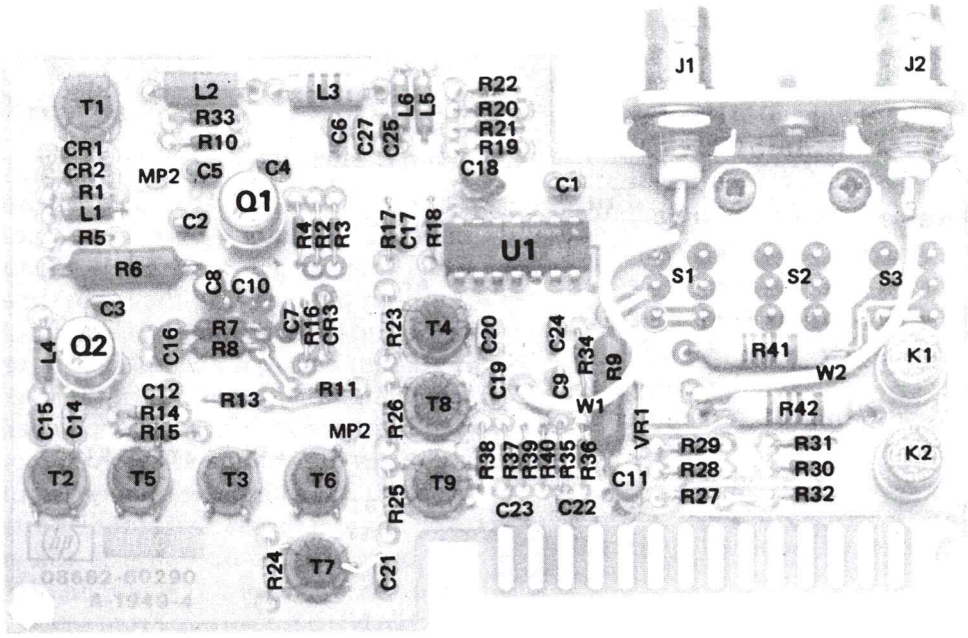
No Reference Detector

The No Reference Detector monitors the output of Q2 to check for the presence of the 10 MHz signal. As long as the 10 MHz reference signal is present, capacitor C17 remains charged. In the absence of the 10 MHz signal due to the loss of the reference source (internal or external) or a circuit malfunction, C17 starts discharging. When the voltage across C17 falls below the comparator's reference (at its inverting input) the comparator goes low, signaling the DCU that no signal is present at the output of Q2.

Oven Status Detector

The Oven Status Detector detects whether or not the internal oscillator's oven temperature has stabilized. From a cold start, that is, the instrument has not been plugged into the Main (line) voltage, the voltage at the oven monitor terminal (A8A3 pin 11) is high. This causes the comparator's output to go low, which signals the DCU that the oven temperature has not heat stabilized. As the oven temperature stabilizes the voltage at the oven monitor terminal drops. It takes approximately 15 minutes for the oven temperature to heat stabilize after the line cord has been plugged in. Power is still supplied to the oven (via A8A3 pin 14) when the LINE switch is in the STANDBY position. From a cold start, the oscillator should be within one hertz of its final value after 10 minutes.

A8A4 ASSEMBLY



† Figure 8-401. A8A4 Reference Buffer Component Locations

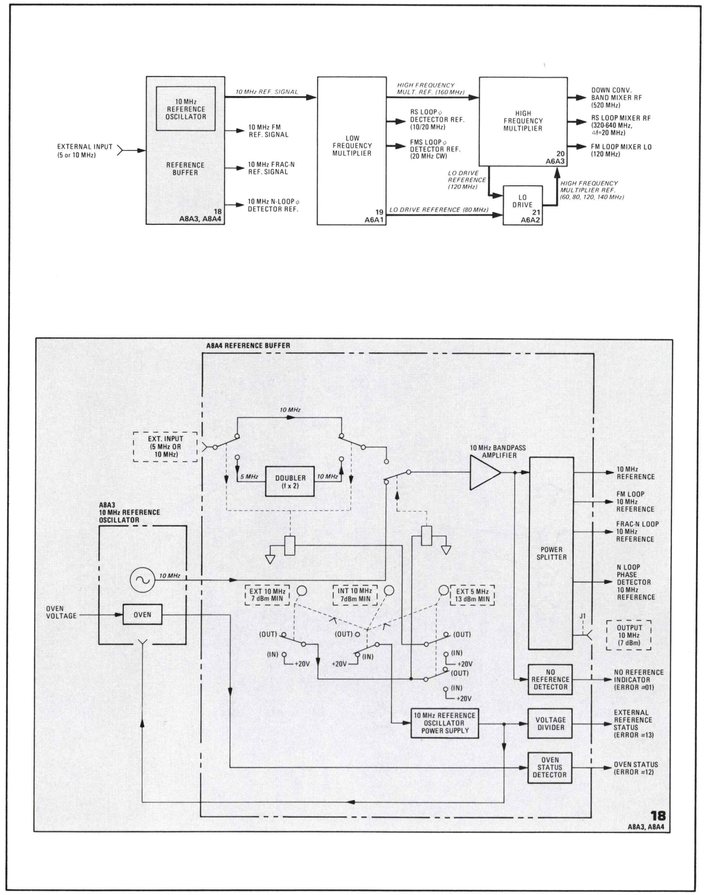


Figure 8-402. A8A3 and A8A4 10 MHz Reference Oscillator and Buffer Block Diagrams

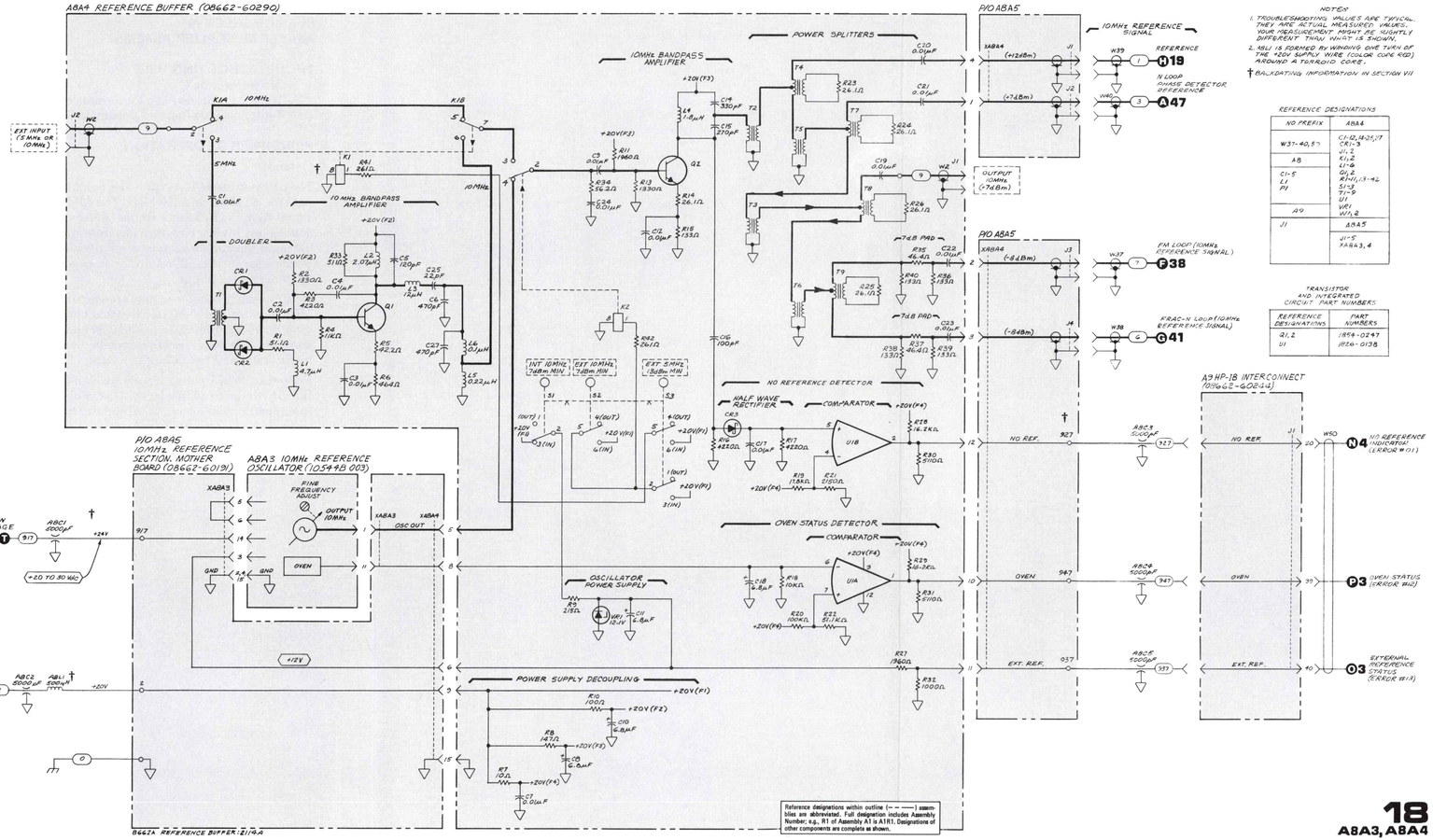


Figure 8-403. A8A3 and A8A4 10 MHz Reference Oscillator and Buffer Schematic

SERVICE SHEET 19
A6A1 LF MULTIPLIER ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram C
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The LF Multiplier (A6A1) provides output signals at 10 MHz, 20 MHz, 40 MHz, 80 MHz, and 160 MHz. The LF Multiplier takes the 10 MHz signal from the Reference Buffer (A8A4) and by the use of frequency doubler and divider circuits it generates the other desired frequencies. Since all the output signals are derived from the 10 MHz Reference Buffer signals, they all retain the same accuracy and stability as the reference source signal.

Four frequency doubler circuits are cascaded in order to multiply the 10 MHz input up to 160 MHz. The other output signals are obtained by tapping various points in the doubler chain. The Doubler circuits are basically full-wave rectifier circuits, consisting of a center-tapped transformer and two Schottky diodes.

Following each Doubler circuit are Band-Pass Amplifiers which are tuned to the doubled frequency. This minimizes the feed through of the fundamental frequency and eliminates unwanted harmonics.

The 40 MHz Filter, FL1, is a narrow band crystal filter. This filter contributes significantly to the Signal Generator's single-sideband phase noise performance.

A6A1 ASSEMBLY

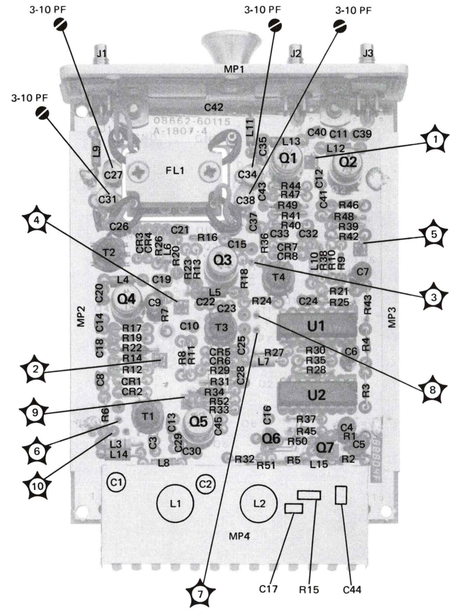


Figure 8-404. A6A1 Reference Section LF Multiplier Component Locations

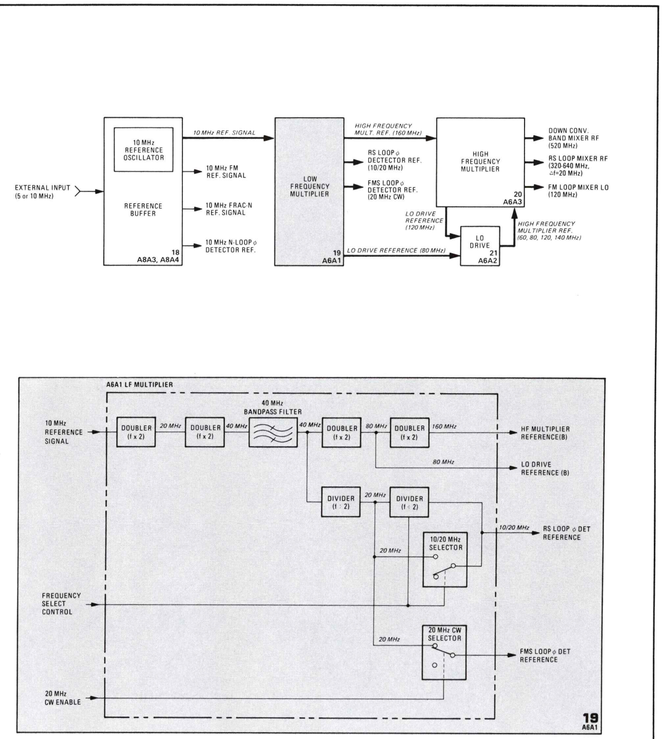
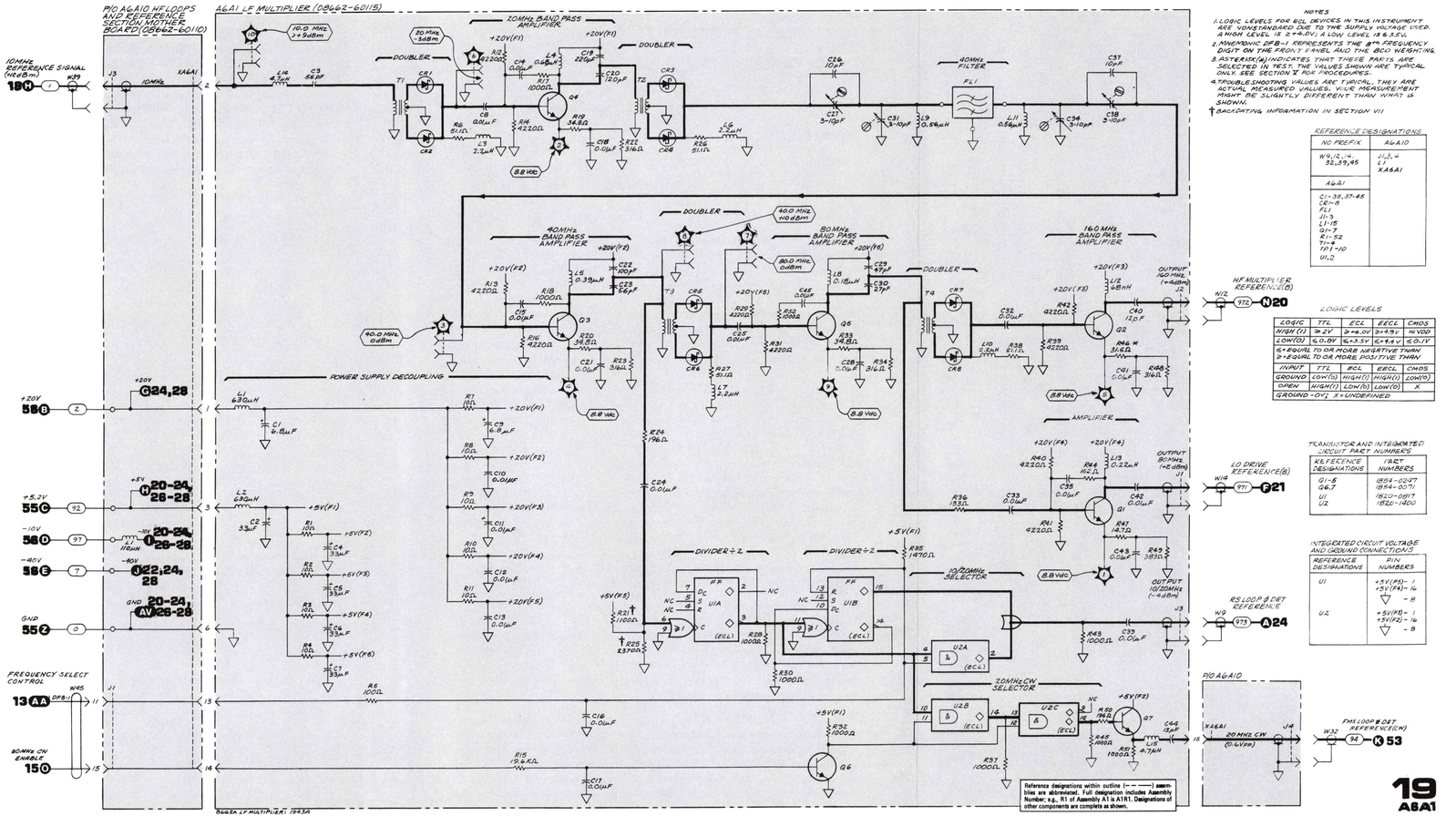


Figure 8-405. A6A1 Reference Section LF Multiplier Block Diagrams



NOTES

1. LOGIC LEVELS FOR ECL DEVICES IN THIS INSTRUMENT ARE NONSTANDARD DUE TO THE SUPPLY VOLTAGE USED. A HIGH LEVEL IS ≥ +4.0V; A LOW LEVEL IS ≤ 3.5V.
2. A NONNUMERIC DASH (-) REPRESENTS THE Ø TH FREQUENCY DIGIT ON THE FRONT PANEL AND THE BCD WEIGHTING.
3. ASTERISK(✱) INDICATES THAT THESE PARTS ARE SELECTED IN TEST. THE VALUES SHOWN ARE TYPICAL ONLY. SEE SECTION V FOR PROCEDURES.
4. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENT MIGHT BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.

† BACKDATING INFORMATION IN SECTION VII

REFERENCE DESIGNATIONS

NO PREFIX	A6A10
W9, 12, 14, 32, 39, 45	J3, 4
	L1
	XA6A1
A6A1	
C1-35, 37-48	
C47-8	
FL1	
J1-3	
L1-15	
Q1-7	
R1-52	
T1-4	
TP1-10	
U1, 2	

LOGIC LEVELS

LOGIC	TTL	ECL	ECL	CMOS
HIGH (1)	≥ 2V	≥ +4.0V	≥ +4.9V	≈ VDD
LOW (0)	≤ 0.8V	≤ +3.5V	≤ +4.4V	≤ 0.1V
X = EQUAL TO OR MORE NEGATIVE THAN -2 = EQUAL TO OR MORE POSITIVE THAN				
INPUT	TTL	ECL	ECL	CMOS
GROUND	LOW (0)	HIGH (1)	HIGH (1)	LOW (0)
OPEN	HIGH (1)	LOW (0)	LOW (0)	X

GROUND = 0V; X = UNDEFINED

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1-6	1854-0247
Q6,7	(1854-0071)
U1	1820-0817
U2	1820-1400

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U1	+5V (F5) - 1
	+5V (F4) - 14
	- 8
U2	+5V (F8) - 1
	+5V (F2) - 14
	- 8

Figure 8-406. A6A1 Reference Section LF Multiplier Schematic

SERVICE SHEET 20
A6A3 HF MULTIPLIER ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram C
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The HF Multiplier (A6A3) generates four separate output signals from its two input signals. Three of the output signals are fixed in frequency, while the fourth output varies from 320 to 640 MHz in 20 MHz steps.

The two 120 MHz output signals, the LO Drive Reference A and the FM Loop Mixer LO, are generated by multiplying, heterodyning, and dividing the 160 MHz input signal, the HF Multiplier Reference (B). The 160 MHz input signal is first passed through a 160 MHz Band-Pass Filter. The 160 MHz filter, FL1, is a narrow band crystal filter. This filter contributes significantly to the Signal Generator's single-sideband phase noise performance. After the 160 MHz Band-Pass Filter, the signal path splits into two paths. One signal path goes to the LO port of Mixer U10, and the other goes to the 160 MHz Band-Pass Amplifier and Doubler circuit. The Doubler is a full-wave rectifier circuit, consisting of a center-tapped transformer and two Schottky diodes. The 320 MHz Band-Pass Amplifier amplifies the doubled frequency while attenuating the fundamental and the undesired higher harmonics. Limiter U7 provides a constant signal level to the RF port of Mixer U10. Mixer U10 heterodynes the 320 MHz signal with the 160 MHz input signal and the resulting sum, 480 MHz, is then amplified by the 480 MHz Band-Pass Amplifier. The 480 MHz Band-Pass Amplifier and the 480 MHz Band-Pass Filter attenuate the residual LO and RF signals and the undesired difference signal. The 480 MHz signal is divided by counter U9, to obtain the 120 MHz output signal. U9 is an ECL device and has complimentary outputs. The two 120 MHz output signals from U9 are then amplified by the 120 MHz Band-Pass Amplifiers which remove the unwanted harmonics from the 120 MHz square wave outputs.

The 520 MHz output signal is generated by doubling the 320 MHz signal from the collector of Q 5 and heterodyning the doubled signal (640 MHz) with the 120 MHz signal from U9. Mixer U1 is a double balanced mixer. The 520 MHz Switch and Band-Pass Amplifier can be turned off by cutting off the emitter current to Q1. The amplifier is tuned to amplify the difference signal and filter the sum signal and the residual input signals (LO and RF).

The 320 to 640 MHz (Δf = 20 MHz) output is generated by heterodyning various combinations of input signals. Mixer U4 is a double balanced mixer (same as U1 and U10) but instead of normally feeding the two input signals into the RF and LO ports, one input signal is applied to the mixer's IF port and the output is taken at the mixer's RF port. In this configuration the mixer acts as a current-controlled switch (normal mixing action is disabled) when a dc current is applied to the mixer's IF port. That is, if a dc control current is applied to the IF port, the signal at the LO port is allowed to pass straight through to the RF

SERVICE SHEET 20 (Cont'd)

port. The input signals to the IF port come from the LO Drive (60, 80, 120, and 140 MHz) and the Controller (which supplies the dc control current to disable the mixer). The input signals to the LO port are derived from the HF Multiplier Reference (B) (320, 480, and 640 MHz). The 3 to 1 Multiplexer circuit, which is comprised of four limiters (U2, U3, U6 and U8), directs one of the three signals to the LO port. Limiters U2, U6, and U8 can be switched on and off by controlling the bias current flowing into the limiters (via pin 3 of the limiters). The voltage at pin 3 is about −10 Vdc when the limiters are enabled.

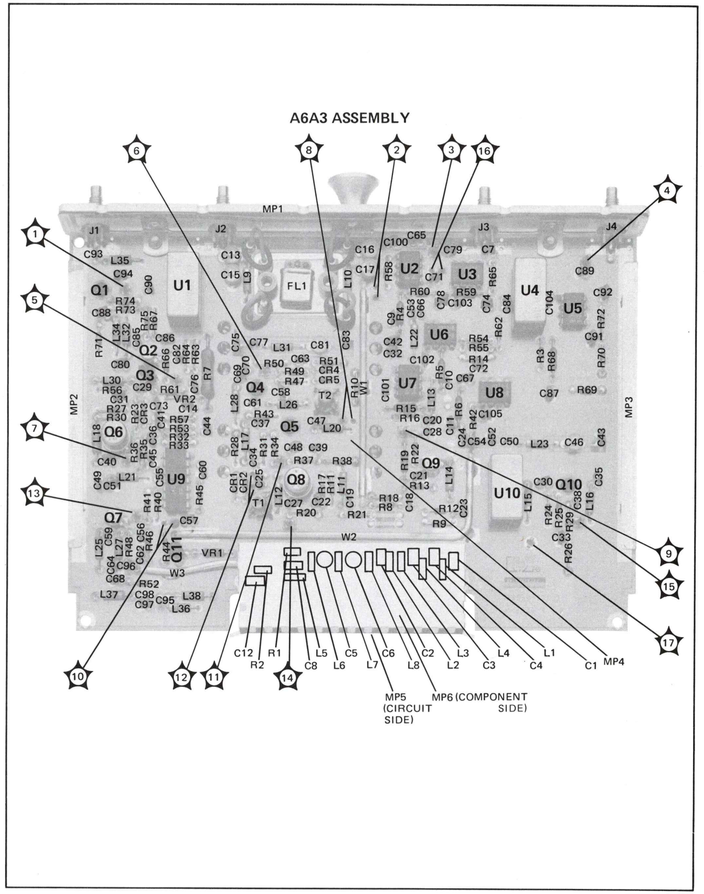


Figure 8-407. A6A3 Reference Section HF Multiplier Component Locations

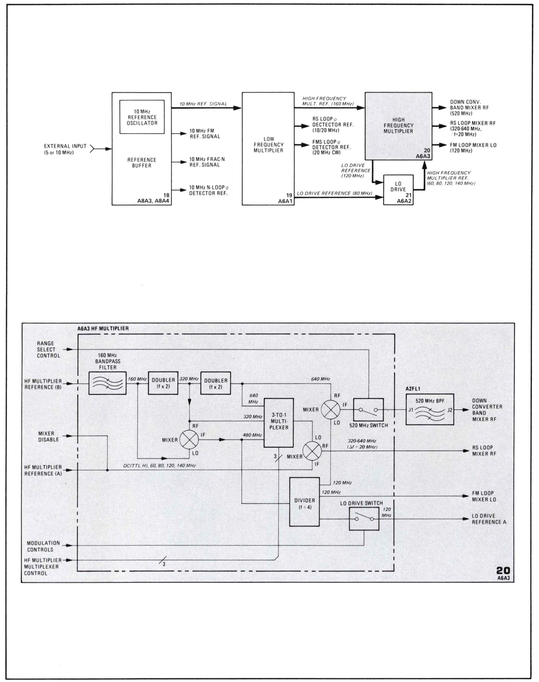
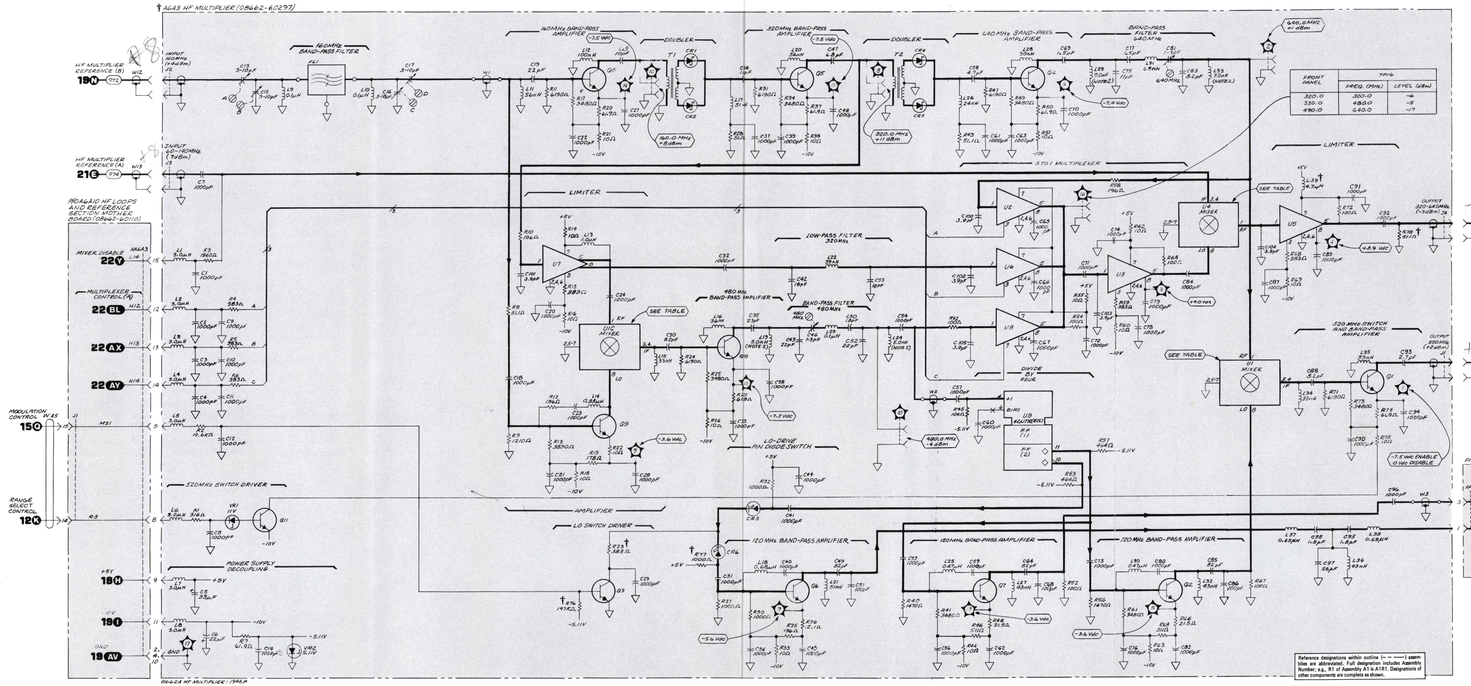


Figure 8-408. A6A3 Reference Section HF Multiplier Block Diagrams


†A6A3 HF MULTIPLIER (08662-60297)
HF MULTIPLIER REFERENCE (B) 19Ø
HF MULTIPLIER REFERENCE (A) 21Ø
A6A3A1 LOOP AND REFERENCE SECTION MOTHER BOARD (08662-60110)
MIXER DISABLE 22Ø
MULTIPLEXER CONTROL (5) 22BL 22AX 22AY
MODULATION CONTROL 15Ø
RANGE SELECT CONTROL 12Ø
+5V 18Ø
-5V 19Ø
INPUT (NOMINAL 0 dBm)
INPUT (60-140MHz, 0 dBm)
160MHz BAND-PASS FILTER
160MHz BAND-PASS AMPLIFIER
DOUBLER
320MHz BAND-PASS AMPLIFIER
DOUBLER
640 MHz BAND-PASS AMPLIFIER
BAND-PASS FILTER 640MHz
640 dBm +7 dBm
FRONT PANEL TAPS
320.0 330.0 490.0
FREQ. (MHz) 320.0 480.0 640.0
LEVEL (dBm) -8 -11 -17
LIMITER
3 TO 1 MULTIPLEXER
LOW-PASS FILTER 320MHz
480 MHz BAND-PASS AMPLIFIER
BAND-PASS FILTER 480MHz
320 MHz SWITCH AND BAND-PASS AMPLIFIER
OUTPUT 320-640MHz (+2 dBm)
MIXER
LO DRIVE PIN DIODE SWITCH
DIVIDE BY FOUR
BURN-IN FILTER(S)
120 MHz BAND-PASS AMPLIFIER
180MHz BAND-PASS AMPLIFIER
120 MHz BAND-PASS AMPLIFIER
320MHz SWITCH DRIVER
AMPLIFIER
LO SWITCH DRIVER
POWER SUPPLY DECOUPLING
+5V
-5.1V
-10V
-7.5V
+8V
+15V
-15V
+5V ENABLE
-5V ENABLE
-7.5V ENABLE
+5V ENABLE
-5.2V
-6.5V
-6.2V
-7.2 Vdc
-7.5 Vdc
-7.4 Vdc
-3.6 Vdc
+3.6 Vdc
+5.0 Vdc
+3.9 Vdc
-5.6 Vdc
-3.4 Vdc
-3.6 Vdc
+5.2 Vdc
+5.1 Vdc
+5.0 Vdc
+5.1 Vdc
+5.2

SERVICE SHEET 21
A6A2 LO DRIVE ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram C
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The LO Drive (A6A2) provides an output signal at either 60 MHz, 80 MHz, 120 MHz, or 140 MHz to the HF Multiplier (A6A3). A 4 to 1 Multiplexer circuit is used to select one of the four frequencies. The primary inputs are the 80 MHz signal (LO Drive Reference (B)), and the 120 MHz signal (LO Drive Reference (A)). When either the 80 MHz or 120 MHz output frequency is selected the corresponding input signal is routed to the output jack, J2. The 60 MHz output is derived by dividing the 120 MHz input by two. For an output of 140 MHz, the 60 MHz signal and 80 MHz input signal are mixed together.

Mixer

Mixer U3 is a double-balanced type which suppresses the input signals. The Mixer heterodynes the 60 MHz and 80 MHz signals to produce the 140 MHz signal (sum product). The difference signal and the residual input signal are attenuated by the 140 MHz Band-Pass Filter, leaving only the desired 140 MHz signal.

4 to 1 Multiplexer

The 4 to 1 Multiplexer consists of PIN diodes CR1 through CR8. PIN diodes act as current controlled resistors at RF frequencies. The Multiplexer Control, U2, supplies the control bias for the PIN diodes. The control bias is either switched on or off, hence, the PIN diodes act as RF switches. When the PIN diodes are forward biased the RF resistance is reduced, allowing the RF signal to pass. When the PIN diodes are reverse biased they offer high resistance to the RF signal.

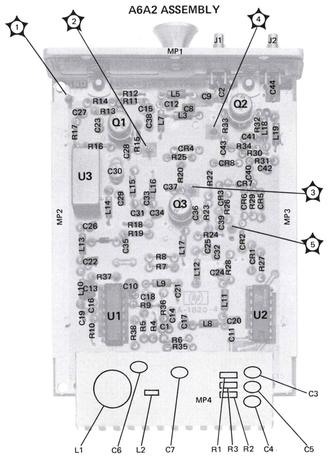
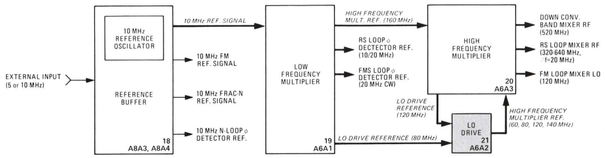


Figure 8-410. A6A2 Reference Section LO Drive Component Locations



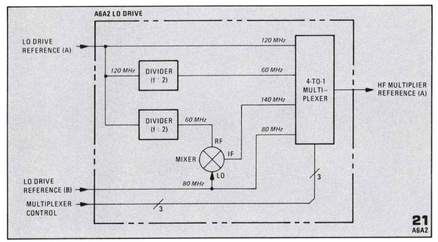
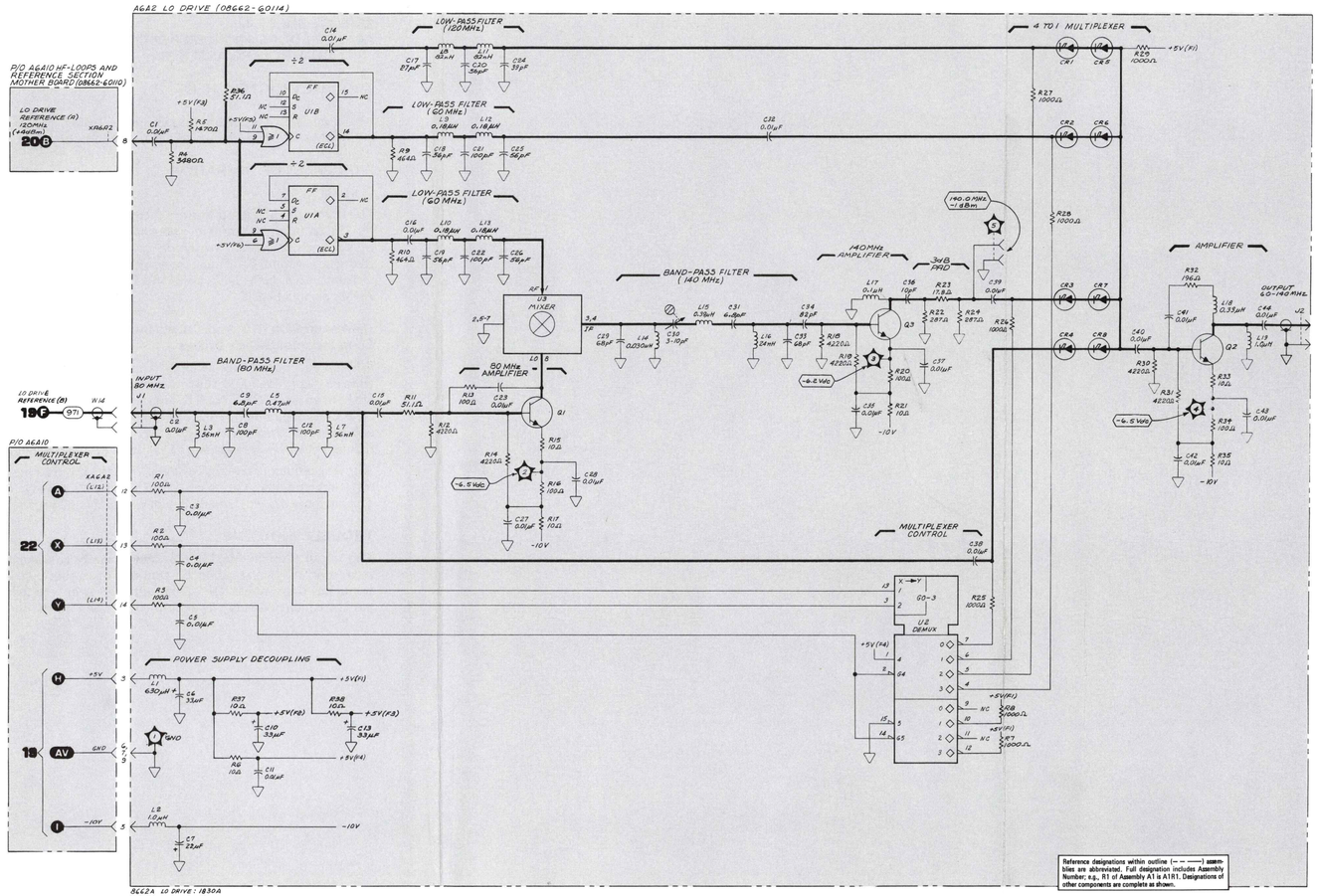


Figure 8-411. A6A2 Reference Section LO Drive Block Diagrams



CAUTION

RF TEST POINTS (PC BOARD EDGE CONNECTORS) MUST BE AC-COUPLED TO TEST EQUIPMENT, OTHERWISE DAMAGE MAY OCCUR TO THE TEST EQUIPMENT OR THE CIRCUIT UNDER TEST. USE THE SPECIAL COAXIAL-TO-CABLE COUPLED CABLE ADAPTER FOUND IN THE SERVICE KIT.

NOTE:

1. LOGIC LEVELS FOR ECL DEVICES IN THIS INSTRUMENT ARE NONSTANDARD DUE TO THE SUPPLY VOLTAGE USED. A HIGH LEVEL IS +4.4V, A LOW LEVEL IS +3.6V.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENT MIGHT BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.

REFERENCE DESIGNATIONS

NO PREFIX	A6A10
W13, 14	XA6A2
R6A2	
C1-44 CR1-8 J1,2 L1-3,5,7-19 Q1-3 R1-38 TP1-5 U1-3	

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1-3	1854-0247
U1	1820-0917
U2	1820-1046

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U1	+5V(F2) - 1 +5V(F3) - 16 ▽ - 8
U2	+5V(F4) - 16 ▽ - 8

LOGIC LEVELS

LOGIC	TTL	ECL	EECL	CMOS
HIGH (1)	≥ 2V	≥ +4.0V	≥ +4.9V	≥ VDD
LOW (0)	≤ 0.8V	≤ +3.5V	≤ +4.4V	≤ 0.1V
5 = EQUAL TO OR MORE NEGATIVE THAN 3 = EQUAL TO OR MORE POSITIVE THAN				
INPUT	TTL	ECL	EECL	CMOS
GROUND	LOW (0)	HIGH (1)	HIGH (1)	LOW (0)
OPEN	HIGH (1)	LOW (0)	LOW (0)	X
GROUND = 0V, X = UNDEFINED				

MIXER BOTTOM VIEW

BLUE LEAD

21 A6A2

Figure 8-412. A6A2 Reference Section LO Drive Schematic

SERVICE SHEET 22
A6A9 HF LOOPS AND REFERENCE SECTION CONTROLLER ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram D
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The ROMs on this board contain factory generated pre-tune and fine-tune information that provides precise control over loop gain, loop lock limits, high frequency switching, and VCO frequency in the high frequency section. BCD lines carrying information which corresponds to front panel digits DF7, DF8, and DF9 provide addressing for the ROMs on this board.

Reference Sum (RS) and Output Sum (OS) Loop Inductor Switch Drivers

When a pair of inductor switch drivers is stimulated by a HI output from its respective ROM, the first transistor (for example, Q1) is turned OFF, turning Q2 ON to pull the inductor line to −30 volts. This shuts OFF the inductor being controlled. When the ROM output goes LO, Q1 is turned ON. This turns Q2 OFF. When Q2 turns OFF, current flows through the PIN diode in the VCO, turning the inductor ON.

All of the inductor driver circuits work in the same manner, except that different transistors are used for different current drive capabilities. The currents are: a, 15ma; b, 30ma; c, 30ma; d, 60ma; and e, 120ma.

TROUBLESHOOTING

The output of the ROMs (U1, U2 and U3) can be checked using Signature Analysis. Service sheet B1 contains operating instructions. The frequency data inputs (DB7-1 through DF9-2) are related to the front panel frequency display as explained in note 1 on the schematic.

A6A9 ASSEMBLY

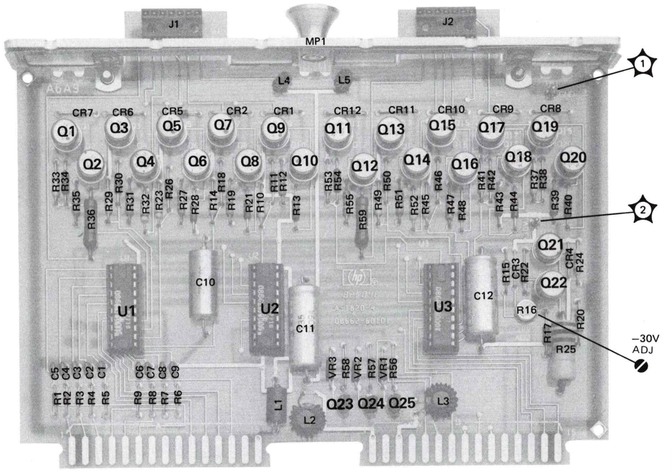


Figure 8-413. A6A9 High Frequency Loops and Reference Section Controller Component Locations

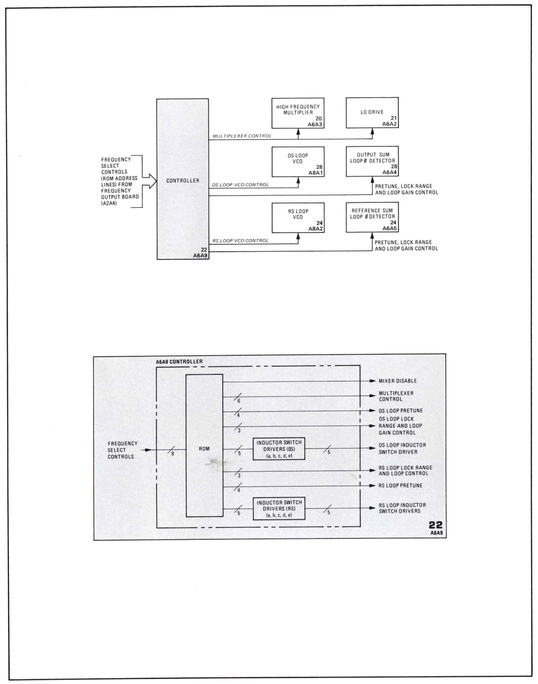


Figure 8-414. A6A9 High Frequency Loops and Reference Section Controller Block Diagrams

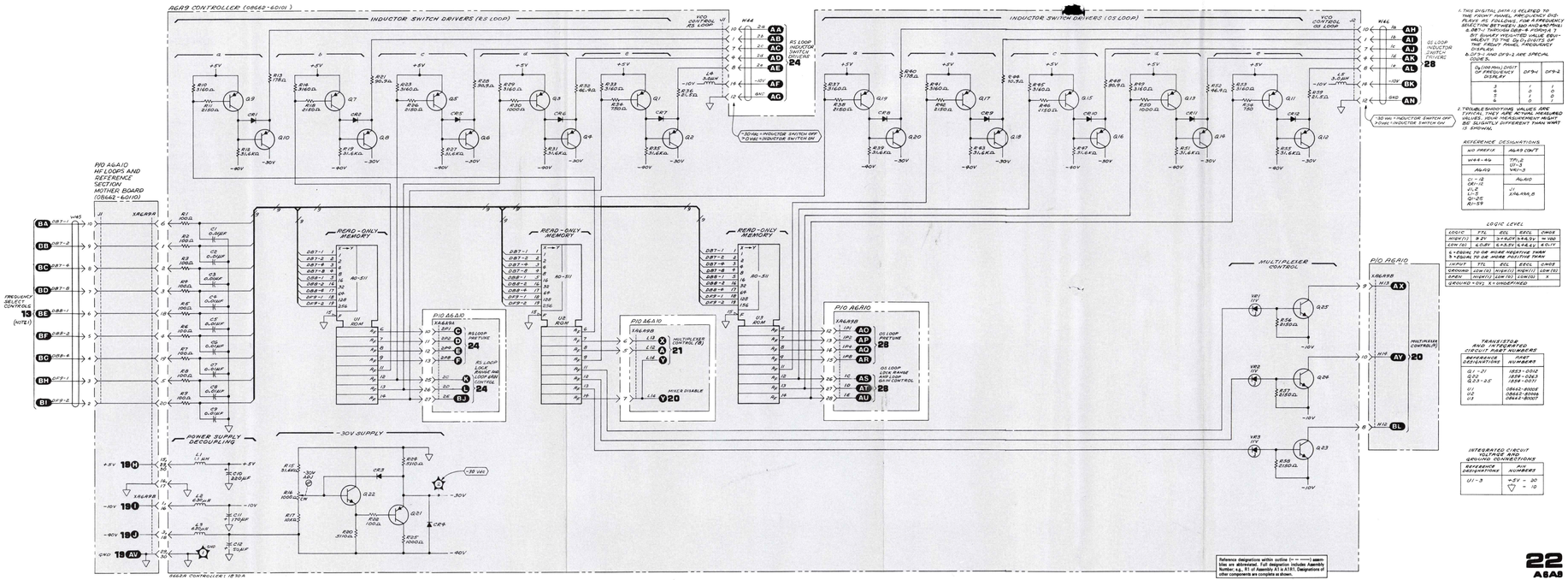


Figure 8-415. A6A9 High Frequency Loops and Reference Section Controller Schematic

SERVICE SHEET 23
A6A6 RF MIXER ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram D
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The RF Mixer Board contains circuitry that combines the 310 MHz to 620 MHz and 320 MHz to 640 MHz inputs to produce the 10 MHz or 20 MHz loop IF output. The two limiter stages serve as buffers and also provide a constant output level to the linear amplifier. Each limiter stage has a gain of about 10 dB and limits at approximately +1 dBm.

The output of limiter U2 is fed to the single stage common emitter amplifier (Q1), which has a gain of about 8 dB. The mixer is a double-balanced type (that is, both inputs are suppressed at the output). The output of the mixer contains the sum and difference frequencies of the two input signals at a power level of approximately −16 dBm. The sum signal is filtered by the 25 MHz low-pass filter, leaving only the desired difference signal at the output.

A6A6 ASSEMBLY

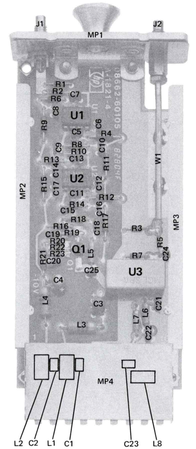
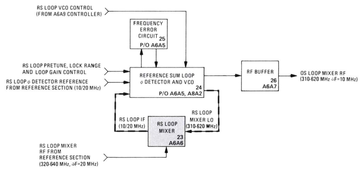


Figure 8-416. A6A6 Reference Sum Loop RF Mixer Component Locations



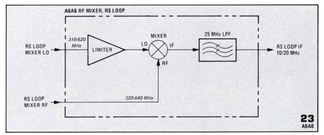


Figure 8-417. A6A6 Reference Sum Loop RF Mixer Block Diagrams

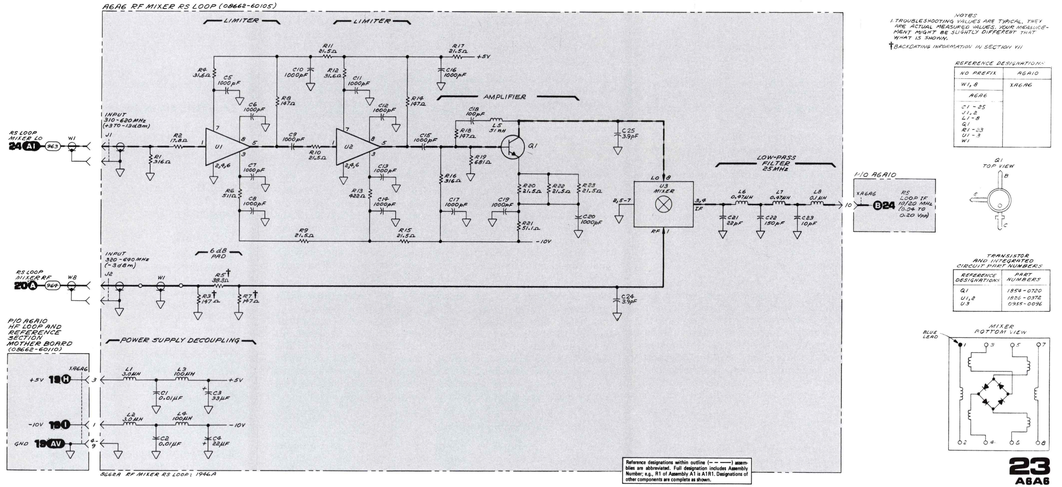


Figure 8-418. A6A6 Reference Sum Loop RF Mixer Schematic

SERVICE SHEET 24
P/O A6A5, A8A2 REFERENCE SUM LOOP PHASE DETECTOR AND VOLTAGE CONTROLLED OSCILLATOR ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram D
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The 10/20 MHz loop phase detector reference signal (at J1) and the 10/20 MHz loop IF signal (at board pin 1) are attenuated and amplified, respectively, and are sent to the phase detector formed by CR1, CR2, CR3, and CR4. The phase detector combines the two signals and outputs a difference signal which is filtered by a 5 MHz low-pass filter and a 19 MHz broadband notch filter before entering the integrator formed by Q7, Q8, and Q9.

The integrator output current is converted to voltage by Q10. This voltage is summed with a four-bit ROM-controlled BCD pretune current in the resistor-diode shaper. The resulting voltage is then filtered, buffered, and used to drive the VCO so that it produces linear tuning with constant loop gain.

The frequency range of the integrator voltage is automatically adjusted to maintain a constant lock range for the loop. The long time constants associated with switching the RC loop gain adjust are accelerated by the speed-up circuit during switching.

Loop Reference And IF Limiters

Before the 10/20 MHz loop IF (from the RF mixer) is compared against the 10/20 MHz loop phase detector reference frequency within the double-balanced phase detector, the two signals are passed through identical limiters. Prior to entering the limiters, the reference signal is attenuated by 3 dB and the IF signal is amplified by 8 dB so that the two signals have amplitudes of about −3 dBm to −5 dBm. The limiters have adequate gain at this input level to produce sharp limiting action over the 10 MHz to 20 MHz frequency range. The outputs of the limiters are connected to the inputs of center-tapped transformers T1 and T2. These transformers, together with four PN junction diodes, form the high level mixer/phase detector.

Phase Detector

A high level mixer is used as the phase detector on this board. Switching both sides of the phase detector hard generates a very linear slope. IF signals are suppressed by double-balanced action so that the main components at the output are dc phase and two times the IF signal. The two signals from the limiters and the phase detector output signal operate the lock acquisition circuitry.

Integrator

The phase detector's output signal passes through the 5 MHz low-pass filter and a 19 MHz notch filter. The signal which enters the integrator is either an ac difference frequency or a dc voltage (for signals of the same frequency). In this latter case, the dc varies between ± 0.6 volts.

The integrator has a large dc gain with a zero located at about 7 kHz. The loop locks at a 90° phase difference when the dc voltage reaches 0 volts. The integrator has only one driving input when the difference frequency is less than 200 kHz. This input comes from the 5 MHz low-pass filter. If the difference signal is greater than 200 kHz, an additional drive current (the primary driver at this point) is supplied by the out-of-lock circuitry.

The integrator's output is proportional to the charge across its feedback capacitor. The output level will be between 0 volts and some positive level determined by the lock range limit control and limit detector (set by the controller).

The integrator is actually a discrete component op-amp. It produces output voltages in 8 ranges. These 8 ranges accommodate the widely differing voltage-frequency sensitivity of the VCO caused as various combinations of inductors are switched into the VCO. Gain of the integrator is maximum at dc, but reaches unity between 250 kHz and 500 kHz. The high gain for close-in signals suppresses VCO noise.

Lock Range Limit Control And Out-Of-Lock Detector

As inductors in the VCO are switched ON in parallel, the VCOs sensitivity increases. As the VCO frequency is increased from 310 MHz to 640 MHz by progressively switching in inductors A, B, C, D, and E, the oscillators' gain increases by a factor of four (12 dB). To maintain constant lock range, the positive voltage swing of the integrator is limited by a 3-bit D/A converter controlled by the signals that switch inductors C, D, and E, the most significant frequency bits. The output of the D/A resistive ladder drives the out-of-lock circuitry.

The out-of-lock detector (U4) comparators the D/A output against the positive swing of the integrator. If the output becomes too positive, an out-of-lock signal is generated. Loss of signal or oscillator-drift, causing the integrator to reach its positive voltage limit, triggers this circuit and causes four things to happen. It lights the out-of-lock LED, sends TTL LO signals back through the motherboard to the microprocessor, enables the first dual CMOS switch and the two TTL trigger circuits, and enables the digital discriminator to clock the mixer beat note, producing a pulse-width modulated discriminator signal.

Resistor Diode Shaping Network

The VCO is controlled by varying the reverse bias on a group of varactor diodes which form part of the oscillator's tank circuit. An increase in reverse bias causes a reduction in junction capacitance, which increases the frequency. However, the frequency characteristic of the tuning circuit is not a linear function of input voltage.

A shaping circuit on the Phase Detector Board is used to linearize the signal. The shaping circuit consists of a ladder of diodes which are reverse biased at successively higher voltages. As the signal level increases, the diodes become progressively forward biased, presenting a lower impedance to the drive source. The tuning curve of the VCO is thus approximated by the shaping circuits in a piecewise linear manner.

4-Bit BCD Pretune

The beat note of the difference of the loop IF down-converted frequency and the reference frequency passes through a 7 MHz low-pass filter to remove the RF sum frequency and leave only the difference frequency. The pretune ensures that this difference frequency will be less than 7 MHz by pretuning within 7 MHz of its locked frequency. The pretune D/A converter is formed by quad comparator U13, JFET switches Q17-Q20, and associated circuitry. The RS loop pretune inputs accept TTL signals from the Controller Assembly (service sheet 29) to control the pretuning. The pretunes are weighted BCD currents of 0.63 mA, 1.25 mA, 2.50 mA and 5.00 mA. R85 allows the pretune currents to be scaled up or down by 7% and allows for minimization of dc offset. The collector of Q12 injects the pretune current into the resistor-diode shaper.

Loop Gain Adjust And Pretune (Speed-Up) Circuitry

The loop gain adjust circuit works on the same principle as the lock range circuit. VCO inductor lines C, D, and E control gates that activate the RC attenuator sections in the loop gain adjust circuit, ensuring that no phase shift occurs at the loop gain crossover frequency. Because of the low frequency and large capacitors, diodes CR29, CR30, CR31, and CR32 are used to speed up charging of these capacitors during switching. R95 and C49 keep loop gain as constant as possible with any combination of inductors A, B, C, D, and E switched on.

VCO (A8A2)

The VCO in the high frequency loop sections is a non-field-repairable assembly; it is sealed and can only be repaired at the factory. The VCO is coarsely tuned by a 5-bit code which switches inductors A, B, C, D, and E inside the VCO. A control voltage of −9 Vdc to −38 Vdc fine tunes the VCO to lock the loop. The output frequency of the VCO extends from 310 MHz to 620 MHz, at +3 dBm to −13 dBm (level depends on frequency).

TROUBLESHOOTING

When a high frequency loops problem has been traced through the block diagram troubleshooting procedure to this assembly, use the following procedure to isolate the cause of the problem.

1. Mount the A6A5 assembly on an extender board. Move the slide switch to the TEST position (up). This opens the loop.

2. Set the front panel frequency setting to 510.0 MHz. Connect a counter or spectrum analyzer to the A8A2 VCO output [disconnect cable W2 (965) from A6A7J1 and measure the signal at the end of the cable]. Connect the output of an adjustable power supply to A6A5TP14 (+) and A6A5TP1 (−).

3. Set the power supply output voltage to approximately 4 volts. The counter should read close to 510 MHz. Slowly decrease the power supply output to zero, and then increase the voltage to +8V. Check that the frequency changes as shown in the following table. Voltage and frequency readings may not be exactly as shown, but the amount and direction of change should be similar to these values.

Voltage applied to TP14 (V_{dc})	TP2(V_{dc})	VCO Frequency (MHz)
0.0	−14.3	504
4.0	−11.8	498
8.0	−9.9	492

If these readings are correct, continue troubleshooting with step 4. Otherwise, there is a problem from TP14 to TP2. Troubleshoot to find the cause.

4. Monitor TP8 with the high impedance input of a counter. The counter should read the difference signal from the phase detector. Vary the adjustable power supply so the VCO frequency varies above and below 500 MHz. The counter should read the absolute frequency error.

   If operation of this circuit is normal, continue troubleshooting with step 5. Otherwise, there is a problem with the phase detector circuitry.

5. Monitor TP7 (service sheet 25) with an oscilloscope or TTL logic probe. Vary the adjustable power supply so the VCO varies above and below 500 MHz. TP7 should be a TTL logic high (>2.4 Vdc) when the VCO is within 200 kHz of 500 MHz. At more than 500.2 and less than 499.2 MHz, TP7 should become a TTL logic low (< 0.8 Vdc).

   If operation of this circuit is normal, continue troubleshooting with step 6. Otherwise, there is a problem with the out-of-lock discriminator circuitry (bottom half of service sheet 25). Troubleshoot this circuitry to find the cause.

6. Monitor U3 pin 7 (service sheet 25) with a scope. Vary the adjustable power supply so the VCO is less than 499.7 MHz. The output of U3 should be less than 0.5 Vdc.

   Increase the VCO frequency to more than 500.3 MHz. The output of U3 should be more than 3.5 Vdc.

   If operation of this circuit is normal, continue troubleshooting with step 7. Otherwise, there is a problem with the frequency detector circuitry (top half of service sheet 25). Troubleshoot this circuitry to find the cause.

7. Monitor TP3 (service sheet 25) with an oscilloscope. Vary the adjustable power supply to increase the frequency of the VCO to more than 501.0 MHz. The signal at TP3 should be a dc level more negative than −3.0 Vdc. This level will become more negative as the RF output frequency increases.

   Decrease the frequency of the VCO to less than 499.0 MHz. The signal at TP3 should be a series of pulses with slow rise and fall times at about a +4 Vdc level. The level increases and the pulses get smaller as the RF output frequency decreases.

   If operation of this circuit is normal, continue troubleshooting with step 8. Otherwise, there is a problem with the CMOS switch (U7) or the circuitry that drives it. Troubleshoot this circuitry to find the cause.

8. Monitor TPA (output of integrator) with an oscilloscope. Vary the adjustable power supply to make the frequency of the VCO signal greater than 501.0 MHz. The waveform at TPA should be a dc level greater than +7.0 Vdc. Decrease the VCO frequency to less than 499.0 MHz. The waveform at TPA should be a dc level near ground. Pulse like those seen on TP3 may be visible on either of these levels.

   If these waveforms are not normal, there is a problem with the integrator circuitry.

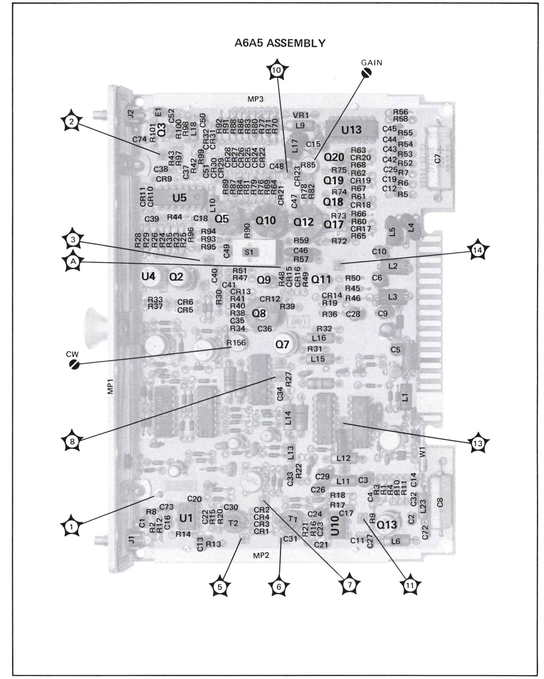


Figure 8-419. P/O A6A5 Reference Sum Loop Phase Detector Component Locations

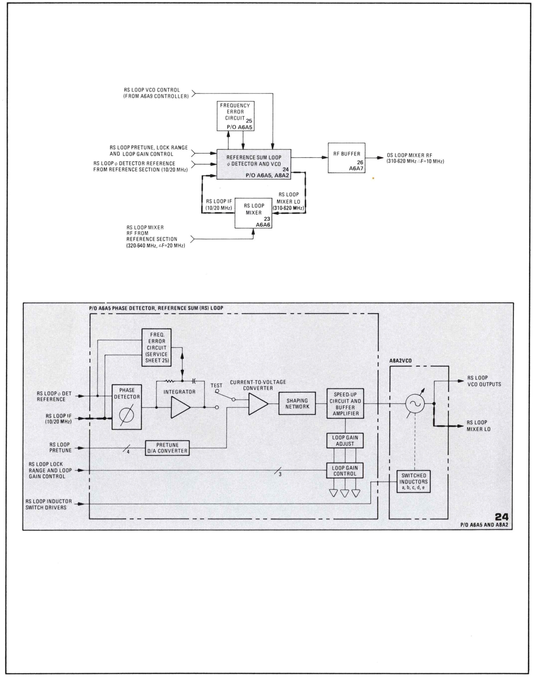


Figure 8-420. P/O A6A5 and A8A2 Reference Sum Loop Phase Detector and Voltage Controlled Oscillator Block Diagrams

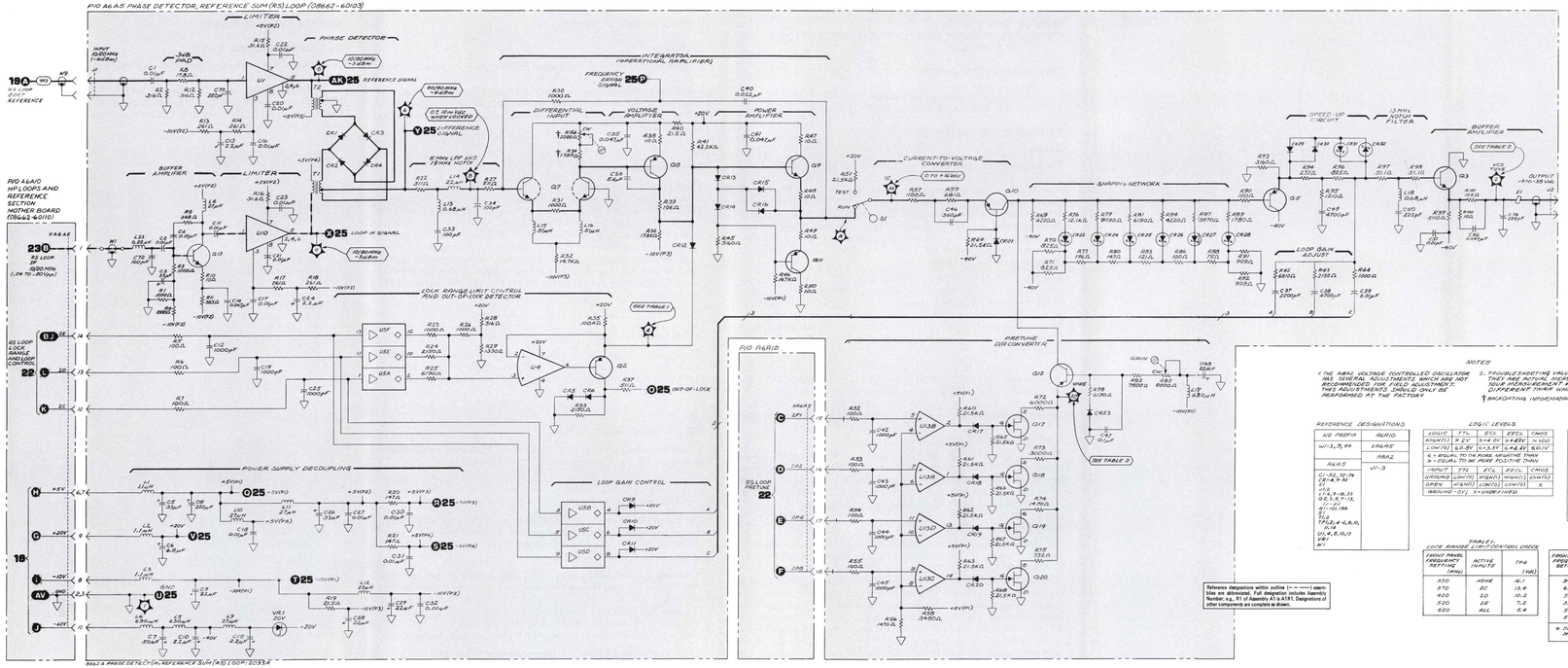


Figure 8-421. P/O A6A5 and A8A2 Reference Sum Loop Phase Detector and Voltage Controlled Oscillator Schematic

SERVICE SHEET 25
P/O A6A5 REFERENCE SUM LOOP PHASE DETECTOR ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram D
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The frequency error-correction circuitry on this board aids the phase lock loop (PLL) in acquiring lock. The first dual CMOS switch (U8) connects the outputs of the limiters to the trigger circuits. The trigger circuits produce TTL signals which are used by the ECL frequency detector when the loop is unlocked. These signals clock the frequency detector, which senses the direction of the frequency offset to determine whether the VCO (service sheet 24) should be driven up or down. The comparator produces a TTL logic level that controls the direction of the VCO frequency change.

The out-of-lock discriminator signal (pin 5 of U11) enables the digital discriminator to clock the mixer difference signal, producing a pulse-width modulated discriminator signal at the output of U12B. This signal is modulated at a frequency which varies from 200 kHz to 2.5 MHz. A resultant signal is generated, and one of the second dual CMOS switches (U7) is activated depending on the direction of the frequency offset.

If the loop is out of lock by more than 2.5 MHz, the correction current stays on continuously. From an offset of 2.5 MHz down to 200 kHz, the discriminator modulates the correction current. This speeds up switching time by a factor of two or three. Under 200 kHz the correction signals are not necessary and the lock acquisition circuitry is disabled.

Dual CMOS Switch No. 1 (U8)

This dual CMOS switch connects the reference and loop IF signal inputs to the TTL trigger circuits. The switch itself is controlled by the out-of-lock signal from the out-of-lock discriminator. It is disabled when the loops are locked, preventing the TTL trigger circuits from being clocked and reducing spurious loop mixer signals.

ECL Frequency Detector

The two output signals from dual CMOS switch No. 1 clock the ECL frequency detector (U2) producing a HI at either pin 4 or pin 11 of the device. A HI at one of the input pins 6 or 9 will produce a HI at the respective output pin. The output pin will remain HI until reset by a HI on the opposite input pin. It will again go HI with a HI input at its respective input and will reset the opposite output. Therefore, one of the output pins will be mostly HI (with some glitches) while the other will be LO (with some glitches). The output that is HI will depend upon which of the two frequencies is greater (that is, the direction of the frequency offset). The glitches are removed by the differential low-pass filter. When locked, the ECL frequency detector inputs are gated off by U9C and U9D and the two outputs end up in either a LO-HI, HI-LO or LO-LO state.

SERVICE SHEET 25 (Cont'd)

Comparator

Comparator U3 converts the filtered ECL frequency signal to a clean TTL logic level. This TTL level in turn controls whether the VCO (service sheet 32) is driven up or down. R141 provides a small amount of positive feedback around the comparator. This serves to suppress oscillation by producing a dead zone and latches the comparator when the loop is locked.

Programmable Inverter

The TTL frequency-direction logic level from the comparator is sent through an exclusive-or gate which acts as a programmable inverter. The RS loop requires a logic inversion here to drive the loop into lock if the VCO frequency is below that required. The OS loop requires no inversion for the feedback level to lock the loop when the frequency is above that of the reference. This is the only difference between the two loops. The state of the programmable inverter is set at pin 5 of the RS and OS loop boards. Pin 5 is allowed to float HI for the RS loop assembly (service sheet 25) and is tied LO for the OS loop assembly (service sheet 29).

7 MHz Low-Pass Filter

When the loop is out of lock, a beat note appears at the output of the mixer (service sheet 24). The 7 MHz low-pass filter removes the sum signal and other mixing products and only allows a beat note below 7 MHz to pass.

150 kHz Active High-Pass Filter

This circuit along with the dead zone in the TTL trigger circuit is used to prevent FM from triggering the out-of-lock circuitry.

Out-Of-Lock Discriminator

The out-of-lock signal (pin 5 of U11) enables the final stage of the digital discriminator and clocks the difference signal from the mixer. If the difference signal is greater than 200 kHz (< 5 μs) pin 5 of U11 will always be high, enabling one-shot U12B.

If the loop is out of lock by more than 2.5 MHz (< 400 ns) pin 12 of one-shot U12B will always be low enabling the dual-OR gates and current will be on continuously until the offset decreases to 2.5 MHz (400 ns). Between 2.5 MHz and 200 kHz U12B produces 400 ns pulses to modulate the correction current pumped into or out of the RC feedback node. As the offset decreases toward 200 kHz the pulse rate decreases.

When an offset of 200 kHz (5 μs) is reached, one-shot U12A and flip flop U11 disable one-shot U12B and the inputs to the ECL frequency detector. At this point the difference signal from the mixer is within the loop bandwidth and the loop will acquire lock by itself.

SERVICE SHEET 25 (Cont'd)

Dual CMOS Switch No. 2 (U7)

This circuit has one channel activated, depending on the out-of-lock direction of the VCO, by one of the two AND circuits being modulated by the discriminator signal. Thus, current is pumped into or out of the RC feedback node of the op-amp integrator (service sheet 24). This forces the output of the op-amp to ramp up or down in the correct direction toward lock.

A6A5 ASSEMBLY

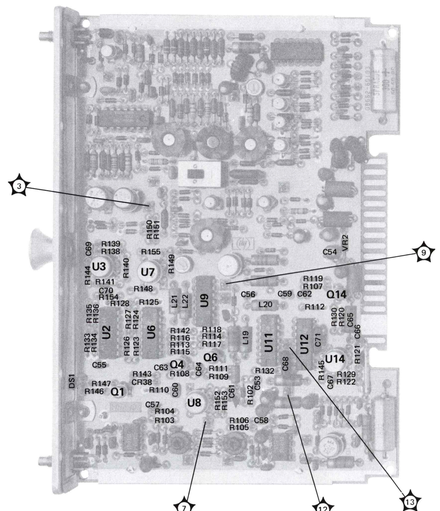
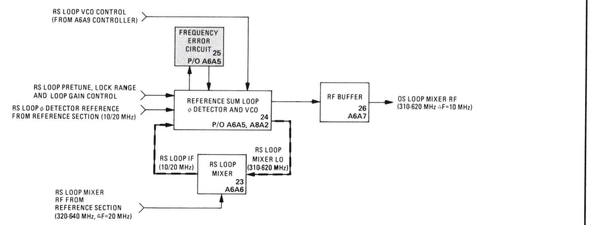


Figure 8-422. P/O A6A5 Reference Sum Loop Phase Detector Component Locations



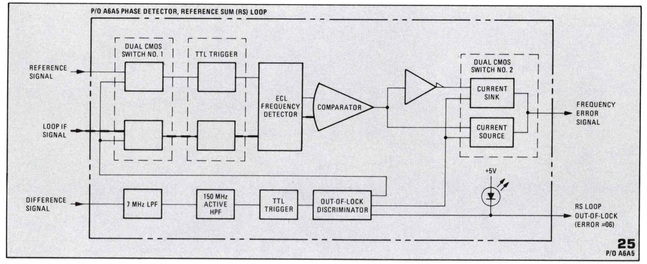


Figure 8-423. P/O A6A5 Reference Sum Loop Phase Detector Block Diagrams

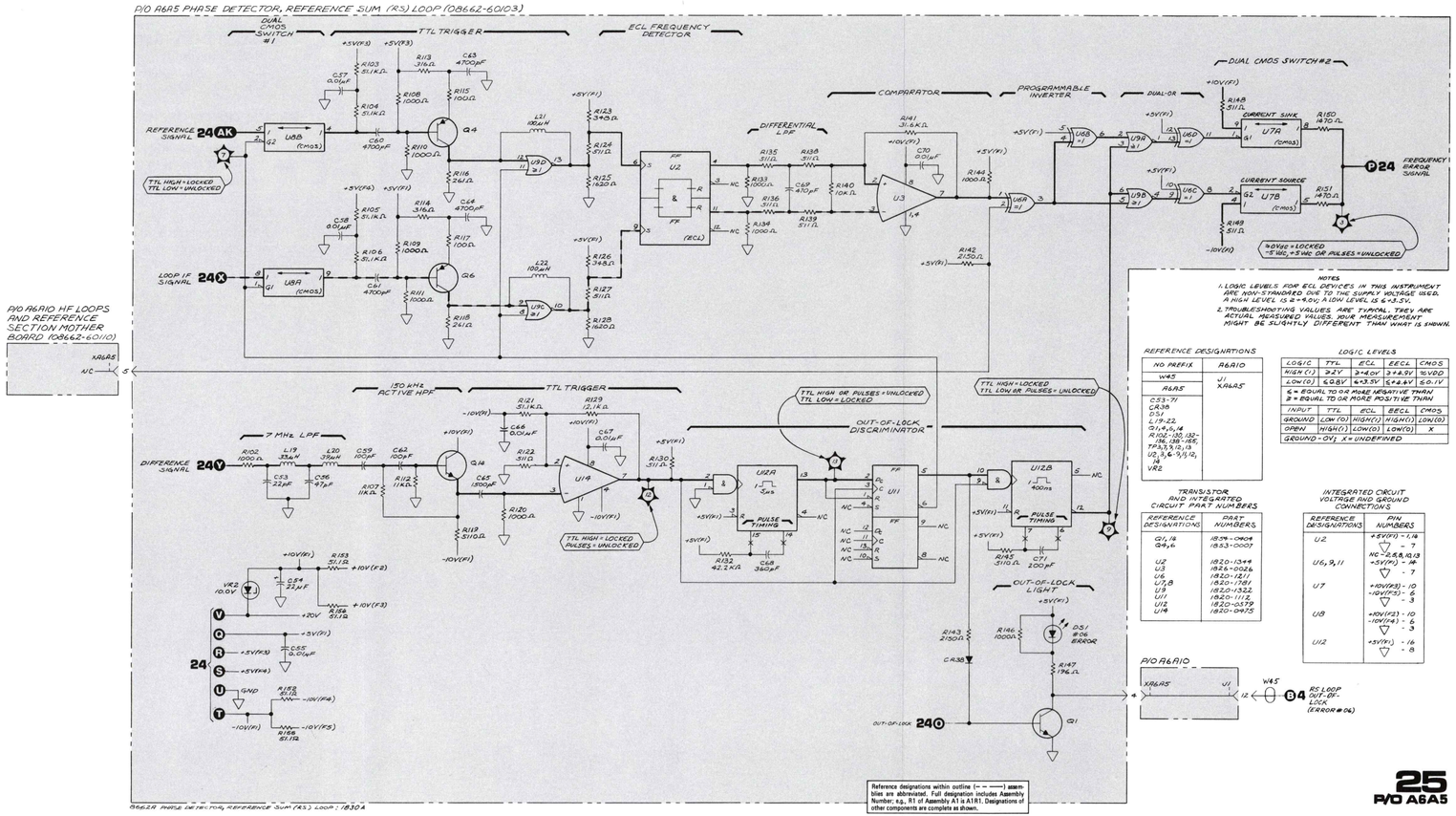


Figure 8-424. P/O A6A5 Reference Sum Loop Phase Detector Schematic

SERVICE SHEET 26
A6A7 RF BUFFER ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram D
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

The RF Buffer Assembly amplifies the 310 MHz to 620 MHz input signal before it is sent to the mixer in the Output Sum Loop. The RF Buffer consists of three limiter stages which provide gain and 75 dB of isolation. Each limiter stage has a gain of about 10 dB and limits at +1 dBm.

The output signal from limiter U3 is sent through a 700 MHz low-pass filter to minimize spurious signals. The level of the output signals from the RF buffer circuit varies from about −2 dBm to −5 dBm. This is due to the high frequency roll-off characteristic of the limiters and the insertion loss of the low-pass filter at higher frequencies.

P/O Reference Sum Loop
Phase Detector
A6A5
SERVICE SHEET 25

A6A7 ASSEMBLY

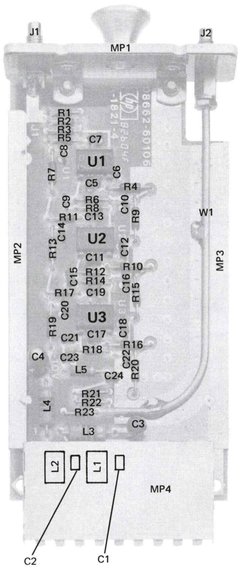


Figure 8-425. A6A7 RF Buffer Component Locations

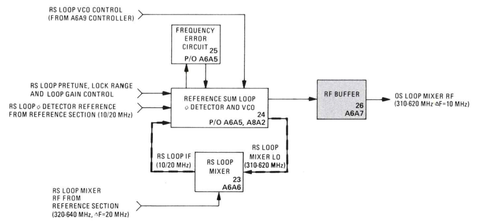


Figure 8-426. A6A7 RF Buffer Block Diagrams

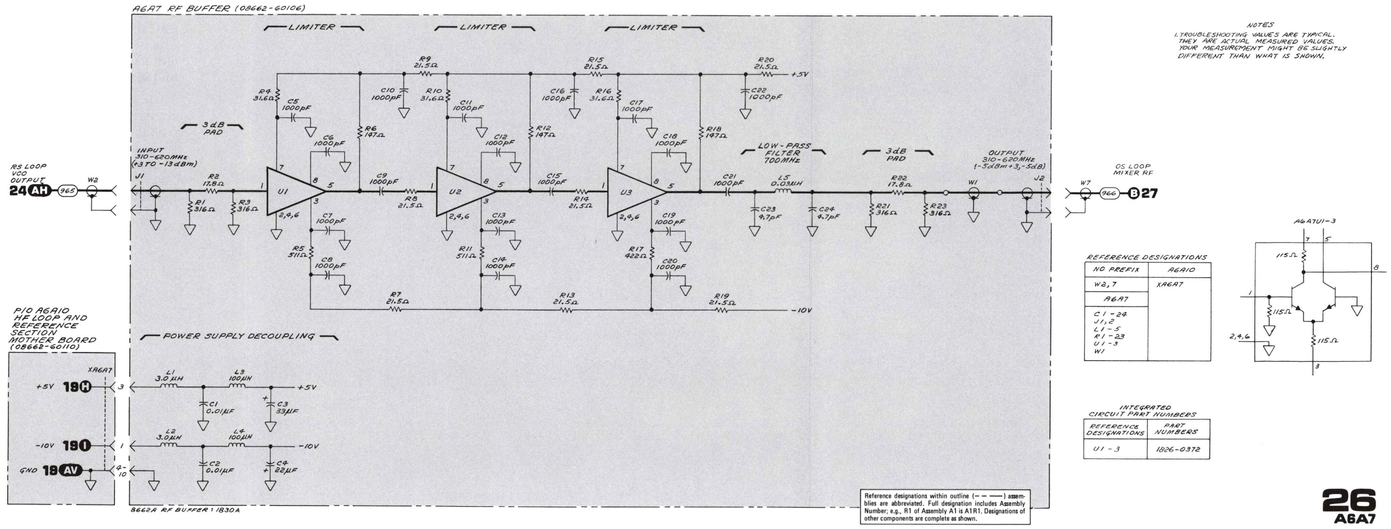


Figure 8-427. A6A7 RF Buffer Schematic

SERVICE SHEET 27
A6A8 RF MIXER ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram D
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

The RF Mixer combines the 310 MHz to 620 MHz and the 320 MHz to 640 MHz inputs to produce the 10 MHz to 20 MHz loop IF output signal. The two limiter stages serve as buffers and provide a constant level output to amplifier Q1. Each of the limiter stages has a gain of 10 dB and limits at +1 dBm.

The output of limiter U2 is amplified by the single stage common-emitter amplifier, which has an approximate gain of 8 dB. The mixer is a double-balanced type (that is, both input signals are suppressed at the output). The output of the mixer contains the sum and difference frequencies of the two input signals at a power level of approximately −16 dBm. The sum signal is filtered by the 25 MHz low-pass filter, leaving only the desired difference signal.

RF Buffer A6A7 SERVICE SHEET 26

A6A8 ASSEMBLY

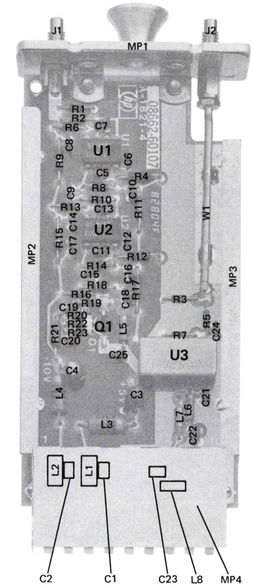
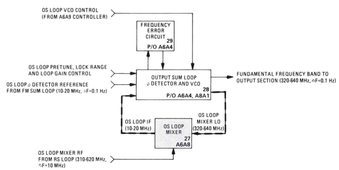


Figure 8-428. A6A8 Output Sum Loop RF Mixer Component Locations



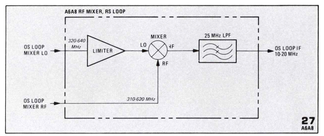
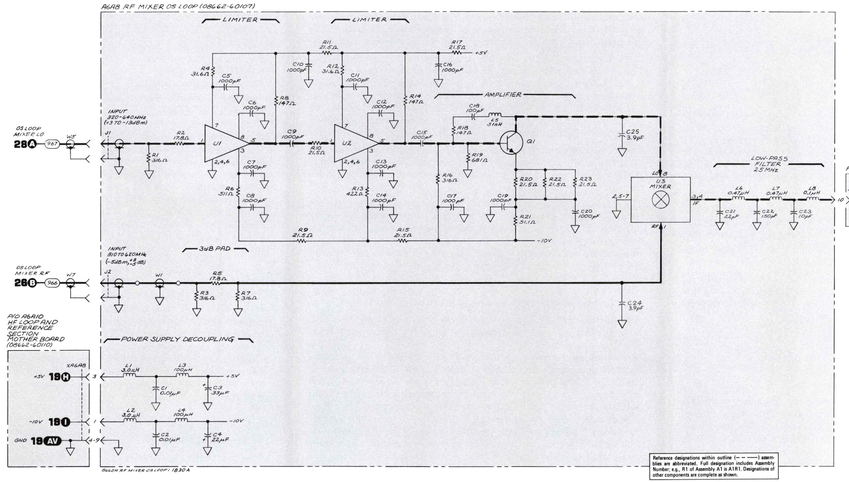


Figure 8-429. A6A8 Output Sum Loop RF Mixer Block Diagrams



NOTES:
1. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE INTENDED AS AN AID TO YOUR MEASUREMENTS AND MAY SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.

REFERENCE DESIGNATIONS

NO PREFIX	A6A10
W5,7	XA6A8
A6A8	
C1-25	
U1,2	
R1-8	
R1-23	
U1-3	
W1	

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATORS	PART NUMBERS
Q1	1854-0320
U1,2	1826-0372



27
A6A8

Figure 8-430. A6A8 Output Sum Loop RF Mixer Schematic

SERVICE SHEET 28
P/O A6A4, A8A1 OUTPUT SUM LOOP PHASE DETECTOR AND VOLTAGE CONTROLLED OSCILLATOR ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram D
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The 10/20 MHz loop phase detector reference signal (at J1) and the 10/20 MHz loop IF signal (at board pin 1) are attenuated and amplified, respectively, and are sent to the phase detector formed by CR1, CR2, CR3, and CR4. The phase detector combines the two signals and outputs a difference signal which is filtered by a 5 MHz low-pass filter and a 19 MHz broadband notch filter before entering the integrator formed by Q7, Q8, and Q9.

The integrator output current is converted to voltage by Q10. This voltage is summed with a four-bit ROM-controlled BCD pretune current in the resistor-diode shaper. The resulting voltage is then filtered, buffered, and used to drive the VCO so that it produces linear tuning with constant loop gain.

The frequency range of the integrator voltage is automatically adjusted to maintain a constant lock range for the loop. The long time constants associated with switching the RC loop gain adjust are accelerated by the speed-up circuit during switching.

Loop Reference And IF Limiters

Before the 10/20 MHz loop IF (from the RF mixer) is compared against the 10/20 MHz loop phase detector reference frequency within the double-balanced phase detector, the two signals are passed through identical limiters. Prior to entering the limiters, the reference signal is attenuated by 3 dB and the IF signal is amplified by 8 dB so that the two signals have amplitudes of about −3 dBm to −5 dBm. The limiters have adequate gain at this input level to produce sharp limiting action over the 10 MHz to 20 MHz frequency range. The outputs of the limiters are connected to the inputs of center-tapped transformers T1 and T2. These transformers, together with four PN junction diodes, form the high level mixer/phase detector.

Phase Detector

A high level mixer is used as the phase detector on this board. Switching both sides of the phase detector hard generates a very linear slope. IF signals are suppressed by double-balanced action so that the main components at the output are dc phase and two times the IF signal. The two signals from the limiters and the phase detector output signal operate the lock acquisition circuitry.

Integrator

The phase detector's output signal passes through the 5 MHz low-pass filter and a 19 MHz notch filter. The signal which enters the integrator is either an ac difference frequency or a dc voltage (for signals of the same frequency). In this latter case, the dc varies between ± 0.6 volts.

The integrator has a large dc gain with a zero located at about 7 kHz. The loop locks at a 90° phase difference when the dc voltage reaches 0 volts. The integrator has only one driving input when the difference frequency is less than 200 kHz. This input comes from the 5 MHz low-pass filter. If the difference signal is greater than 200 kHz, an additional drive current (the primary driver at this point) is supplied by the out-of-lock circuitry.

The integrator's output is proportional to the charge across its feedback capacitor. The output level will be between 0 volts and some positive level determined by the lock range limit control and limit detector (set by the controller).

The integrator is actually a discrete component op-amp. It produces output voltages in 8 ranges. These 8 ranges accommodate the widely differing voltage-frequency sensitivity of the VCO caused as various combinations of inductors are switched into the VCO. Gain of the integrator is maximum at dc, but reaches unity between 250 kHz and 500 kHz. The high gain for close-in signals suppresses VCO noise.

Lock Range Limit Control And Out-Of-Lock Detector

As inductors in the VCO are switched ON in parallel, the VCOs sensitivity increases. As the VCO frequency is increased from 310 MHz to 640 MHz by progressively switching in inductors A, B, C, D, and E, the oscillators' gain increases by a factor of four (12 dB). To maintain constant lock range, the positive voltage swing of the integrator is limited by a 3-bit D/A converter controlled by the signals that switch inductors C, D, and E, the most significant frequency bits. The output of the D/A resistive ladder drives the out-of-lock circuitry. The out-of-lock detector (U4) comparators the D/A output against the positive swing of the integrator. If the output becomes too positive, an out-of-lock signal is generated. Loss of signal or oscillator-drift, causing the integrator to reach its positive voltage limit, triggers this circuit and causes four things to happen. It lights the out-of-lock LED, sends TTL LO signals back through the motherboard to the, microprocessor, enables the first dual CMOS switch and the two TTL trigger circuits, and enables the digital discriminator to clock the mixer beat note, producing a pulse-width modulated discriminator signal.

Resistor Diode Shaping Network

The VCO is controlled by varying the reverse bias on a group of varactor diodes which form part of the oscillator's tank circuit. An increase in reverse bias causes a reduction in junction capacitance, which increases the frequency. However, the frequency characteristic of the tuning circuit is not a linear function of input voltage. A shaping circuit on the Phase Detector Board is used to linearize the signal. The shaping circuit consists of a ladder of diodes which are reverse biased

at successively higher voltages. As the signal level increases, the diodes become progressively forward biased, presenting a lower impedance to the drive source. The tuning curve of the VCO is thus approximated by the shaping circuits in a piecewise linear manner.

4-Bit BCD Pretune

The beat note of the difference of the loop IF down-converted frequency and the reference frequency passes through a 7 MHz low-pass filter to remove the RF sum frequency and leave only the difference frequency. The pretune ensures that this difference frequency will be less than 7 MHz by pretuning within 7 MHz of its locked frequency. The pretune D/A converter is formed by quad comparator U13, JFET switches Q17-Q20, and associated circuitry. The RS loop pretune inputs accept TTL signals from the Controller Assembly (service sheet 22) to control the pretuning. The pretunes are weighted BCD currents of 0.63 mA, 1.25 mA, 2.50 mA and 5.00 mA. R85 allows the pretune currents to be scaled up or down by 7% and allows for minimization of dc offset. The collector of Q12 injects the pretune current into the resistor-diode shaper.

Loop Gain Adjust And Pretune (Speedup) Circuitry

The loop gain adjust circuit works on the same principle as the lock range circuit. VCO inductor lines C, D, and E control gates that activate the RC attenuator sections in the loop gain adjust circuit, ensuring that no phase shift occurs at the loop gain crossover frequency. Because of the low frequency and large capacitors, diodes CR29, CR30, CR31, and CR32 are used to speed up charging of these capacitors during switching. R95 and C49 keep loop gain as constant as possible with any combination of inductors a, b, c, d, and e switched on.

VCO (A8A1 and A8A2)

The VCO in the high frequency loop sections is a non-field-repairable assembly; it is sealed and can only be repaired at the factory. The VCO is coarsely tuned by a 5-bit code which switches inductors a, b, c, d, and e inside the VCO. A control voltage of −9 Vdc to −38 Vdc fine tunes the VCO to lock the loop. The output frequency of the VCO extends from 310 MHz to 620 MHz, at +3 dBm to −13 dBm (level depends on frequency).

TROUBLESHOOTING

When a high frequency loops problem has been traced through the block diagram troubleshooting procedure to this assembly, use the following procedure to isolate the cause of the problem.

1. Mount the A6A4 assembly on an extender board. Move the slide switch to the TEST position (up). This opens the loop.

2. Set the front panel frequency setting to 510.0 MHz. Connect a counter to the front panel RF output of the Generator. Connect the output of an adjustable power supply to A6A4:
   + terminal to TP14
   − terminal to TP1 (ground)
3. Set the power supply output voltage to approximately 4 volts. The counter should read close to 510 MHz. Slowly decrease the power supply output to zero, and then increase the voltage to +8V. Check that the frequency changes as shown in the table, below. Voltage and frequency readings may not be exactly as shown, but the amount and direction of change should be similar to these values.

Voltage applied to TP14 (V_{dc})	TP2(V_{dc})	RF Output Frequency (MHz)
0	−21.7	516.0
4.0	−17.1	509.6
8.0	−13.8	503.5

   If these readings are correct, continue troubleshooting with step 4. Otherwise, there is a problem from TP14 to TP2. Troubleshoot to find the cause.
4. Monitor TP8 with the high impedance input of a counter. The counter should read the difference signal from the phase detector. Vary the adjustable power supply so the RF output frequency varies above and below 510 MHz. The counter should read the absolute frequency error.

   If operation of this circuit is normal, continue troubleshooting with step 5. Otherwise, there is a problem with the phase detector circuitry.
5. Monitor TP7 (service sheet 29) with an oscilloscope or TTL logic probe. Vary the adjustable power supply so the RF output varies above and below 510 MHz. TP7 should be a TTL logic high (>2.4 Vdc) when the RF output is within 200 kHz of 510 MHz. At more than 510.2 and less than 509.8 MHz, TP7 should become a TTL logic low (< 0.8 Vdc).

   If operation of this circuit is normal, continue troubleshooting with step 6. Otherwise, there is a problem with the out-of-lock discriminator circuitry (bottom half of service sheet 29). Troubleshoot this circuitry to find the cause.
6. Monitor U3 pin 7 (service sheet 29) with a scope. Vary the adjustable power supply so the RF output is more than 510.3 MHz. The output of U3 should be less than 0.5 Vdc.

   Decrease the RF output frequency to less than 509.7 MHz. The output of U3 should be more than 3.5 Vdc.

   If operation of this circuit is normal, continue troubleshooting with step 7. Otherwise, there is a problem with the frequency detector circuitry (top half of service sheet 29). Troubleshoot this circuitry to find the cause.

7. Monitor TP3 (service sheet 29) with an oscilloscope. Vary the adjustable power supply to increase the frequency of the RF output to more than 511.0 MHz. The signal at TP3 should be a dc level more negative than −3.0 Vdc. This level will become more negative as the RF output frequency increases.

   Decrease the frequency of the RF output to less than 509.0 MHz. The signal at TP3 should be a series of pulses with slow rise and fall times at about a +4 Vdc level. The level increases and the pulses get smaller as the RF output frequency decreases.

   If operation of this circuit is normal, continue troubleshooting with step 8. Otherwise, there is a problem with the CMOS switch (U7) or the circuitry that drives it. Troubleshoot this circuitry to find the cause.
8. Monitor TPA (output of integrator) with an oscilloscope. Vary the adjustable power supply to make the frequency of the RF output signal greater than 511.0 MHz. The waveform at TPA should be a dc level greater than +7.0 Vdc. Decrease the RF output frequency to less than 509.0 MHz. The waveform at TPA should be a dc level near ground. Pulses like those seen on TP3 may be visible on either of these levels.

   If these waveforms are not normal, there is a problem with the integrator circuitry.

Output Sum Loop RF Mixer A6A8 SERVICE SHEET 27

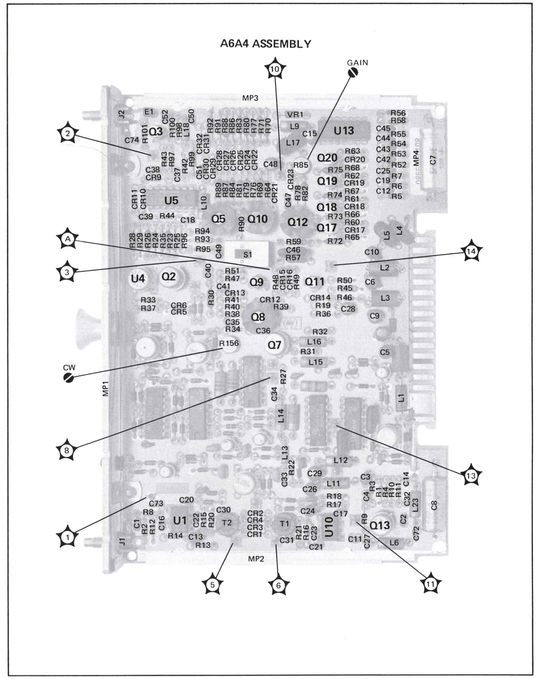


Figure 8-431. P/O A6A4 Output Sum Loop Phase Detector Component Locations

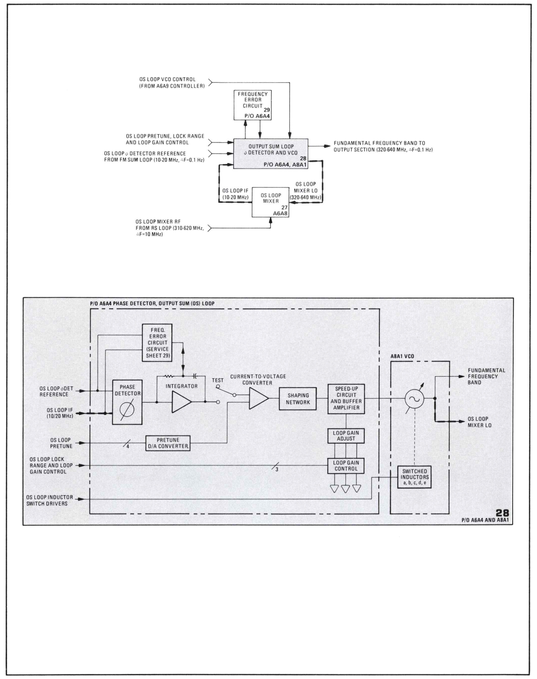


Figure 8-432. P/O A6A4 and A8A1 Output Sum Loop Phase Detector and Voltage Controlled Oscillator Block Diagrams

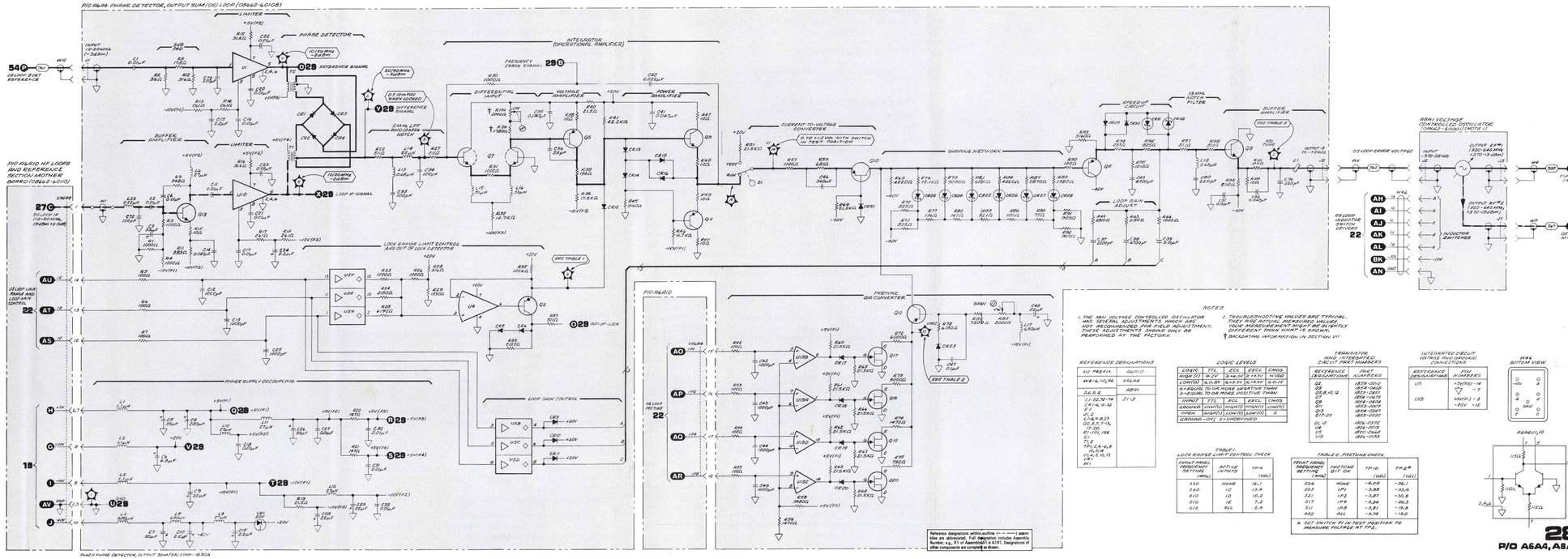


Figure 8-433. P/O A6A4 and A8A1 Output Sum Loop Phase Detector and Voltage Controlled Oscillator Schematic

SERVICE SHEET 29
P/O A6A4 OUTPUT SUM LOOP PHASE DETECTOR ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram D
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The frequency error-correction circuitry on this board aids the phase lock loop (PLL) in acquiring lock. The first dual CMOS switch (U8) connects the outputs of the limiters to the trigger circuits. The trigger circuits produce TTL signals which are used by the ECL frequency detector when the loop is unlocked. These signals clock the frequency detector, which senses the direction of the frequency offset to determine whether the VCO (service sheet 28) should be driven up or down. The comparator produces a TTL logic level that controls the direction of the VCO frequency change.

The out-of-lock discriminator signal (pin 5 of U11) enables the digital discriminator to clock the mixer difference signal, producing a pulse-width modulated discriminator signal at the output of U12B. This signal is modulated by a frequency which varies from 200 kHz to 2.5 MHz. A resultant signal is generated, and one of the second dual CMOS switches (U7) is activated depending on the direction of the frequency offset.

If the loop is out of lock by more than 2.5 MHz (400 ns), the correction current stays on continuously. From an offset of 2.5 MHz down to 200 kHz, the discriminator modulates the correction current. This speeds up switching time by a factor of two or three. Under 200 kHz (5 μs) the correction signals are not necessary and the lock acquisition circuitry is disabled.

Dual CMOS Switch No. 1 (U8)

This dual CMOS switch connects the reference and loop IF signal inputs to the TTL trigger circuits. The switch itself is controlled by the out-of-lock signal from the out-of-lock discriminator. It is disabled when the loops are locked, preventing the TTL trigger circuits from being clocked and reducing spurious loop mixer signals.

ECL Frequency Detector

The two output signals from dual CMOS switch No. 1 clock the ECL frequency detector (U2) producing a HI at either pin 4 or pin 11 of the device. A HI at one of the input pins 6 or 9 will produce a HI at the respective output pin. The output pin will remain HI until reset by a HI on the opposite input pin. It will again go HI with a HI input at its respective input and will reset the opposite output. Therefore, one of the output pins will be mostly HI (with some glitches) while the other will be LO (with some glitches). The output that is HI will depend upon which of the two frequencies is greater (that is, the direction of the frequency offset). The glitches are removed by the differential low-pass filter.

SERVICE SHEET 29 (Cont'd)

When locked, the ECL frequency detector inputs are gated off by U9C and U9D and the two outputs end up in either a LO-HI, HI-LO or LO-LO state.

Comparator

Comparator U3 converts the filtered ECL frequency signal to a clean TTL logic level. This TTL level in turn controls whether the VCO (service sheet 36) is driven up or down. R141 provides a small amount of positive feedback around the comparator. This serves to suppress oscillation by producing a dead zone and latches the comparator when the loop is locked.

Programmable Inverter

The TTL frequency-direction logic level from the comparator is sent through an exclusive-or gate which acts as a programmable inverter. The RS loop requires a logic inversion here to drive the loop into lock if the VCO frequency is below that required. The OS loop requires no inversion for the feedback level to lock the loop when the frequency is above that of the reference. This is the only difference between the two loops. The state of the programmable inverter is set at pin 5 of the RS and OS loop boards. Pin 5 is allowed to float HI for the RS loop assembly (service sheet 33) and is tied LO for the OS loop assembly (service sheet 37).

7 MHz Low-Pass Filter

When the loop is out of lock, a beat note appears at the output of the mixer (service sheet 32). The 7 MHz low-pass filter removes the sum signal and other mixing products and only allows a beat note below 7 MHz to pass.

150 kHz Active High-Pass Filter

This circuit along with the dead zone in the TTL trigger circuit is used to prevent FM from triggering the out-of-lock circuitry.

Out-Of-Lock Discriminator

The out-of-lock signal (pin 5 of U11) enables the final stage of the digital discriminator and clocks the difference signal from the mixer. If the difference signal is greater than 200 kHz (< 5 μs) pin 5 of U11 will always be high, enabling one-shot U12B.

If the loop is out of lock by more than 2.5 MHz (< 400 ns) pin 12 of one-shot U12B will always be low enabling the dual-OR gates and current will be on continuously until the offset decreases to 2.5 MHz (400 ns). Between 2.5 MHz and 200 kHz U12B produces 400 ns pulses to modulate the correction current pumped into or out of the RC feedback node. As the offset decreases toward 200 kHz the pulse rate decreases.

SERVICE SHEET 29 (Cont'd)

When an offset of 200 kHz (5 μs) is reached, one-shot U12A and flip flop U11 disable one-shot U12B and the inputs to the ECL frequency detector. At this point the difference signal from the mixer is within the loop bandwidth and the loop will acquire lock by itself.

Dual CMOS Switch No. 2 (U7)

This circuit has one channel activated, depending on the out-of-lock direction of the VCO, by one of the two AND circuits being modulated by the discriminator signal. Thus, current is pumped into or out of the RC feedback node of the op-amp integrator (service sheet 28). This forces the output of the op-amp to ramp up or down in the correct direction toward lock.

A6A4 ASSEMBLY

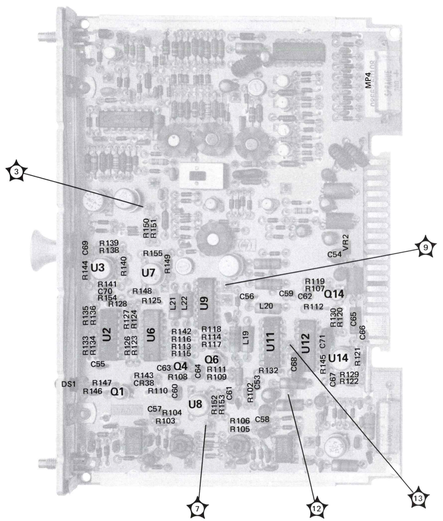


Figure 8-434. P/O A6A4 Output Sum Loop Phase Detector Component Locations

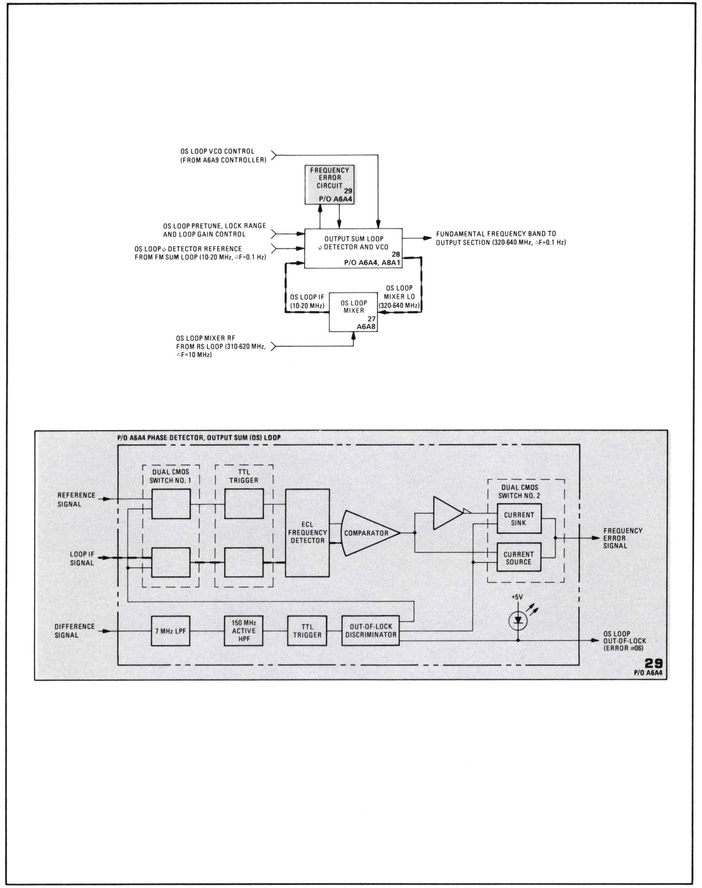


Figure 8-435. P/O A6A4 Output Sum Loop Phase Detector Block Diagrams

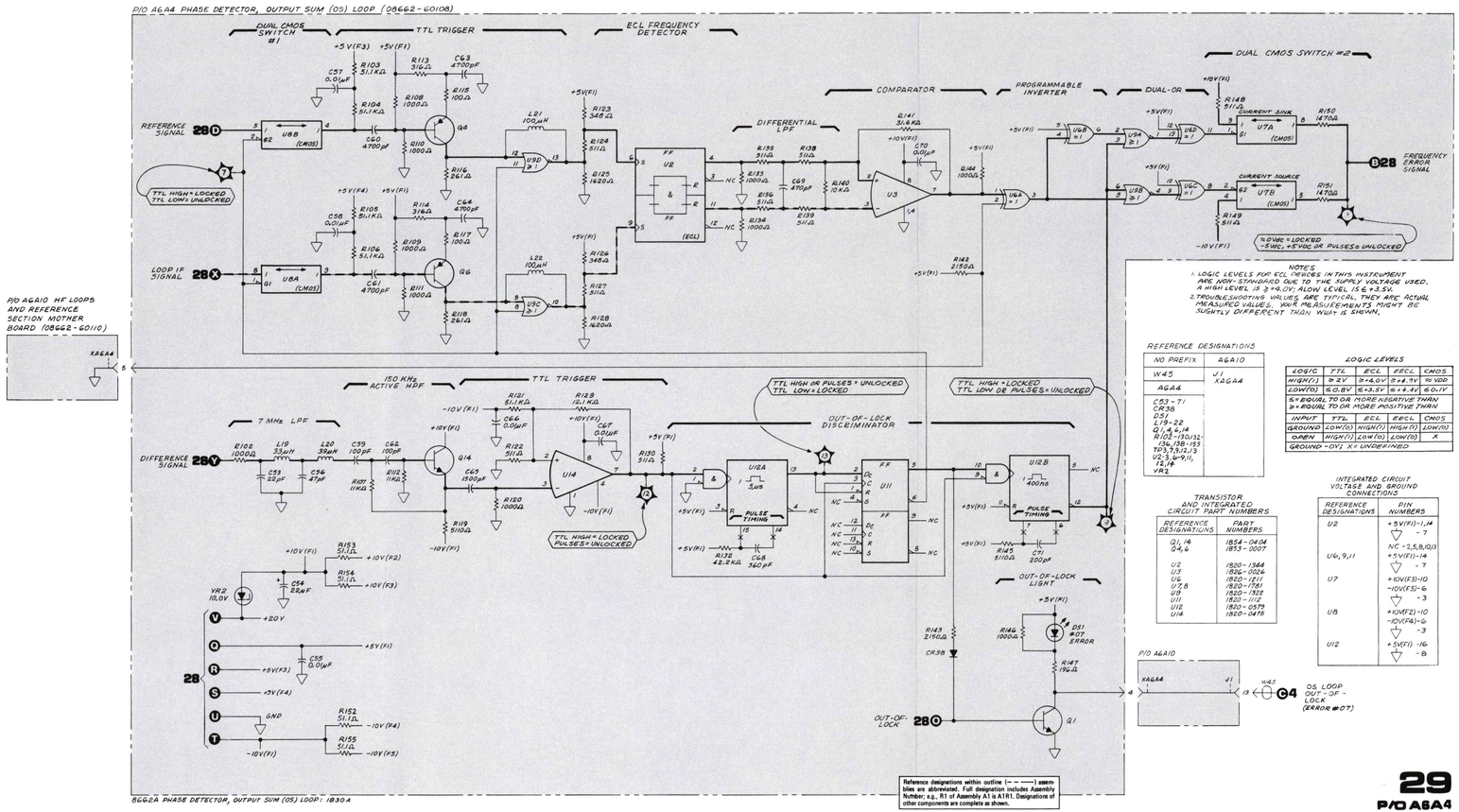


Figure 8-436. P/O A6A4 Output Sum Loop Phase Detector Schematic



Printed in U.S.A.

SERVICE MANUAL

8662A Synthesized Signal Generator

10 kHz — 1280 MHz



P/O Section VIII
Service Sheets

30-40

Output Section
Modulation Section

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HEWLETT PACKARD

SERVICE SHEET 30
A4A4 DISTRIBUTOR BOARD

TROUBLESHOOTING HELP

Block Diagram E
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The Distributor board converts the basic (fundamental) frequency band at the output of the high frequency section (320 MHz to 640 MHz at 0 dBm to −16 dBm) for use by the doubler band, down-converter band, and midband circuits. The three frequency inputs to these circuits are 320 MHz to 640 MHz, 520.01 MHz to 640 MHz, and 120 MHz to 640 MHz, respectively.

Limiters

The fundamental frequency band signal (320 MHz to 640 MHz in 0.1 Hz steps) enters the output section at J1 and passes through two cascaded limiter sections which provide gain and limiting. The limiters are ECL devices. Each has a gain of approximately 10 dB and limits at +1 dBm. There are two outputs from the second limiter (U2); one is inverted and one is non-inverted.

Dividers, Low-Pass Filters, and Control Circuitry

The non-inverted output of U2 is routed through two low-pass filters. One is a 640 MHz 7-pole low-pass filter; the other is a 460 MHz 5-pole low-pass filter. The filters are selected one at a time by PIN diodes CR1, CR2, CR6, and CR10. The diodes are enabled by lines LF4 and LF5. The filter to be selected is determined by ROM U8, which is addressed by lines RØ through R4 from the DCU.

The second output from U2 is used to drive the input of U3, a divide-by-two flip flop. U3 is enabled and disabled via pin 12; U3 is not enabled unless the Generator is operating in one of the divider bands. The output of U3 drives the 240 MHz and 340 MHz low-pass filters. These filters are switched in and out of the circuit by lines LF2 and LF3 from U8. The output of the divide-by-two circuit formed by U4 drives the 180 MHz low-pass filter. U4 is turned on and off by pin 12, by way of signals from U8 and U9. Only one of the filter bands is on at any given time. The output of the filters is usually −5 dBm to −8 dBm, nominal.

Amplifier Stages

There are two amplifier stages. The first stage (formed by Q5) provides 3 dB of gain. The second amplifier (formed by U6) has a gain of 11 dB.

Loop Gain Amplifier (AGC)—Local Leveling

The purpose of the AGC loop is to regulate any ripples caused by the dividers, limiters, switching circuits, or filters. These amplitude ripples may be as great as 3 dB peak to peak. The modulator for the AGC loop consists of PIN diodes CR11 and CR13. The more current that flows through R33 and R45, the lower the impedance of the PIN diodes.

Lower impedance results in lower insertion loss, causing more signal to be passed.

The AGC loop sensor is formed by peak detector diode CR14; C49 is a bypass capacitor. The loop comparator and driver is formed by U5B; C46 is an integrating capacitor. The reference voltage for the loop is formed by R42 and R40. This voltage is compared to the voltage from the divider formed by CR14 and R46. AGC action forces the voltage at the cathode of CR14 to be fixed, establishing U5B as a voltage source. CR12 is a temperature compensation diode.

R49 (51.1Ω) is inserted at the output of the +11 dB amplifier and acts to match the local leveling circuitry to a 50Ω system. The output signal's frequency range is 120 MHz to 640 MHz at +1.5 dBm (±0.5 dB).

Output Multiplexor Switching

Switching for the three-way output multiplexor is controlled by CR16, CR17, and CR18. As in the low-pass filter section, only one channel of the multiplexor is on at any given time. Signals from U8 control switching in the same manner that switching is controlled in the low-pass filter section. The J2 output is the 320 MHz to 640 MHz (+1.75 dBm) doubler band source. The J3 output is the 520.01 MHz to 640 MHz (+1.75 dBm) down converter source. The J4 output is the 120 MHz to 640 MHz (+1.0 dBm) midband source. CR19 and CR20 provide increased isolation against spurious signals when switched in by the control circuitry. When J4 is not

SERVICE SHEET 30 (Cont'd)

selected, these PIN diodes help to attenuate the output by more than 40 dB.

Error Detector

The error detector verifies that the Distributor Board is functioning correctly by monitoring the output power levels. U5A senses the output of peak detector diode CR14 and compares it against a fixed voltage. If the signal level is incorrect, the microprocessor is signalled and error lamp DS1 is turned on. VR1 insures that one of the output switches is conducting at all times.

NOTE

An invalid ROM input will cause none of the output multiplexor channels to be selected, thus causing an error indication.

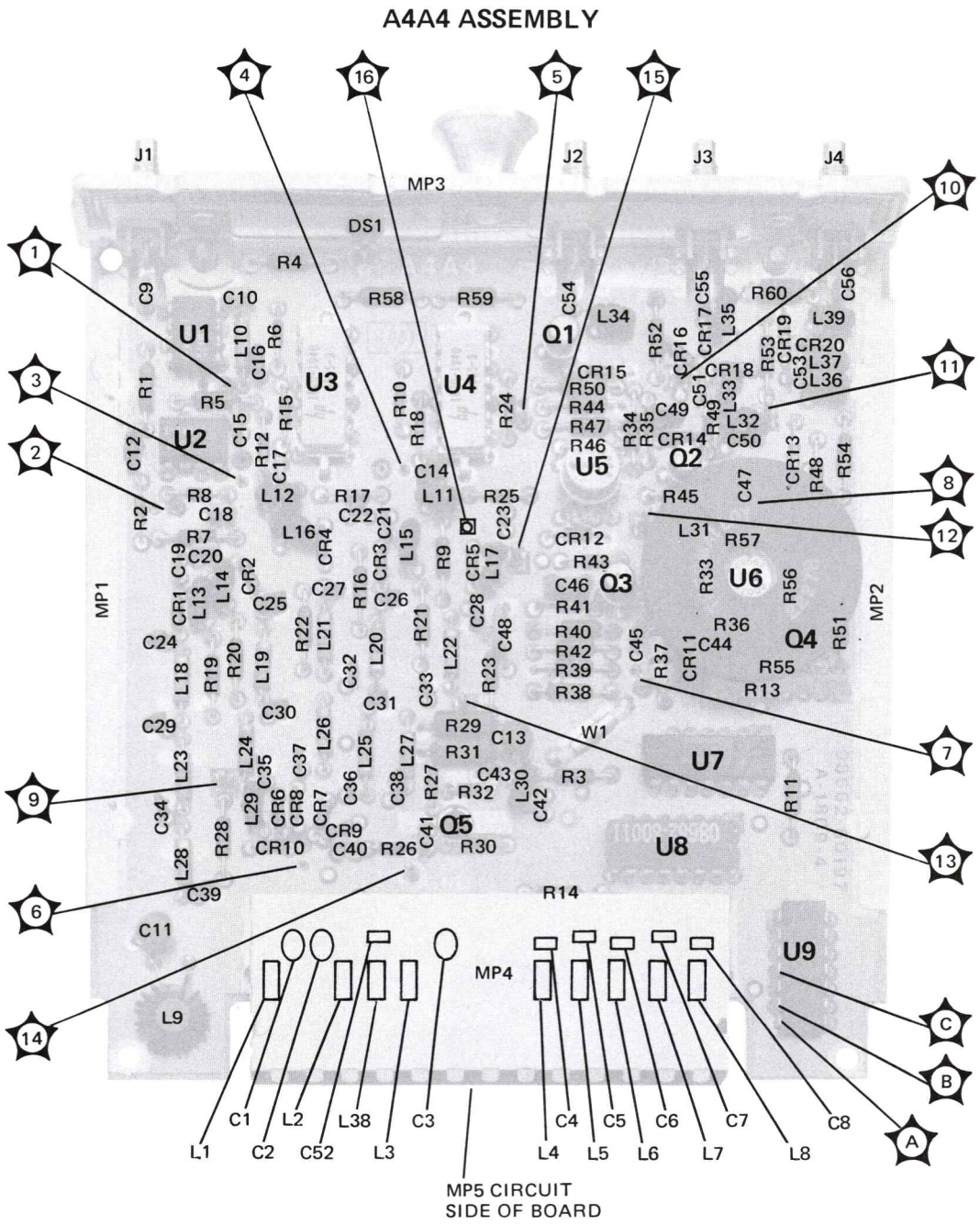


Figure 8-501. A4A4 Output Section Distributor Component Locations

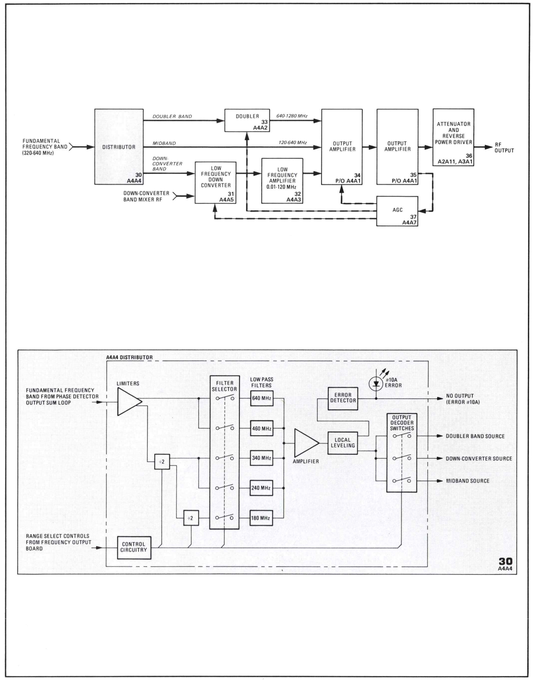


Figure 8-502. A4A4 Output Section Distributor Block Diagrams

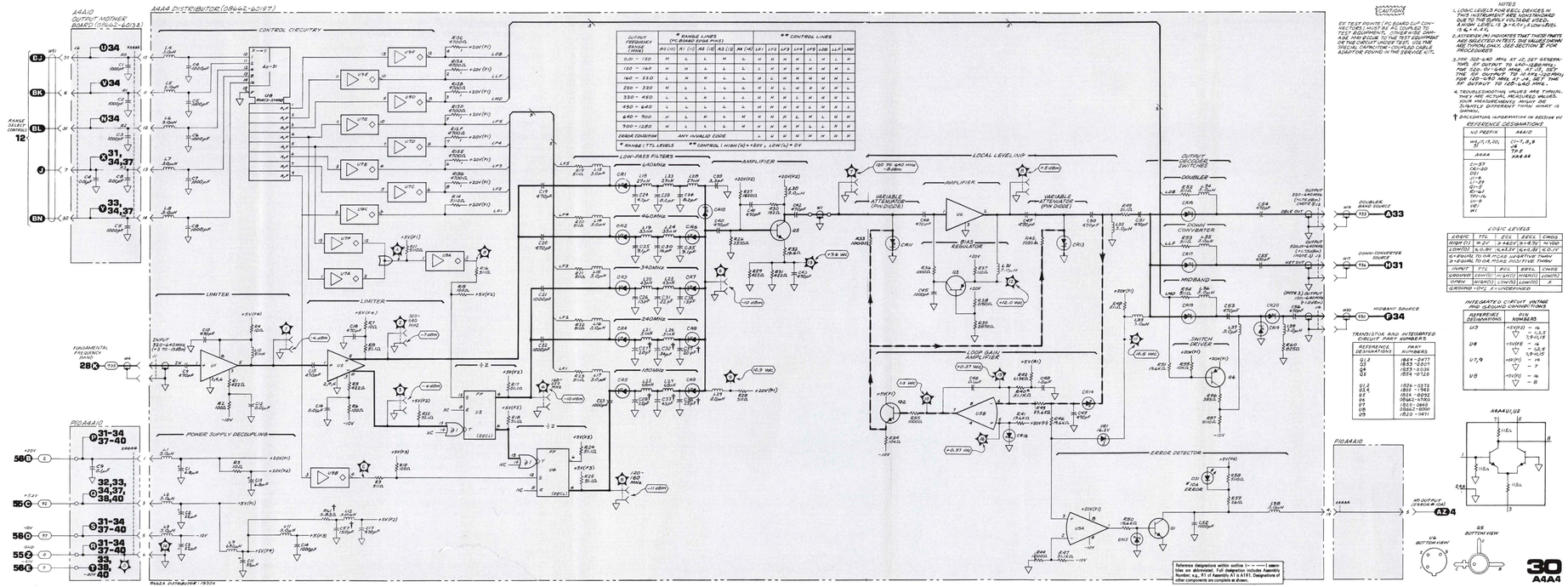


Figure 8-503. A4A4 Output Section Distributor Schematic

SERVICE SHEET 31
A4A5 LOW FREQUENCY DOWN CONVERTER BOARD

TROUBLESHOOTING HELP

Block Diagram E
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The Low Frequency Down Converter Board generates the 10 kHz to 120 MHz low frequency RF band. It does this by mixing the 520.01 MHz to 640 MHz down converter source signal from the Distributor Board (service sheet 30) with the 520 MHz down converter band mixer RF from the reference section.

The 520.01 MHz to 640 MHz down converter source signals from the distributor enter the Down Converter Board by way of J1. This signal is boosted from +1.75 dBm to approximately +11 dBm by microcircuit amplifier U1. The signal is then coupled, via C14, to a narrow-band tuned amplifier formed by Q2. Tuning is accomplished by variable capacitor C16 in conjunction with L9. The gain of this stage is approximately 10 dB, boosting the signal to +20 dBm.

The 680 MHz low-pass filter reduces harmonics present in the output to 40 dB below signal level. The 3 dB pad attenuates the signal output to +17 dBm and creates a better broadband match to the LO input of the mixer.

The 520 MHz input from the reference section enters the Down Converter Board via the J3 input at +1 dBm. To compensate for the insertion loss of the AM modulator, the signal is amplified to +10 dBm by the +9 dB amplifier formed by Q6. This amplifier is biased from the negative supply.

PIN Modulator

The PIN diode AM modulator formed by CR1, CR2, CR3, and CR4, modulates the 520 MHz input signal with the signal from the AGC Board (service sheet 37). The AGC signal enters the Down Converter Board via pin 9 and is injected between CR2 and CR3. The signal splits and goes through both the right and left set of diodes. The more current that flows in the line, the lower the impedance of the diodes. This results in lower insertion loss and a greater amplitude output signal.

Following modulation, the signal is amplified by the +9 dB amplifier formed by Q5. The output of this amplifier is approximately −5 dBm. The signal then passes through a 680 MHz low-pass filter and a 3 dB pad, and is fed into the RF input of the mixer (U2) at approximately −8 dBm.

Mixer

The mixer takes the 520.01 MHz to 640 MHz down converter source signal and hetrodynes it with the 520 MHz reference RF to produce the 10 kHz to 120 MHz low level down converter band. The 25 dB difference between the LO and RF inputs of the mixer is necessary to reduce the effect of spurs. If the difference is greater than 25 dB, the signal will

SERVICE SHEET 31 (Cont'd)

become buried in noise. Part of the effect of the AGC loop is to ensure that the mixer operates within the 25 dB range.

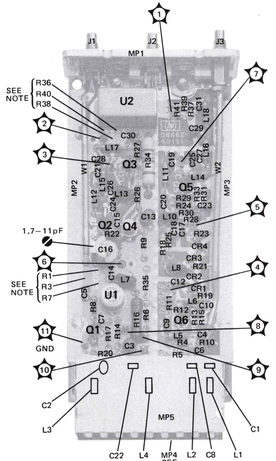
The output of the mixer is about −16 dBm. Before being sent to the output amplifier stages, it is amplified by the Low Frequency Preamplifier (service sheet 32).

Bias Regulators and Down Converter Enable

The bias regulators for the two down converter source amplifiers are formed by Q3 and Q4. The down converter enable line from the Distributor Board (service sheet 30) is used to switch the Down Converter Board ON and OFF through transistor Q4, which is the ground source for the bias regulators.

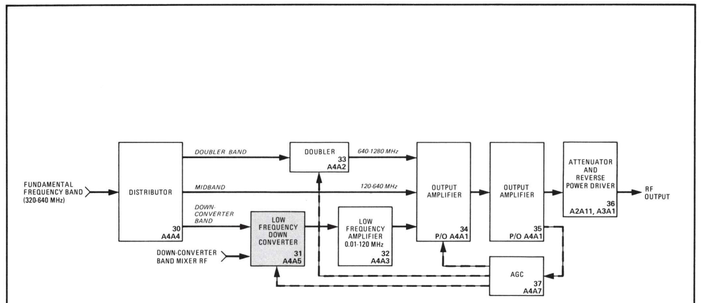
Output Section Distributor A4A4 SERVICE SHEET 30

A4A5 ASSEMBLY



NOTE: R1, 3, 7, 36, 38, 40 AND MP4 ARE ON CIRCUIT SIDE OF BOARD

Figure 8-504. A4A5 Output Section LF Down Converter Component Locations



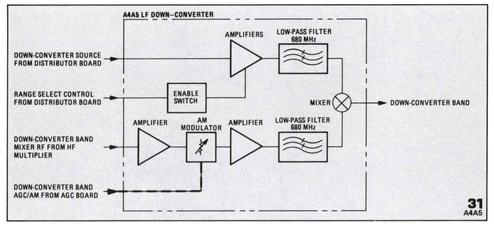
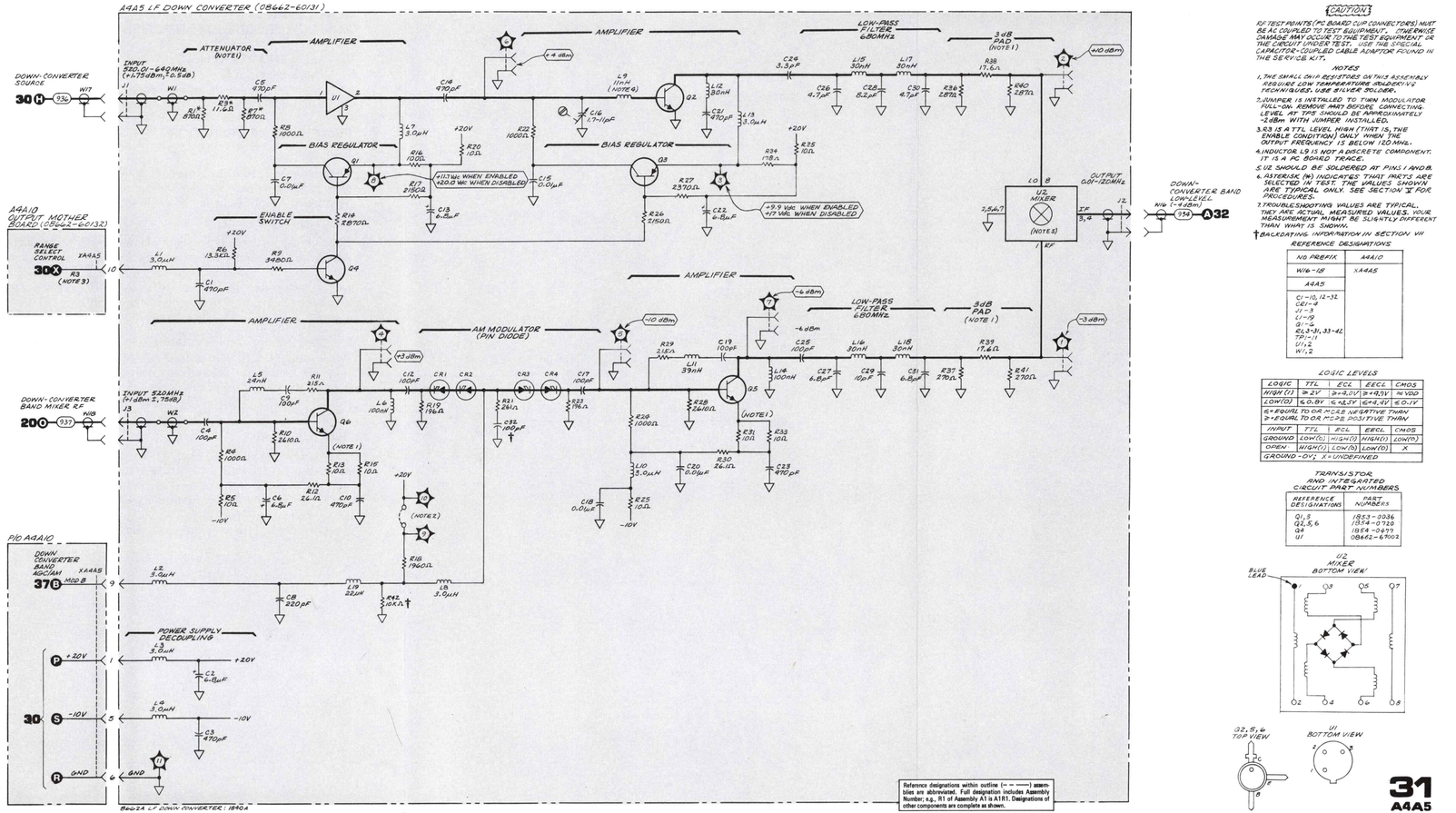


Figure 8-505. A4A5 Output Section LF Down Converter Block Diagrams



CAUTION

RF TEST POINTS (PC BOARD CUP CONNECTORS) MUST BE AC COUPLED TO TEST EQUIPMENT. OTHERWISE DAMAGE MAY OCCUR TO THE TEST EQUIPMENT OR THE CIRCUIT UNDER TEST. USE THE SPECIAL CAPACITOR-COUPLED CABLE ADAPTOR FOUND IN THE SERVICE KIT.

NOTES

1. THE SMALL CHIP RESISTORS ON THIS ASSEMBLY REQUIRE LOW TEMPERATURE SOLDERING TECHNIQUES. USE SILVER SOLDER.
2. JUMPER IS INSTALLED TO TURN MODULATOR FULL-ON. REMOVE WHEN CONNECTING LEVEL AT TP2 SHOULD BE APPROXIMATELY -2dBm WITH JUMPER INSTALLED.
3. R3 (IS A TTL LEVEL HIGH (THAT IS, THE ENABLE CONDITION) ONLY WHEN THE OUTPUT FREQUENCY IS BELOW 120 MHz.
4. INDUCTOR L9 IS NOT A DISCRETE COMPONENT. IT IS A PC BOARD TRACE.
5. U2 SHOULD BE SOLDERED AT PINS 1 AND 8.
6. ASTERISK (*) INDICATES THAT PARTS ARE SELECTED IN TEST. THE VALUES SHOWN ARE TYPICAL ONLY. SEE SECTION V FOR PROCEDURES.
7. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENT MIGHT BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.

† BACKDATING INFORMATION IN SECTION VII

REFERENCE DESIGNATIONS

NO PREFIX	A4A10
W16-18	XA4A5
A4A5	
C1-10, 12-32 CR1-4 J1-3 L1-19 Q1-6 R3, 8-31, 33-42 TP1-11 U1, 2 W1, 2	

LOGIC LEVELS

LOGIC	TTL	ECL	EECL	CMOS
HIGH (1)	≥ 2V	≥ -0.1V	≥ +0.5V	≥ VDD
LOW (0)	≤ 0.8V	≤ -1.5V	≤ -1.4V	≤ 0.1V
5= EQUAL TO OR MORE NEGATIVE THAN				
2= EQUAL TO OR MORE POSITIVE THAN				
INPUT	TTL	ECL	EECL	CMOS
GROUND	LOW(0)	HIGH(1)	HIGH(1)	LOW(0)
OPEN	HIGH(1)	LOW(0)	LOW(0)	X
GROUND-0V	X = UNDEFINED			

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1, 3	1853-0036
Q2, 5, 6	1854-0720
Q4	1854-0477
U1	08662-60002

U2 MIXER BOTTOM VIEW

Q2, 5, 6 TOP VIEW

U1 BOTTOM VIEW

31 A4A5

Figure 8-506. A4A5 Output Section LF Down Converter Schematic

SERVICE SHEET 32
A4A3 LOW FREQUENCY AMPLIFIER BOARD

TROUBLESHOOTING HELP

Block Diagram E
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The low level (−16 dBm typical) 0.01 to 120 MHz output from the Low Frequency Down Converter (service sheet 31) is pre-amplified by the Low Frequency Amplifier before it is sent to the final output amplifiers.

Low-Pass Input Filter

The signal from the Low Frequency Down Converter enters the Low Frequency Amplifier at J1. Here, the mixer sum frequency signal is terminated by a 50 ohm load so that it won't reflect back into the mixer. The desired difference frequency is passed through 120 MHz and 140 MHz low-pass filters, preventing any RF or LO signals from entering the amplifier.

Amplifier Section

The two feedback amplifiers formed by Q1 and Q3 are low in noise. The amplifier formed by Q1 has a gain of approximately 13 dB. Buffer amplifier Q2 minimizes loading of Q1 and matches impedance to the next stage. The signal level at the output of this buffer is −3 dBm. The second feedback amplifier (formed by Q3) provides 7 dB of gain and has an output signal level of about +4 dBm.

Switchable Pads

The switchable pads following Q3 control the output signal level. The pads attenuate at 2 dB, 4 dB, and 8 dB so that any desired attenuation between 2 dB and 14 dB can be accomplished in 2 dB steps. These pads are switched in and out by the low frequency amplifier level-control lines, which come from the DCU. The output of the Low Frequency Amplifier Board is sent to the Output Amplifier Board (service sheets 34 and 35).

A4A3 ASSEMBLY

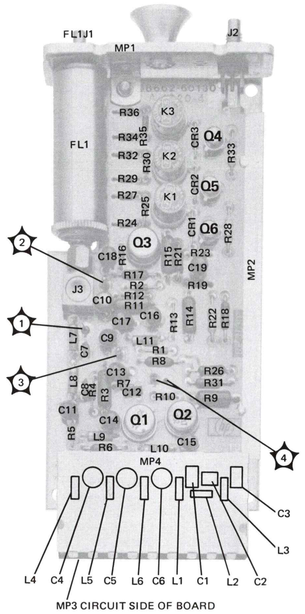
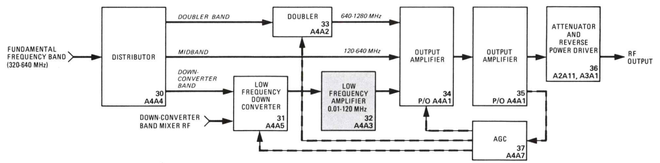


Figure 8-507. A4A3 Output Section LF Amplifier Component Locations



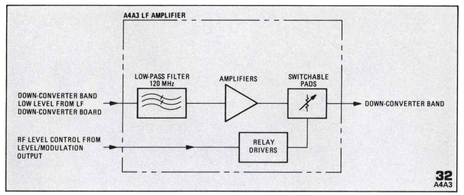


Figure 8-508. A4A3 Output Section LF Amplifier Block Diagrams

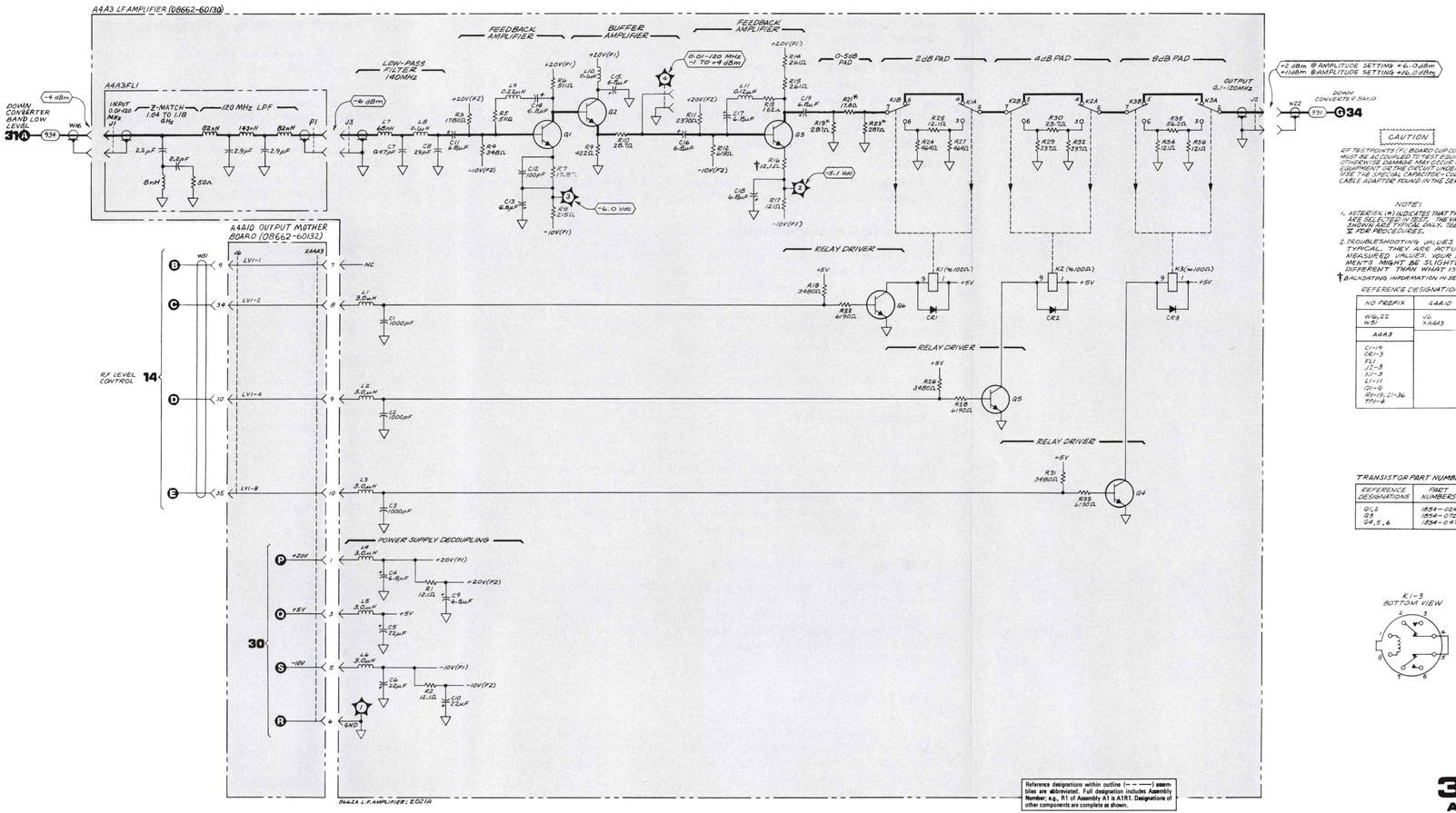


Figure 8-509. A4A3 Output Section LF Amplifier Schematic

SERVICE SHEET 33
A4A2 DOUBLER BOARD

TROUBLESHOOTING HELP

Block Diagram E
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The Doubler Board doubles the basic band frequency from the Distributor Board so that the 640 MHz to 1280 MHz frequency range can be generated.

Doubler Filter Microcircuit (A4U2)

The doubler band frequency enters the doubler filter (a microcircuit which is located on the A4A2 board) at J1. The input frequency is 320 MHz to 640 MHz (at +1.75 dBm). The signal is first amplified and then sent to the doubler. Following the doubler is a voltage-tuned filter. This is a bandpass filter made of varactor diodes in a back-to-back arrangement (to minimize harmonic generation).

The last block in A4U2 is the final amplifier stage. The signal enters it from the voltage-tuned filter at 0 dBm and is amplified to +10 dBm. The output of this amplifier is sent to the modulator filter (A4U3) through a coaxial cable.

Modulator Filter (A4U3)

The output signal from J2 to A4U2 enters A4U3 at J1. The first stage in this microcircuit is the voltage-tuned filter. Following this is a pi-type PIN modulator. The PIN diodes behave as RF resistors. Their resistance is controlled by the amount of dc bias current flowing through them. The amount of control current used by the modulator varies from 0 mA to 5 mA. Following the modulator is another amplifier. The output from it is 640 MHz to 1280 MHz at +5 dBm maximum (depending on the modulator settings).

AGC and Doubler Enable Circuitry

The AGC circuitry controls the gain of the modulator in microcircuit A4U3 so that the Generator's RF output is constant. The AGC signal comes from the AGC board (service sheet 37) and enters the Doubler Assembly via pin 6. The doubler in microcircuit A4U2 is enabled by the doubler enable circuitry found on the Doubler Board. The signals which control this circuit come from the DCU.

Filter Tuning D/A Converter

The control signals for the voltage-tuned filters come from ROM U4 by way of the D/A converter formed by U1 and U5. Actual frequency select signals which address the ROM come from the DCU. These signals determine the frequencies to be passed or rejected by the tuned filters. The ROM is enabled at the same time as the doubler in A4U2.

Transistor Q3 forms a constant reference voltage source (adjustable by R29) for the D/A converter. This also determines the maximum frequency pass band of the voltage-tuned filters. R40 sets the low filter tracking voltage. During the initial setup procedure, R40 is first adjusted and then R29 is adjusted. This

SERVICE SHEET 33 (Cont'd)

order eliminates interaction between the two pots (if R29 is adjusted first, interaction will occur).

The ROM contains information for automatic correction of the tuning curves of the filters. ROM advancement of the voltage-tuned filters is in 2 MHz steps from 640 MHz to 1280 MHz. The addresses which select the ROM D/A outputs are not available in table form, but if the ROM address lines are incremented (by putting the instrument into sweep mode; 2 MHz steps from 640 MHz to 1280 MHz), verification of proper stepping can be made by checking that the output of the doubler band increments in 2 MHz steps. It should be noted that the frequency will still increment even if the filter isn't working properly.

NOTE:

Anytime either one or both of the microcircuits A4U2 and A4U3 are changed, a new ROM must be installed. When the ROM is programmed, any inconsistencies which exist within the two microcircuits are taken into account. The software in the ROM is unique to the two microcircuits and must be re-generated at the factory (and a new ROM programmed) in the event that the microcircuits are replaced.

TROUBLESHOOTING

This assembly contains a unique ROM (U4) which is programmed at the factory to match the voltage-tuned filters in the two microcircuits. If the ROM or either microcircuit fails, the entire A4A2 doubler assembly must be replaced. A rebuilt assembly is available (see section VI, Replaceable Parts, for part number). All other parts can be replaced. It is more economical to replace components where possible.

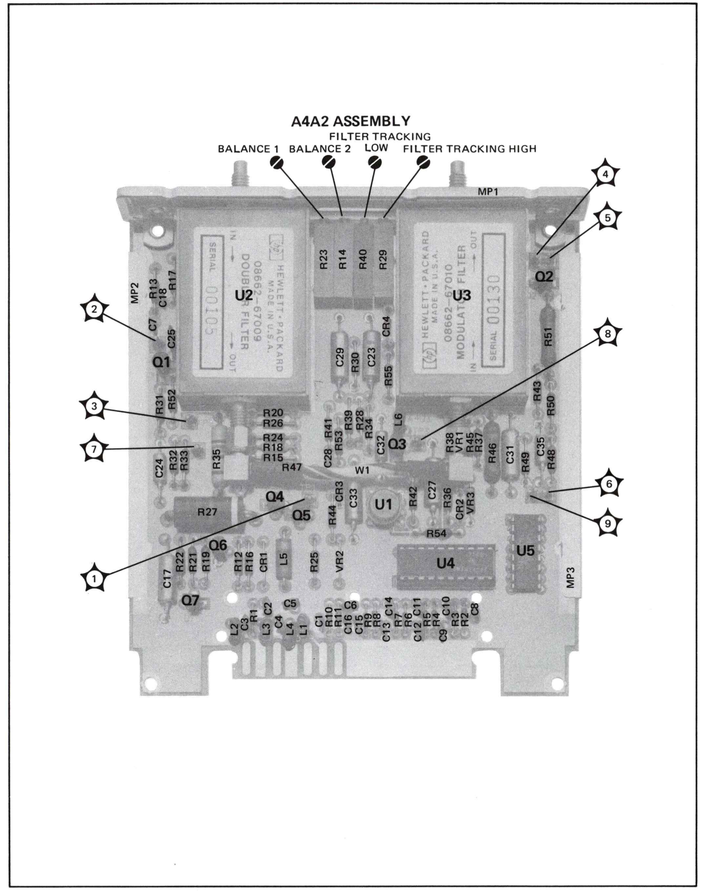


Figure 8-510. A4A2 Output Section Doubler Component Locations

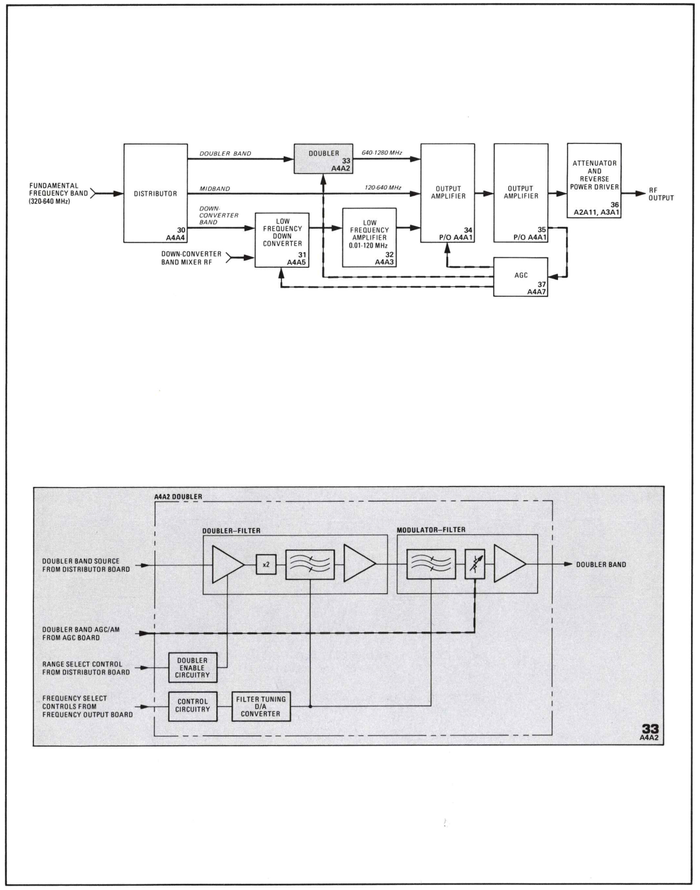


Figure 8-511. A4A2 Output Section Doubler Block Diagrams

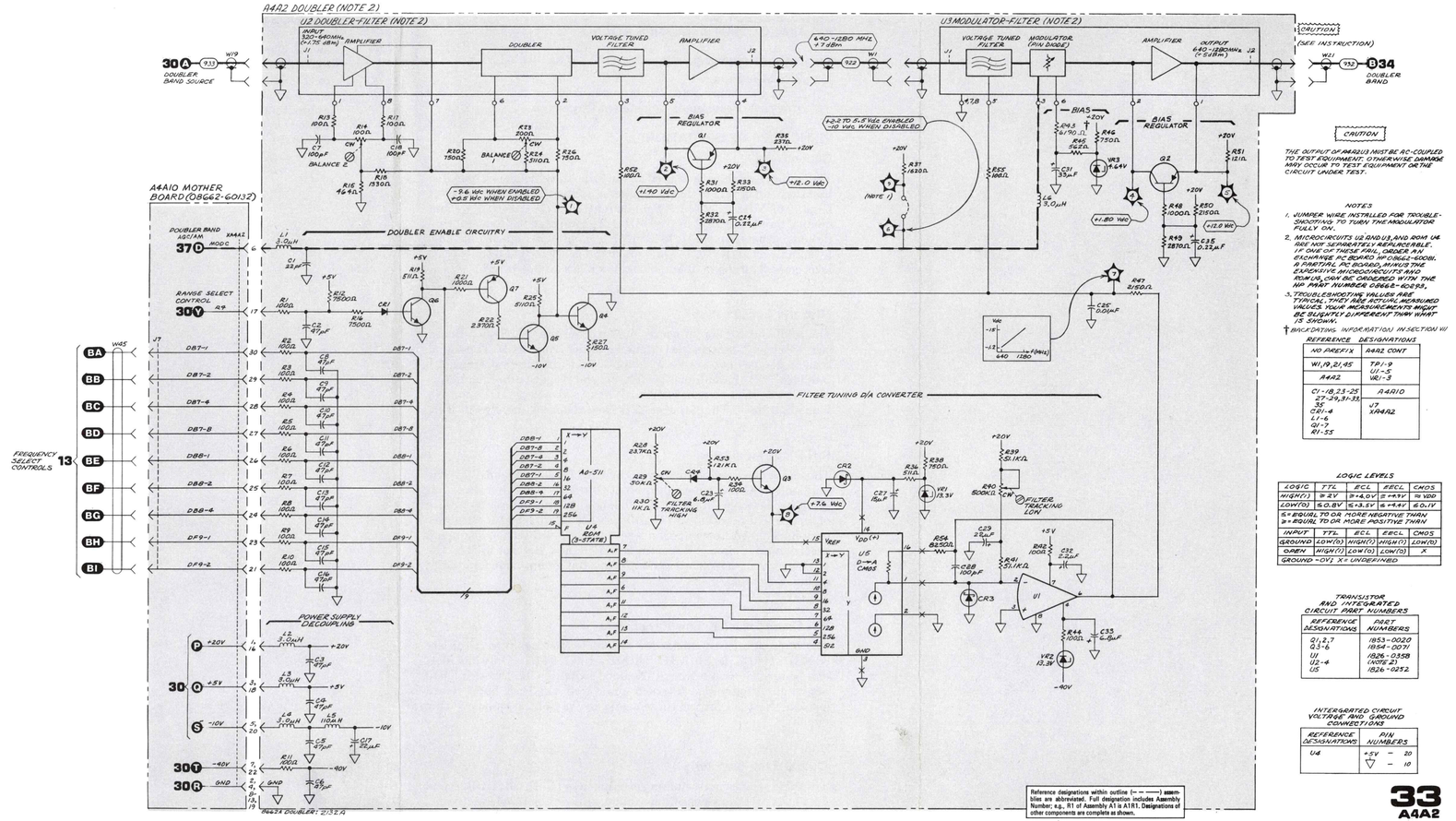


Figure 8-512. A4A2 Output Section Doubler Schematic

SERVICE SHEET 34
P/O A4A1 OUTPUT AMPLIFIER BOARD

TROUBLESHOOTING HELP

Block Diagram E
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The Output Amplifier Board consolidates the three frequency bands so that they can be sent to the final power amplifier. The down-converter band (0.01 MHz to 120 MHz), midband (120 MHz to 640 MHz) and doubler band (640 MHz to 1280 MHz) are combined to produce a continuous output from 10 kHz to 1280 MHz. Band switching is controlled by signals from the DCU. Only one band is selected at a time. AGC level control for the midband also takes place on this board.

Midband Amplification

The midband RF signal source output from the Distributor Board (service sheet 30) enters the Output Amplifier Board at J1. The signal then undergoes two stages of amplification. In the first stage, Q1 provides 3 dB of amplification. The second stage of amplification is provided by micro-circuit U2, which has 11 dB of gain. Q7 acts as a bias stage for U2. The output of U2 is fixed at approximately +13 dBm.

PIN Diode Modulator

The midband modulator is formed by CR2, CR3, CR4, and CR5. The midband AGC line enters the output board via pin 4 and its signal is injected between CR3 and CR4. The signal forward-biases both pairs of diodes. The more current that flows through the diodes, the lower their impedance. Low impedance results in a low insertion loss and a greater output signal. Resistors R18, R19, and R21 act to keep the control current versus attenuation curve flat and provide for greater modulator range.

PIN Diode Switched Low-Pass Filters

The filter cutoff frequencies for the 5-pole low pass filter bank are 660 MHz, 460 MHz, 340 MHz, 240 MHz and 180 MHz. Only one filter can be turned on at a time. PIN diode switches CR6 through CR15 activate the individual filters. Signals from the Distributor Board (service sheet 30) control these diodes by way of the on-board logic circuitry.

Output Band Switching

The three-way output switching is handled by CR20, CR21, CR22, and CR23. As in the low-pass filter section, only one channel is activated at a time. Signals from U4 in the logic section control switching in the same manner as they do in the filter section. CR21 switches the doubler band to the output, CR22 switches the midband, and CR20 and CR23

switch the down-converter band. Since the band switches are paralleled, the output to the Output Power Amplifier Board is continuous in three ranges from 10 kHz to 1280 MHz. Test point 5, which is dc coupled to the cathodes of CR21, CR22, and CR23, is maintained at approximately +4.75 volts by normal operation of the output multiplexor circuit. The output from the decoder section is connected by C41 to the final power amplifier (service sheet 35).

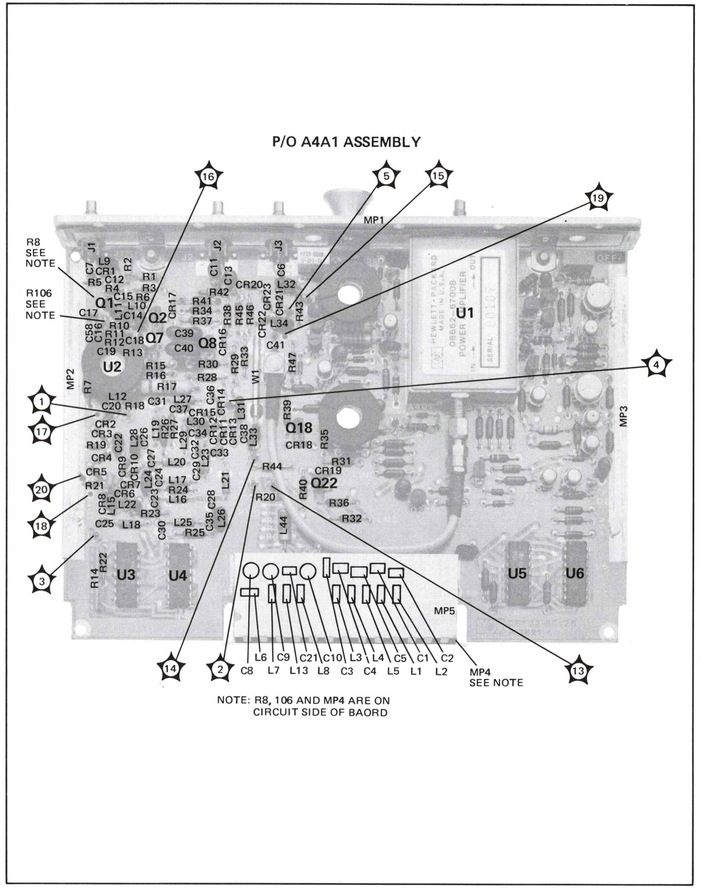


Figure 8-513. P/O A4A1 Output Amplifier Component Locations

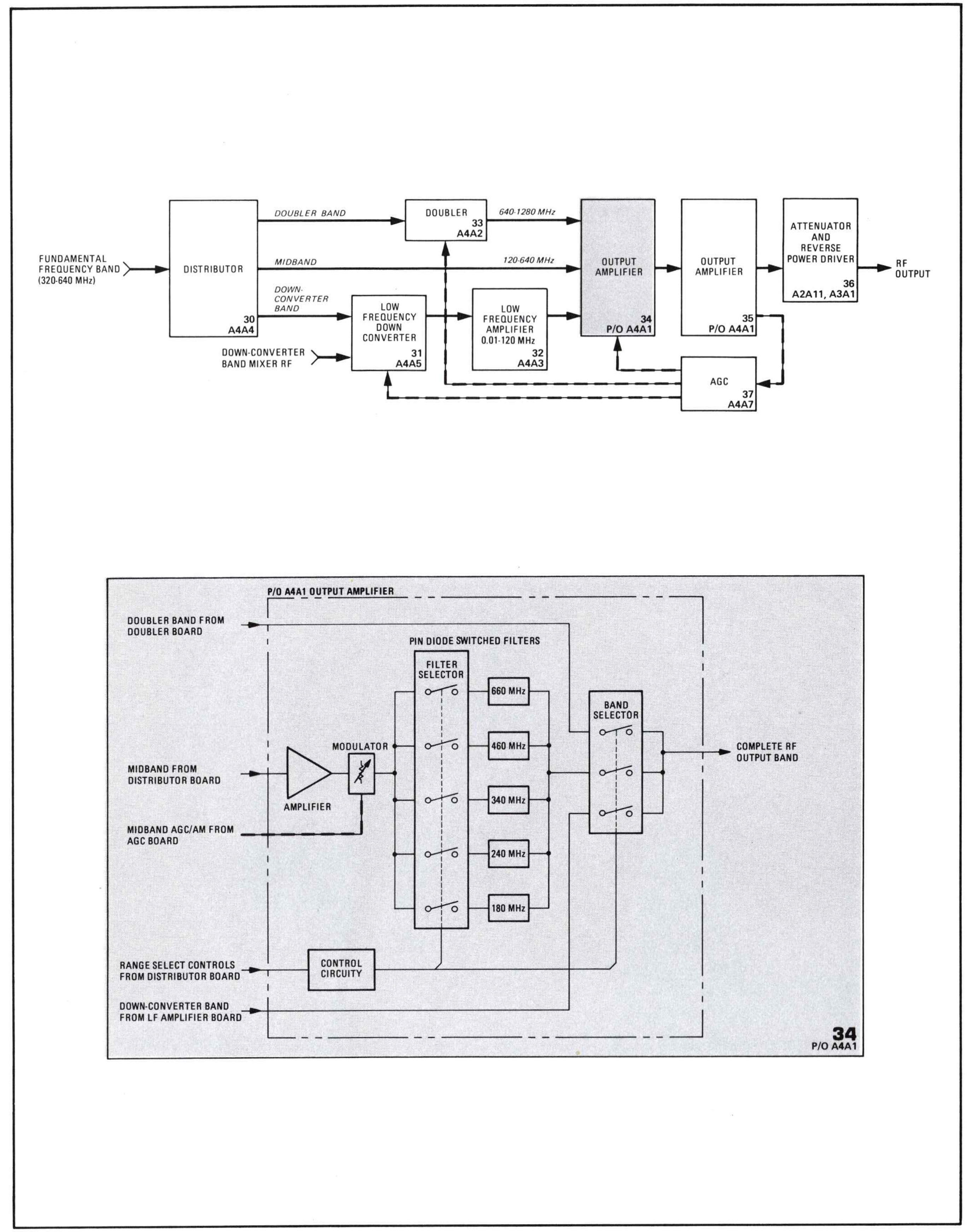
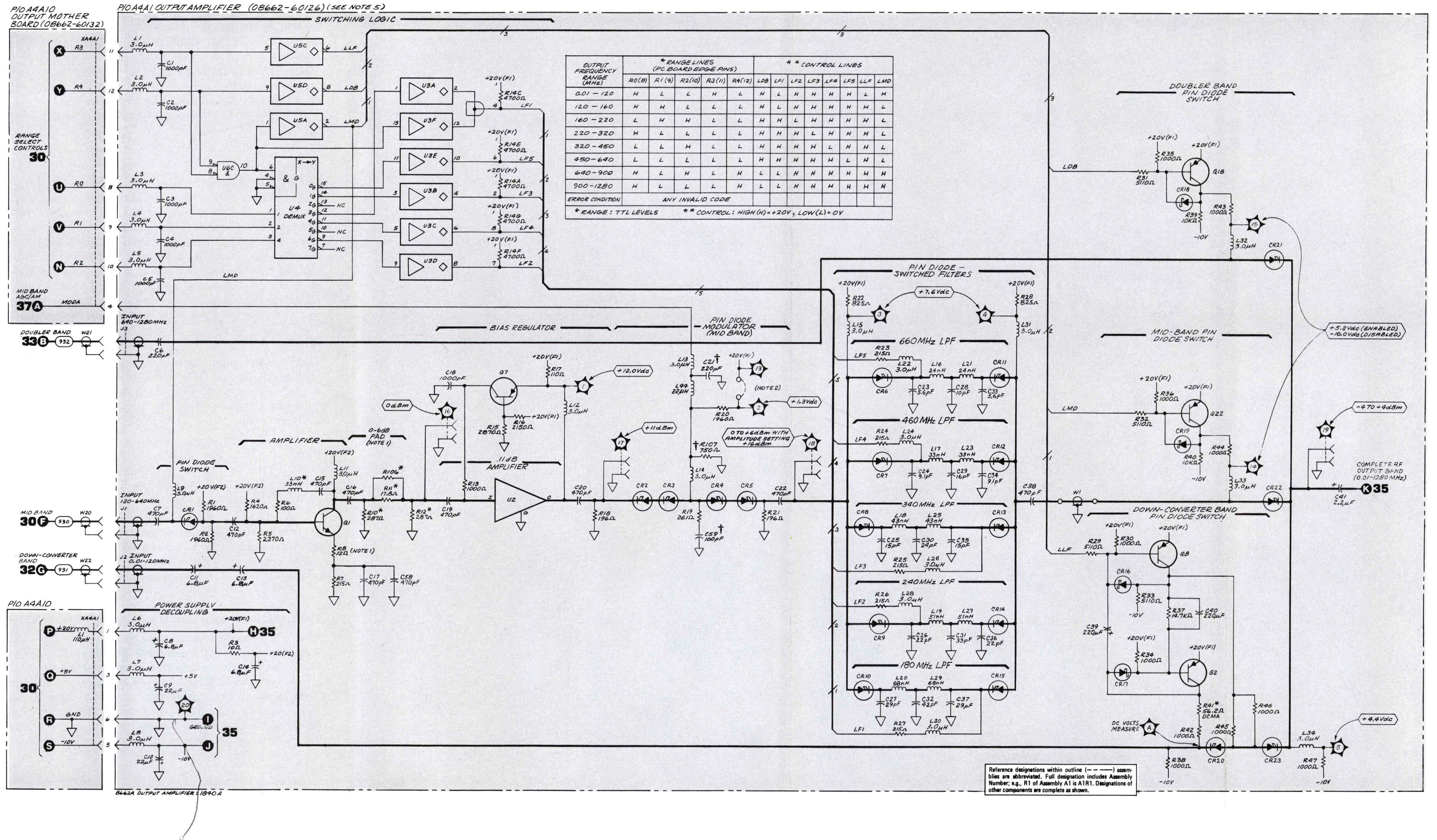


Figure 8-514. P/O A4A1 Output Amplifier Block Diagrams



OUTPUT FREQUENCY RANGE (MHz)	* RANGE LINES (PC BOARD EDGE PINS) R0(8)	R1(9)	R2(10)	R3(11)	R4(12)	** CONTROL LINES LDB	LF1	LF2	LF3	LF4	LF5	LLF	LMD
0.01 – 120	H	L	L	H	L	H	L	H	H	H	H	L	H
120 – 160	H	H	L	L	L	H	L	H	H	H	H	H	L
160 – 220	L	H	H	L	L	H	H	L	H	H	H	H	L
220 – 320	H	L	L	L	L	H	H	H	L	H	H	H	L
320 – 450	L	L	H	L	L	H	H	H	H	L	H	H	L
450 – 640	L	L	L	L	L	H	H	H	H	H	L	H	L
640 – 900	H	L	H	L	H	L	L	H	H	H	H	H	H
900 – 1280	H	L	L	L	H	L	L	H	H	H	H	H	H
ERROR CONDITION	ANY INVALID CODE												

* RANGE: TTL LEVELS ** CONTROL: HIGH (H) = +20V, LOW (L) = 0V

CAUTION

RF TESTPOINTS (PC BOARD CUP CONNECTORS) MUST BE AC-COUPLED TO THE TEST EQUIPMENT. OTHERWISE, DAMAGE MAY OCCUR TO THE TEST EQUIPMENT OR THE CIRCUIT UNDER TEST. USE THE CAPACITOR-COUPLED CABLE ADAPTOR FOUND IN THE SERVICE KIT.

NOTES

1. THE SMALL CHIP RESISTORS ON THIS ASSEMBLY REQUIRE LOW TEMPERATURE SOLDERING TECHNIQUE. USE SILVER SOLDER. R11 AND R106 WILL BE CHIP RESISTORS ONLY FOR CERTAIN SELECTED VALUES.
2. JUMPER WIRE IS INSTALLED FOR TROUBLESHOOTING ONLY TO TURN MODULATOR FULLY ON.
3. ASTERISK (*) INDICATES THAT THESE PARTS ARE SELECTED IN TEST. THE VALUES SHOWN ARE TYPICAL ONLY (IN SOME CASES, R106 WILL NOT BE USED). SEE SECTION V FOR PROCEDURES
4. TROUBLESHOOTING VALVES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALVES. YOUR MEASUREMENTS MIGHT BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
5. A PARTIAL PC BOARD, MINUS THE EXPENSIVE MICROCIRCUIT U1, CAN BE ORDERED WITH HP PART NUMBER 08662-60291.

† BACKDATING INFORMATION IN SECTION VII

REFERENCE DESIGNATIONS

NO PREFIX	A4A1 CONT.
W20-22	R1-8, 10-47, 107 TP1-5, 13-20 U2-6 W1
A4A1	A4A10
C1-41, 59 CR1-23 J1-3 L1-39, 44 Q1, 2, 7, 8, 18, 22	L1 XA4A1

LOGIC LEVELS

LOGIC	TTL	ECL	EECL	CMOS
HIGH (1)	≥2V	≥+4.0V	≥+4.9V	≈VDD
LOW (0)	≤0.8V	≤+3.5V	≤+4.4V	≤0.1V

≤ = EQUAL TO OR MORE NEGATIVE THAN
≥ = EQUAL TO OR MORE POSITIVE THAN

INPUT	TTL	ECL	EECL	CMOS
GROUND	LOW(0)	HIGH(1)	HIGH(1)	LOW(0)
OPEN	HIGH(1)	LOW(0)	LOW(0)	X

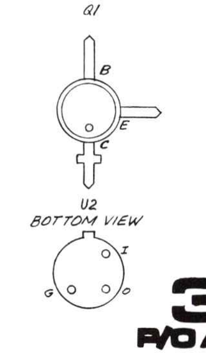
GROUND - 0V; X = UNDEFINED

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1	1854-0720
Q2, 8, 18, 22	1853-0036
Q7	1853-0007
U2	08662-67002
U3	1820-0668
U4	1820-1216
U5	1820-0471
U6	1820-1144

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U3, 5, 6	+5V – 14; ground – 7
U4	+5V – 16; ground – 8



34 P/O A4A1

Figure 8-515. P/O A4A1 Output Amplifier Schematic

SERVICE SHEET 35
P/O A4A1 OUTPUT AMPLIFIER BOARD

TROUBLESHOOTING HELP

Block Diagram E
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The RF signal from the Output Amplifier goes through two levels of amplification within the final wideband power amplifier stage. These two stages of gain are provided by microcircuit A4U1. Supportive functions are provided by additional circuitry on this board. Included are two wideband bias regulators (for the two amplifiers in the microcircuit), time constant switches (which adjust the AM bandwidth at various frequencies), a subtractor operational amplifier (for eliminating the dc component of the RF signal used by the AGC circuitry), noise shunts, reference detector bypass, and switching logic.

Wideband Regulators

The wideband regulator for the first amplifier stage is formed by Q19, Q23, and Q24. Q3, Q10, and Q15 form the regulator for the second stage. These regulators are essentially gain-controlled feedback loops which have built-in rolloff characteristics to prevent oscillation at high frequencies and prevent low frequency RF from affecting biasing.

The regulator in the first amplifier stage senses the output of U1 at pin 2 and adjusts the bias at pin 1. Q23 and Q24 keep TP8 at +14 volts. C46 shorts TP9 to the base of Q19 at RF frequencies so that the impedance seen by the output of the first amplifier stage of A4U1 (through pin 2) is high. This prevents loading of the amplifier output.

The bias regulator for the second amplifier stage is almost identical to that for the first stage, except that there is an adjustment (R86) which allows the current to be set so that optimum harmonic performance can be obtained from this final output stage. The bias regulator senses at pin 4 and sends a bias voltage back to pin 3.

Peak and Reference Detectors

The AGC peak detector diode is connected to the collector of the final output transistor in the second stage of the power amplifier. The capacitor connected to it is the main peak detector capacitor for frequency bands between 10 MHz and 1280 MHz. As the operating frequencies drop below 10 MHz, however, additional capacitors are needed to decrease the bandwidth of the bypass. These capacitors are switched in by Q4, Q11, and Q14, which are driven by switching logic in the DCU. Any combination of capacitors can be switched by the DCU.

Subtractor Circuitry

The RF signal passing through U1 is superimposed on the dc collector voltage of the second amplifier stage (which is about +13Vdc). This dc voltage is removed by the subtractor stage so that the peak RF can be

SERVICE SHEET 35 (Cont'd)

filtered and sent to the AGC Assembly (service sheet 37).

The subtractor is a discrete differential op-amp (formed by Q17) operating in a common-rejection mode. One input is fed the (negative) peak detected RF-plus-dc (from the AGC Negative Peak Detector); the other input is fed dc only (from the Reference Detector). The differential op-amp cancels the dc bias component because it is common to both inputs, but passes the RF signal. A low-pass filter at the output of the subtractor eliminates harmonics. The output of this filter is sent to the AGC Board (service sheet 37) at 0 to +4Vdc. This voltage increases with increasing RF.

Noise Shunts and Reference Detector Bypass

The output amplifier (U1) generates considerable broadband noise below 1 MHz. This noise is shunted through Q9 and Q13 and is bypassed to ground by C54 and R105.

The reference detector bypass consists of a continuously connected capacitor (C57) and a switchable capacitor (C56), which attenuate the lower frequency RF that is removed by the reference detector in U1. Attenuation of higher RF frequencies is accomplished by L43.

P/O Output Amplifier
P/O A4A1
SERVICE SHEET 34

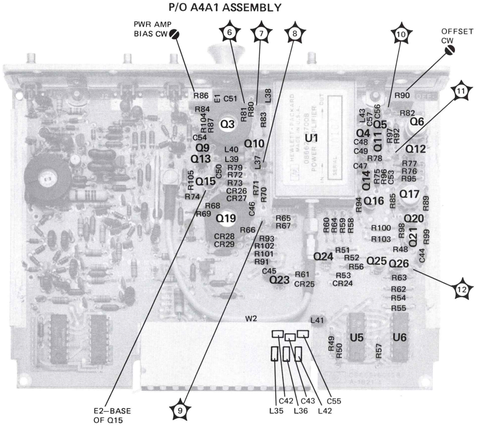


Figure 8-516. P/O A4A1 Output Amplifier Component Locations

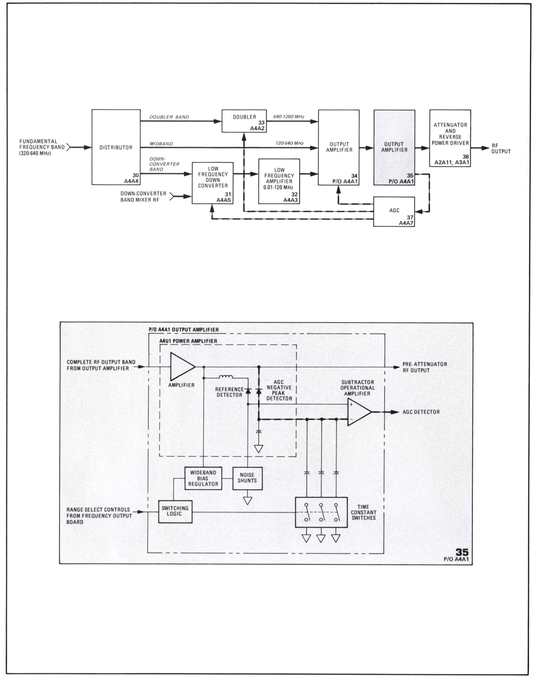
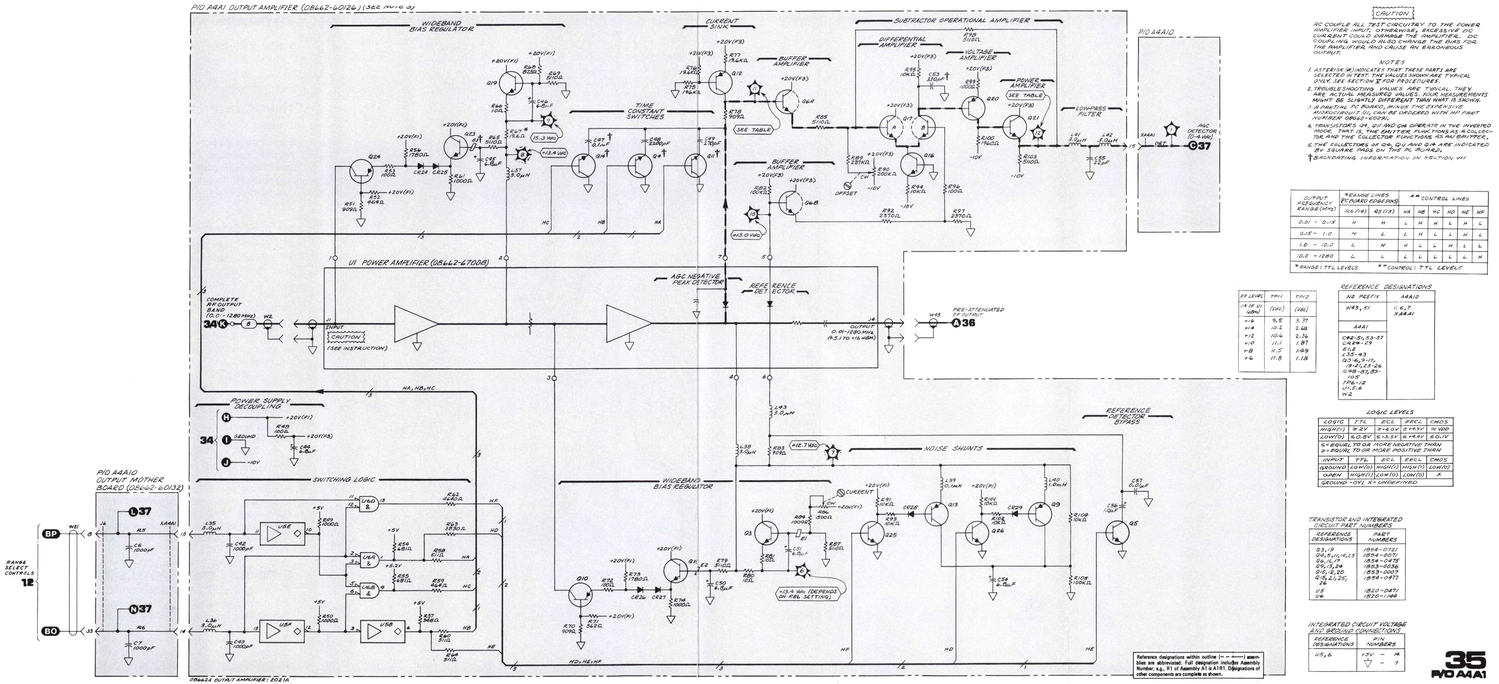


Figure 8-517. P/O A4A1 Output Amplifier Block Diagrams



CAUTION

AC COUPLE ALL TEST CIRCUITRY TO THE POWER AMPLIFIER INPUT, OTHERWISE, EXCESSIVE DC CURRENT COULD DAMAGE THE AMPLIFIER. DC COUPLING WOULD ALSO CHANGE THE BIAS FOR THE AMPLIFIER AND CAUSE AN ERRONEOUS OUTPUT.

NOTES

1. ASTERISK (*) INDICATES THAT THESE PARTS ARE SELECTED IN TEST AND THEREFORE ARE TYPICAL ONLY. SEE SECTION VI FOR PROCEDURES.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MIGHT BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
3. A PARTIAL PC BOARD, MINUS THE EXPENSIVE MICROWAVE SILICA, IS ORDERED WITH HP PART NUMBER 08662-60018.
4. TRANSISTORS Q4, Q7 AND Q16 GENERATE THE INVERTED VERSIONS OF THE SIGNALS THAT THEIR EMITTERS ARE CONNECTED TO. THEIR FUNCTIONING IS CRITICAL.
5. THE VALUES OF THE 20 Ω R-A ARE INDICATED BY SQUARE PADS ON THE PC BOARD.

†INDICATES INFORMATION IN SECTION VII

OUTPUT FREQUENCY RANGE (GHz)	*RANGE LINES (PC BOARD EDGE PINS)		**CONTROL LINES					
	RA (P18)	RB (P3)	HA	HB	HC	HD	HE	HF
0.01 - 0.19	H	H	L	H	H	L	H	L
0.15 - 1.0	H	L	L	H	H	L	L	H
1.0 - 10.0	L	H	H	L	L	H	L	L
10.2 - 12.80	L	L	L	L	L	L	L	H

*RANGE: TTL LEVELS **CONTROL: TTL LEVELS

RF LEVEL (+13 dBm)	TP11 (Vdc)	TP12 (Vdc)
+16	9.6	3.77
+14	10.2	2.48
+12	10.6	2.14
+10	11.1	1.87
+8	11.5	1.69
+6	11.8	1.58

REFERENCE DESIGNATIONS

NO PREFIX	A4A10
H45, 51	C 6, 7 R 4, 7
A4A1	
C42-51, 53-57 C429-29 L 1 L52 L53 03-69-71, 73-81, 83-84, 86-87 L94, 98 U1, 2, 8 W2	

LOGIC LEVELS

<LOGIC	TTL	ECL	FACL	CMOS
HIGH(1)	2.2V	-1.4.0V	0.45V	10 VDC
LOW(0)	0.8V	-5.2V	0.45V	0.0V

1=EQUAL TO OR MORE POSITIVE THAN
0=EQUAL TO OR MORE POSITIVE THAN

INPUT	TTL	ECL	FACL	CMOS
GROUND	LOW(0)	HIGH(1)	HIGH(1)	LOW(0)
OPEN	HIGH(1)	LOW(0)	LOW(0)	X
GROUND-ONLY X'S UNDEFINED				

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q3, 9 Q4, 5, 11, 12, 13 Q6, 7, 8 Q9, 15, 16 Q10, 14 Q14, 21, 23, 24 U5 U6	1854-0702 1854-0071 1854-0478 1853-0036 1854-0215 1854-0493 1820-0471 1820-1144

INTEGRATED CIRCUIT VOLTAGE AND RESISTOR CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U5, 6	+5V = 14 GND = 7

Reference designations within outline (— — —) assemblies are abbreviated. Full designation includes Assembly Number; e.g., 51 of Assembly A1 is A1R1. Designations of other components are complete as shown.

35
P/O A4A1

Figure 8-518. P/O A4A1 Output Amplifier Schematic

SERVICE SHEET 36
A3A1 REVERSE POWER DRIVER, A2A11 ATTENUATOR

TROUBLESHOOTING HELP

Block Diagram E
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The attenuator provides precise level control at the RF output of the Signal Generator. The attenuator is composed of six electro-mechanical attenuator pads. Three of the pads attenuate the signal by 40 dB, one by 20 dB, one by 10 dB, and one by 5 dB. Any combination of pads can be switched to produce attenuation up to 145 dB.

Reverse-Power Protection Circuitry

The reverse power sensor (limiter/detector) is located in the attenuator. This circuit sends a continuous reference voltage to the Reverse Power Board (A3A1) so that comparator U1 can determine when an excessive power condition is occuring. When the output of the comparator goes HI, latch U2B sets. This triggers the relay driver circuitry, which in turn activates the output-disconnect relay.

The limiter/detector circuit provides temporary protection to the output section in the event that power is accidentally connected to the front or rear panel RF Output connectors. This limiter circuitry only provides protection until the switching relay can be activated to disconnect the RF outputs from the attenuator and Output Amplifier.

General-Reverse Power Driver Board (A3A1)

The reverse-power protection circuitry is a standard feature designed to protect the Signal Generator from accidental applications of reverse signal levels (up to 30 watts) that could damage sensitive output circuitry, or cause component deterioration, resulting in reduced performance. The circuitry is designed to trigger at 10 volts peak RF, protecting against accidental keying of transmitters, connection of charged cables, or other potentially destructive inputs to the RF output connectors. Pressing the AMPLITUDE key will reset the Signal Generator to normal operation after the reverse-power protection circuit has been activated.

Comparator, Latch and Driver Circuitry

The comparator circuit checks the voltage from the sensor circuitry in the attenuator against a reference voltage in order to trigger the relay activation latch. The comparator is programmed to trigger when the peak reverse RF signal exceeds 10 volts. Once the latch has been set, the relay driver circuitry activates the output-disconnect relay. When the relay opens, the RF output connectors are disconnected from the attenuator and the Output Power Amplifier.

When the latch opens, an error message is sent to the DCU. The DCU in turn activates the user message indicator lamps on the front panel.

SERVICE SHEET 36 (Cont'd)

Once the AMPLITUDE key is pressed, the DCU generates a reset pulse which is sent to the latch. When the latch resets, the relay driver circuitry is disabled. This closes the output-disconnect relay and causes the output power amplifier to be reconnected to the front or rear panel RF Output connectors.

Power-Up Circuitry

When the instrument is first turned on, the power-up circuitry forces the relay-activation latch to come up in a reset mode. This ensures that the Output Amplifier is connected to the RF output connectors. Should a reverse power condition be in effect during power-up, however, the output protection relay will trigger and disconnect the output.

P/O Output Amplifier
P/O A4A1
SERVICE SHEET 35

A3A1 ASSEMBLY

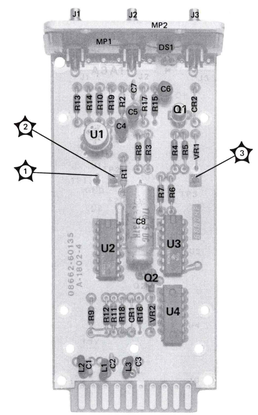


Figure 8-519. A3A1 Reverse Power Driver Component Locations

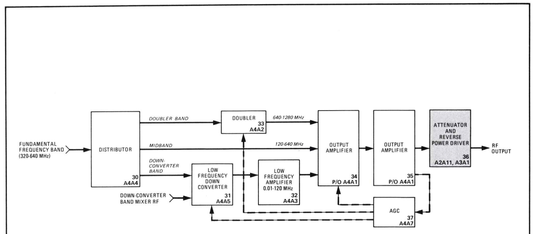
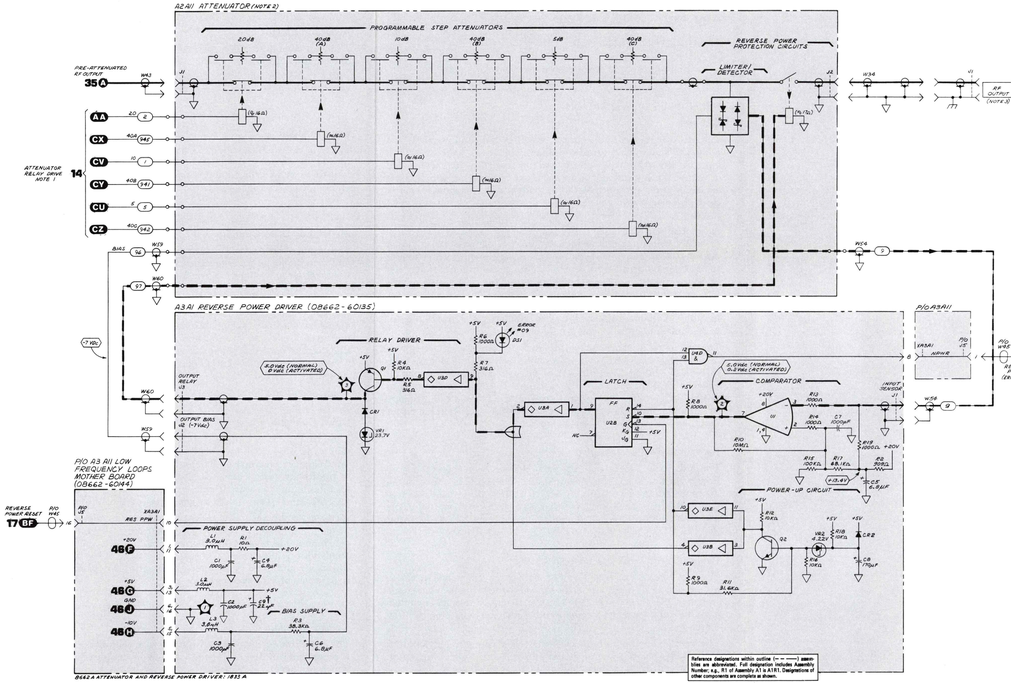


Figure 8-520. A3A1 Reverse Power Driver and Attenuator Block Diagrams



NOTES

1. A TTL HIGH INPUT TO THIS STEP ATTENUATOR ACTIVATES THE ATTENUATION ELEMENT, WHILE A LOW WILL ACTIVATE THE THRU LINE FOR THAT SECTION.
2. THE ATTENUATOR ASSEMBLY IS FACTORY REPAIRABLE ONLY. IT IS REPLACEABLE WITH A KIT THAT INCLUDES A SPECIAL LEVEL CORRECTION ROM. SEE SECTION VI FOR INFORMATION ON HOW TO ORDER A KIT NUMBERED.
3. FOR OPTION 004, W34 IS A SEMI-RIGID COAXIAL CABLE CONNECTED TO THE REAR PANEL (OPTIONAL RF OUTPUT).
4. TROUBLESHOOTING THIS ASSEMBLY MAY TAKE MORE ACTIVE REVERSE POWER. YOUR INTERFERENCE MIGHT BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.

† SIGNIFICANT INFORMATION IN SECTION VII

REFERENCE DESIGNATORS

NO PREFIX	A1A1
J1	J1-3
W14, 43, 45, 74, 80	J10,2
	J12
A2A11	J1,3
	J2,3
	J1,2
	A1-15
	J11-3
	J13,2
	W6,2
	A3A11
	J1 P/O A3A11

LOGIC LEVELS

LOGIC	TTL	ECL	PECL	CMOS
HIGH(1)	2.2V	-1.42V	3.98V	≥ 70%
LOW(0)	0.8V	-1.63V	3.48V	≤ 30%

0 = EQUAL TO OR MORE NEGATIVE THAN
1 = EQUAL TO OR MORE POSITIVE THAN

INPUT	TTL	ECL	PECL	CMOS
GROUND (LOW(0))	HIGH(1)	HIGH(1)	LOW(0)	
OPEN	HIGH(1)	LOW(0)	LOW(0)	A
GROUND =10V, X = UNDEFINED				

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1	1853-0062
Q2	1884-0071
U1	1826-0026
U2	1820-1212
U3	1820-0175
U4	1820-1197

INTEGRATED CIRCUIT POWER AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U2	+5V - 16
	▽ - 8
U3,4	+5V - 14
	▽ - 7

Figure 8-521. A3A1 Reverse Power and Attenuator Schematic

SERVICE SHEET 37
A4A7 AGC ASSEMBLY BOARD

TROUBLESHOOTING HELP

Block Diagram E
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The AGC section levels the output, provides vernier adjustment, and adds AM. The circuitry forms a feedback loop in which the level of the output is sensed by an RF detector and compared to a reference voltage at the AGC comparator. The output of the comparator, which represents the level error, drives the individual band modulator-boards through their respective modulator driver amplifiers on the AGC assembly.

As an example of leveling action, suppose the output RF level drops (possibly as a result of frequency tuning). The output of the negative peak detector diode will become more positive. The comparator checks the corresponding peak detector voltage decrease at the output of the inverting amplifier against the $-V_{REF}$ from the reference/AM level D/A converter and senses the change as an error. The comparator then drives the modulator in such a manner as to increase the current into it. This reduces the modulator's attenuation of the RF signal, increasing amplitude level at the RF output.

The reference/AM level D/A converter also sums with $-V_{REF}$ or any AM input (which may come from the front panel AM jack or the internal modulation source). AM works within the leveling loop by varying $-V_{REF}$. Varying $-V_{REF}$ causes the AGC comparator to sense that a level change is occuring. The AGC comparator responds by adjusting the output level to correct for the change. The result is an amplitude modulated RF output signal.

Reference/AM Level Amplifier

The AM signal generated in the modulation section enters the AGC Board via pin 20. If AM is desired, the AM signal is added to the reference voltage developed across VR1. The resulting signal is amplified and inverted by U12, which has a gain of about two. This signal is then applied to the reference/AM level D/A converter (U8 and U13).

Reference/AM Level D/A Converter

The D/A converter is essentially an attenuator. The signal at TP2 is attenuated by U8 according to the RF level control inputs which come from the DCU (LV2-0 to LV2-9). TP3 is at the junction of R25 and R26, a voltage divider which serves to attenuate the noise from U13 by a factor of two.

The fraction of attenuation by U8 can be anywhere from 1/1024 to 1. Q1 is used in a non-inverting mode as an impedance matching buffer. The attenuated AM reference signal is summed with the AGC detector signal, which comes from the Output Amplifier Board (service sheet 35), at the junction of R27 and R28.

SERVICE SHEET 37 (Cont'd)

AGC Comparator

The loop comparator is a discrete low-noise operational amplifier formed by Q2, Q3, Q4, and Q5. R32 is the feedback resistor; Q3 provides gain and acts as a level-shifter. The output of the comparator is the difference between the reference and the detector signals.

Error Detector

The error detector is a window comparator formed by U4A and U4B. Ideally, the output of the AGC comparator should be zero. If it is not zero, the error detector generates a signal which lights error lamp DS1 and sends an error message to the DCU.

Modulation Drive Circuitry

The output of the AGC comparator is sent to either the doubler band, midband, or down-converter band through the switching action of Q7, Q8, or Q9. Only one band can be enabled at a time. Once a band switch turns on, the signal from the AGC comparator is directed to one of the loop gain amplifiers. These amplifiers amplify the error voltages from the AGC comparator to drive the voltage-to-current converters (modulator drivers) and provide controlled rolloff as modulation frequency increases. The loop gain amplifiers are integrators with high dc gain that decreases with increasing frequency. High dc gain assures level accuracy. The high frequency rolloff points are determined by capacitors C18, C19, and C26.

Down Converter Band

The down-converter band operates from 10 kHz to 120 MHz. Its operation is different from the other bands because of the RF pads in the low frequency preamp (service sheet 31). These pads change the level of the RF as well as the AGC loop gain. Since it is not desirable for this change to occur, dc gain is adjusted for compensation. FETs Q12, Q13, and Q14 switch in to change the gain of U5.

As the carrier frequency decreases, the detector diode begins to follow not only the voltage peaks, but the entire carrier waveform. The AGC responds by decreasing the carrier amplitude. To prevent this, the bandwidth of the down-converter band is reduced at lower frequencies. This is accomplished by switching in integrating capacitors C24 and C25 by way of FET switches Q15 and Q16.

Control Circuitry

The switching of the FETs within the three bands is controlled by logic circuitry on the AGC board. This logic decodes digital signals which are sent to it from the Distributor Board, Output Amplifier Board, and the RF level control lines from the DCU so that the proper attenuators, gain stages, and outputs are switched at the correct times.

SERVICE SHEET 37 (Cont'd)

TROUBLESHOOTING

When an output section problem has been traced through the block diagram troubleshooting procedure to this assembly, use the following procedure to isolate the cause of the problem.

Procedure

1. Mount the A4A7 on an extender board and measure the output of the D/A converter at TP3 with a DVM. Compare the measured values to the numbers in the table, below.

FRONT PANEL AMPLITUDE SETTING	TP3 Vdc ± 0.04
+ 5.1	−0.97
+10.0	−1.85
+16.0	−3.38

The D/A converter can be more fully checked using the Mainframe Stimulus Diagnostic. Operating instructions are contained in service sheet B1.

If these voltages are normal, continue troubleshooting with step 2. Otherwise, there is a problem with the reference D/A converter circuitry so troubleshoot this part of the assembly to find the cause of the problem. To determine if the digital data to the D/A circuitry is correct, the 10 bit digital word (LV2-0 through LV2-9) which programs the D/A converter can be calculated for any front panel amplitude setting from 5.1 to 16.0 dBm as follows:

1) Subtract 16.0 from the front panel amplitude setting (result is 0 or a negative number) and divide the result by 20.
2) Take the antilog ($10^{\overline{X}}$) of this value (result is a positive number, 1 or less) and multiply the result by 1023.
3) Round off the result to the nearest integer number and convert to a 10 bit binary number.

This formula is $\left\{10^{\left[\frac{(N_{AMPL} - 16.0)}{20}\right]}\right\}_{\bullet} 1023$

where N_{AMPL} is the front panel amplitude setting (+5.1 to +16.0).

2. Move the slide switch on A4A7 to the TEST position (down). Refer to the following table to check each of the band amplifiers by performing the following sequence:
   1) Set the front panel frequency to within the band being checked.
   2) Connect to TP6 and other test points per the table.
   3) Check the driver output voltages and the front panel RF output level as shown in the table. The column listed "W/PIN" means the assembly containing the modulator for the band being checked is in the instrument and is loading the driver. The column labeled "W/O PIN" means the assembly containing the modulator is not in the instrument or the A4A7 edge connector pins where the drive signal leaves the board are taped to prevent the modulator from loading the driver.

SERVICE SHEET 37 (Cont'd)

4) Check each band with TP6 both open and grounded which turns the modulator fully off and on. If both voltage extremes are reached, that circuitry is functioning normally.

Band	TP6	Short Test Points	Driver Outputs Vdc ±0.1 W/PIN	Driver Outputs Vdc ±0.1 W/O PIN (TP18)	RF Output w/PIN modulator in
Down Converter (.01≤f<120)	open	none	− 0.26	−10.02	−30
	ground	TP20 and TP20A (see Note)	+ 1.63	+10.77	+20
Mid Band (120≤f<640)	open	none	(TP8) − 0.25	−10.02	−40
	ground	TP19 and TP19A	+ 1.61	+10.73	+16
Doubler (640≤f<1280)	open	none	(TP7) −10.02	−10.05	−30
	ground	TP17 and TP17A	+ 7.97	+ 8.61	+16

Note: Set front panel Amplitude setting to +16.0 dBm.

If operation is normal, continue troubleshooting with step 3. Otherwise, troubleshoot the driver circuitry which is not normal.

3. Set the front panel amplitude to +10 dBm. Set front panel frequency to 500.0 MHz. The switch on A4A7 should be in the test position (down) and TP6 should be open. This turns the RF off as far as the modulator can. In this condition the AGC comparator (TP5) should go to its maximum positive output value as shown in the table, below.

Condition	TP3	TP4	TP5
RF Off	−1.83 Vdc	+0.03 Vdc	+7.80 Vdc
RF On	−1.83 Vdc	+4.52 Vdc	−6.69 Vdc

Ground TP6 and short TP19 and TP19A together. This should turn the modulator fully on (RF on). The AGC comparator should go to its most negative value as shown in the table.

If the comparator output goes from its positive extreme to its negative extreme, the comparator is functioning normally. Otherwise there is a problem with the comparator circuitry.

A4A7 ASSEMBLY

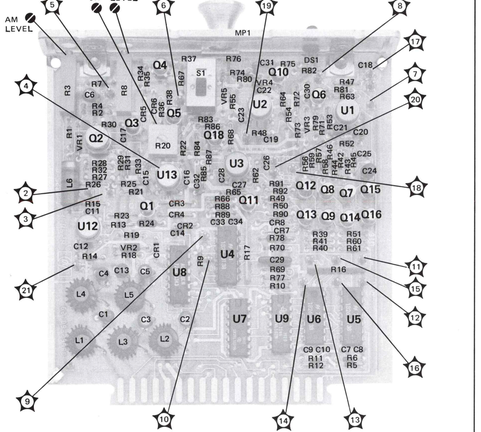


Figure 8-522. A4A7 Output Section AGC Component Locations

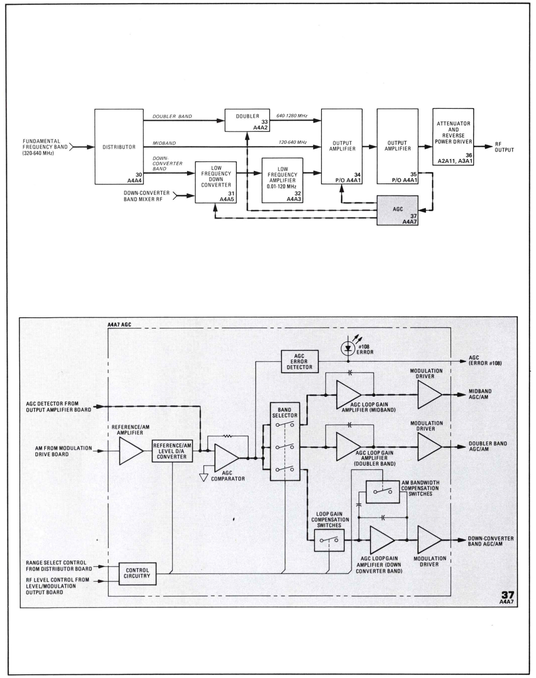


Figure 8-523. A4A7 Output Section AGC Block Diagrams

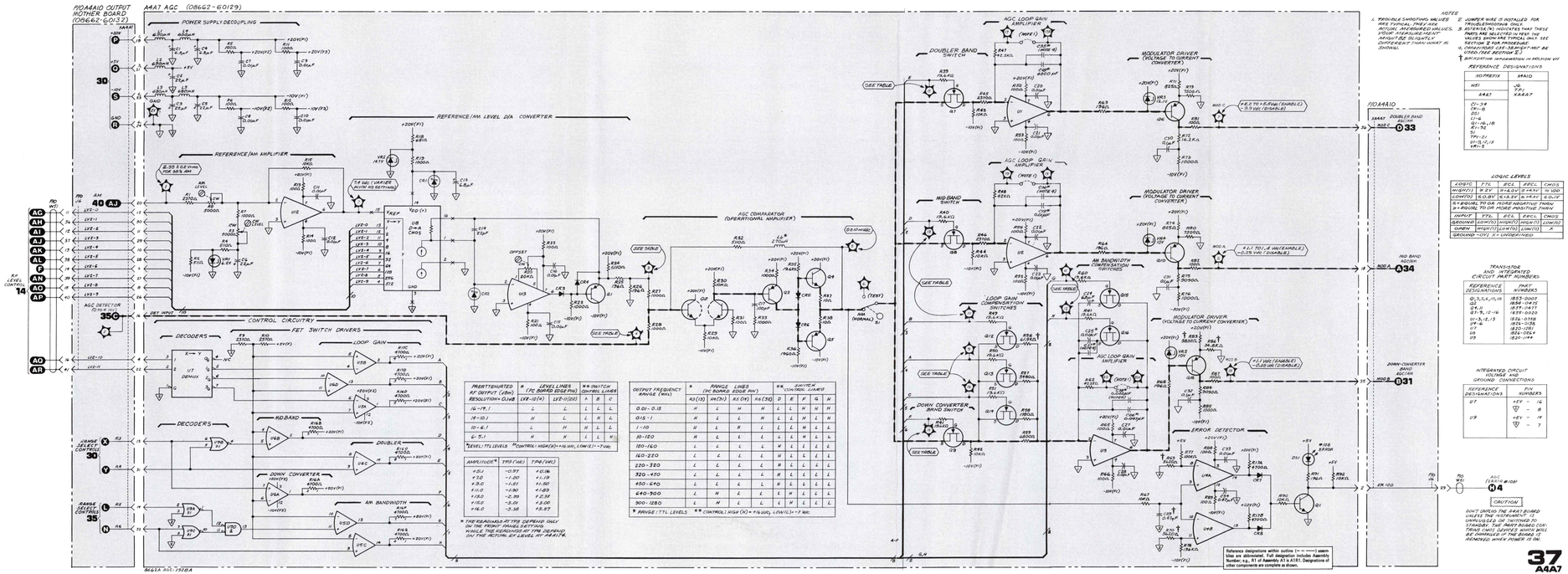


Figure 8-524. A4A7 Output Section AGC Schematic

SERVICE SHEET 38
A4A8 MODULATION DIVIDER

TROUBLESHOOTING HELP

Block Diagram F
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The purpose of the Modulation Divider (A4A8) is to develop the 400 Hz and 1000 Hz internal modulation signals and the FM Loop Error Voltage. The internal modulating signals are derived by dividing down the 10 MHz signal from the Reference Section. The FM Loop Error Voltage is developed by comparing the VCO output with a 10 MHz reference signal. The Modulation Divider consists of two major sections which are the Phase Detector Circuitry and the Internal Modulation Dividers.

Phase Detector Circuitry

The Phase Detector Circuitry compares the phase difference between the reference signal (FM 10 MHz Reference Signal) and the output of the VCO (FM Loop N-Divider Drive), then generates a voltage proportional to the phase error. Both input signals are first divided down to 100 kHz before they are compared by the FM Loop Phase Detector, U4. The 10 MHz signal from the Reference Section is divided by a total of 100. This signal becomes the reference input to the phase detector. The 140 MHz VCO output is divided by a total of 1400. This signal becomes the variable input to the phase detector.

The Phase Detector, U4, is a digital phase detector that generates output pulse widths proportional to the phase difference between the two input signals. If the variable 100 kHz signal is lower in frequency or lags the reference input in phase, the output on pin 13 generates a pulse (see figure 8-525). When the variable input is higher in frequency or leads the input in phase the output on pin 2 generates a pulse (see figure 8-526).

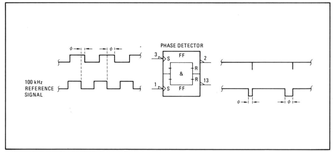


Figure 8-525. Phase Detector Operation
(Variable Input is Lower in Frequency than Reference Signal)

SERVICE SHEET 38 (Cont'd)

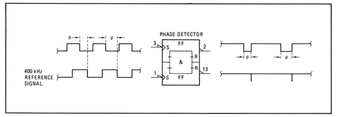


Figure 8-526. Phase Detector Operation
(Variable Input is Higher in Frequency than Reference Signal)

Following the FM Loop Phase Detector are the Switch, Low-Pass Filter, and Integrator circuits. In a phase-locked condition the switch circuit (gates U3A and U3D) is enabled, allowing the output pulses from the phase detector to pass through. The Low-Pass Filter and the Integrator convert the pulses into a voltage. This becomes the FM Loop Error Voltage. Each pulse causes a given amount of charge to be placed on the integrating capacitors, C11 and C12.

When the FM Loop is disabled the switch circuit prevents the phase detector output pulses from reaching the Integrator. To prevent the Integrator's output from slewing against the power supply rails when the FM Loop is disabled, R20 is shunted across the integrating capacitors.

When no modulation signal is applied, the error voltage developed by the Phase Detector Circuit is dependent on the frequency and phase of the 140 MHz VCO. In the phase-locked FM mode the error voltage is also dependent on the instantaneous frequency deviation. As long as the modulation rate is well above the FM Loop's bandwidth, which is about 6 Hz, the error voltage caused by the modulation signal is negligible. Phase-locked FM is possible down to modulation rates of 20 Hz. Modulation rates below 20 Hz result in the gradual cancellation of the modulating signal because the phase-locked loop can now start responding to the modulation signal.

An overmodulation condition exists when the peak deviation of the 140 MHz VCO exceeds the limit or range of the phase detector, U4. This overmodulation condition is detected by monitoring the output of the phase detector. The output is first filtered by a Low Pass Filter consisting of R11 and C7. The output waveform from the low pass filter is similar to a half wave rectified sine wave. This signal is monitored by the Overmodulation Detector (located on the Modulation Drive A4A9) which is a peak detect circuit. If the output waveform from the low pass filter exceeds 1 volt peak, the Overmodulation Detector is triggered.

Internal Modulation Divider

The Internal Modulation Divider divides the 100 kHz signal from the ÷ 100 (Reference) dividers to obtain the 400 Hz and 1000 Hz internal modulation signal. In the 1000 Hz mode counters U7A-U7D are enabled, dividing the 100 kHz signal by a total of 100. In the 400 Hz mode, U7B, U8B, U8C, and U8D are enabled. This combination of dividers provides a divide number of 250.

SERVICE SHEET 38 (Cont'd)

The 1 kHz and 400 Hz control lines are used to select the proper counter combinations. Note, simultaneous 1 kHz and 400 Hz output are not possible. If both the 400 Hz and 1000 Hz control lines are high, all of the counters are disabled and the Int/Ext control line goes high. A high Int/Ext control line indicates that an external modulation source has been selected.

Output Section AGC
A4A7
SERVICE SHEET 37

A4A8 ASSEMBLY

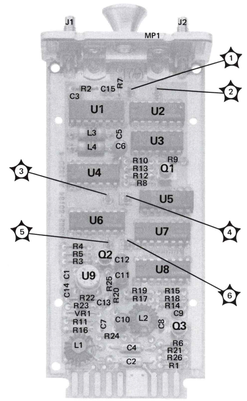
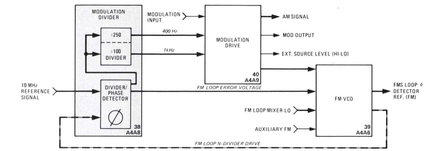


Figure 8-527. A4A8 Modulation Divider Component Locations



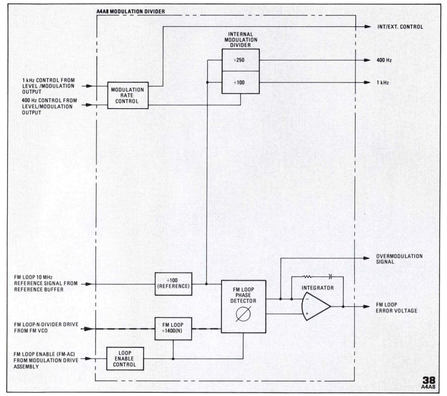
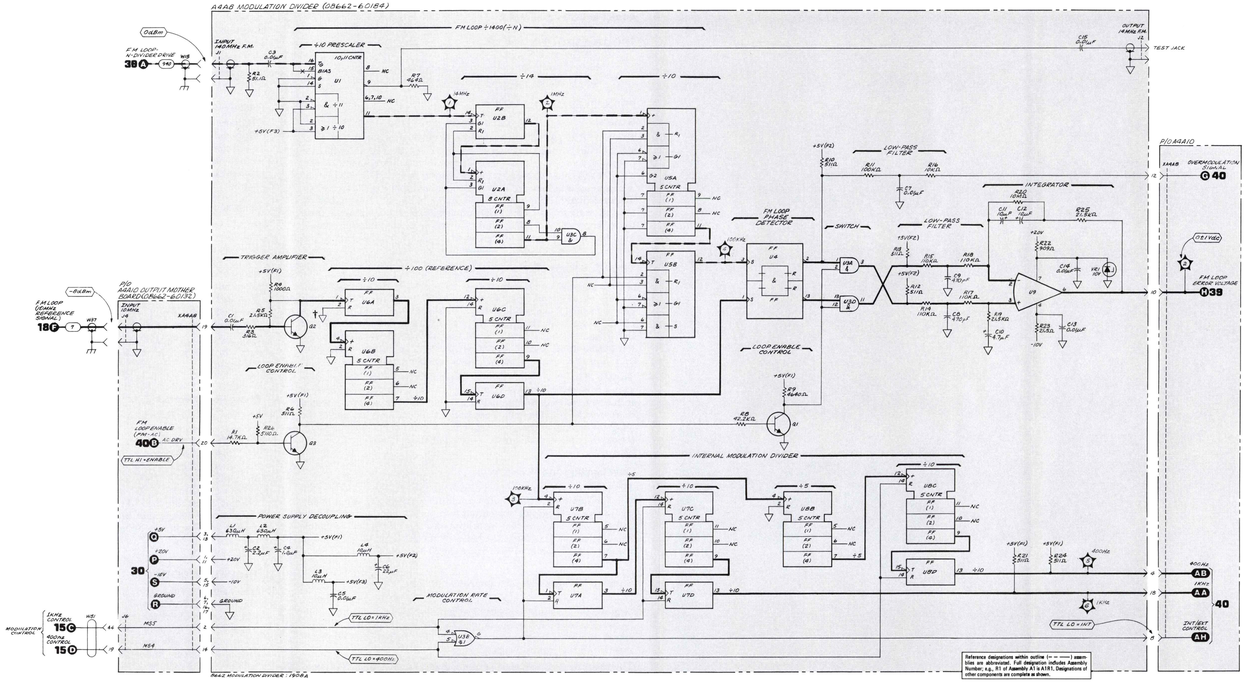


Figure 8-528. A4A8 Modulation Divider Block Diagrams



NOTES

1. TROUBLESHOOTING VOLTAGES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MIGHT BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.

† BRACKETED INFORMATION IN SECTION VII

REFERENCE DESIGNATIONS

NO PREFIX	A4A8
W5,W7,W1	W5 = W7 = W1 A4A8
A4A8	
C1-15 C17 C19 C21-24 C27-29 C31 VR1	

LOGIC LEVELS

LOGIC	TTL	ECL	ECL	CMOS
HIGH (1)	≥ 2V	≥ -1.0V	≥ +4V	≥ VDD
LOW (0)	≤ 0.8V	≤ -1.5V	≤ +4V	≤ 0.1V
0=GROUND, TO OR MORE NEGATIVE THAN ≥ -5.2VDC, TO OR MORE POSITIVE THAN				

INPUT	TTL	ECL	ECL	CMOS
GROUND	LOW (0)	HIGH (1)	HIGH (1)	LOW (0)
OPEN	HIGH (1)	LOW (0)	LOW (0)	X

GROUND = 0VDC, X = UNDEFINED

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1,3	1854-0404
Q2	1854-0071
Q4	1853-0180
Q5	1853-0478
Q6	1853-0221
Q7	1853-0490
Q8-9	1853-0163
U9	1826-0073

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS	
U1	+5V(P3)	4,5
	▽	14
U2	+5V(P1)	5
	▽	10
U3	+5V(P1)	14
	▽	7
U4	+5V(P2)	14
	▽	7
U5	+5V(P2)	5
	▽	7
U6	+5V(P1)	16
	▽	8
U7,8	+5V(P1)	16
	▽	8

38 A4A8

Figure 8-529. A4A8 Modulation Divider Schematic

SERVICE SHEET 39
A4A6 FM VCO ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram F
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The FM VCO (A4A6) generates the frequency modulated 20 MHz signal. The FM signal is generated by applying the modulation signal to the varactor diode that forms part of the oscillator's tank circuit. The FM VCO has two primary outputs. One is the 140 MHz VCO output which is used to lock the loop and the other output is the frequency modulated 20 MHz signal. The 20 MHz FM signal is developed by heterodyning the 140 MHz VCO output with the 120 MHz signal from the Reference Section. The primary inputs are the modulation signals and the FM Loop Error Voltage which is used to lock the loop.

140 MHz Voltage Controlled Butler Oscillator (VCO)

Q1, Q2 and associated components form the 140 MHz Voltage Controlled Oscillator. Q1 is a common-gate FET amplifier with the tank circuit located in its drain circuit. The signal developed in the tank circuit is coupled to the gate of Q2 by C13. Q2 acts as a source follower in the feedback circuit, providing a high impedance at its gate and a low output impedance at its drain. Q2 amplifies the feedback signal and feeds the signal back to Q1 to sustain oscillation.

The 140 MHz VCO is both frequency modulated and phase locked by varying the reverse-bias voltage across the varactor diode. An increase in the reverse-bias voltage reduces the junction capacitance, which increases the resonant frequency of the tank circuit. This causes the VCO to oscillate at a higher frequency. When the FM Loop is phase locked the center frequency is always 140 MHz.

Gain Limiting and Mixer Circuit

The 140 MHz signal developed across the tank is coupled to Limiter, U1. The Limiter acts as a buffer amplifier for the VCO and provides a constant level output. One output from the Limiter is used to phase lock the loop. The other output is applied to the RF port of the double balanced mixer, U2. The Mixer heterodynes the 140 MHz VCO output with the 120 MHz signal to produce the 20 MHz FM signal.

Shaping Network and Shaping Network Bias

Due to the nonlinear tuning characteristic of the varactor diode and the large amount of shunt capacity used in the resonant circuit, a Shaping Network is required. The Shaping Network conditions the modulation signal applied to the varactor to ensure that the frequency change is linear with the applied voltage.

The Shaping Network consist of a ladder of diodes that are reverse biased, in sequence, at a voltage higher than the reverse bias on the diode previous to it. As the input signal level increases (negative

direction) the diodes successively become forward biased, in sequence, and present a lower impedance to the input signal.

The Shaping Network Bias circuit acts as a voltage supply for the resistor-diode network and for Q3. The bias voltage is about +14.1 Vdc.

Voltage to Current Converter

The various input signals (the FM Loop Error Voltage, DC Offset and the modulating signals) are summed at the emitter of Q5. Q5 operates in the common-base mode with the inputs applied at its emitter. The base is biased one diode drop above ground, therefore the voltage at the emitter is approximately zero volts.

Loop and Aux FM Switch

Q6 and Q7 are JFETs used as analog switches. The FM Loop Enable and the Aux FM Switch Drive lines are the control lines that drive the JFET switches either ON or OFF. To maintain the JFET switches in the ON state, the control lines are biased to approximately +9 Vdc. This reverse biases both diodes, CR1 and CR2, and the gates are essentially left floating. To turn the JFET switches OFF, the control lines are biased to approximately −19 Vdc. This voltage forward biases both diodes, and clamps the gates at a negative voltage. This negative voltage at the gates effectively pinches off the JFETs (OFF state).

Loop switch, Q6, is used to disable the FM Loop Error Voltage. The Aux FM switch, Q7, isolates the modulation signal from the Aux FM Input.

Phase Lock Detector

The Phase Lock Detector consists of two comparators that form a window comparator circuit. This circuit determines if the FM Loop Error Voltage lies between two preset voltage limits (the window). R41, R42, and R43 form a voltage divider that establishes the upper and lower voltage limits. The upper and lower voltage limits, +1.39 Vdc and −1.34 Vdc respectively, are applied to the inverting input of comparator U3A and U3B. When the error voltage is within the voltage window, indicating the FM Loop is phase locked, the output from the comparators will remain high. If the error voltage lies outside the voltage window, one of the comparators will go low, turning the Out of Lock Indicator on.

TROUBLESHOOTING

If any components in the 140 MHz Voltage Controlled Butler Oscillators fail, the A4A6 assembly may have to be replaced. Resistors R21-R24 are selected to match the characteristics of the oscillator. Changing a component in the oscillator could change the characteristics enough to require new selected resistors. The selection process requires a special test fixture and is very time consuming; therefore, it cannot be done in the field. To check if a new board is needed, replace the defective component and measure FM distortion with 100 kHz deviation. If FM distortion is within the specifications listed in Table 1-1,

the repair is successful. However, if FM distortion is not within the specifications, the board will have to be replaced. The varactor (CR9) is the most critical component.

Modulation Divider A4A8 SERVICE SHEET 38

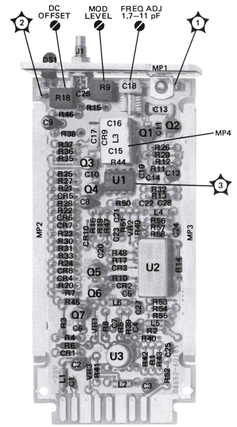


Figure 8-530. A4A6 FM Loop VCO Component Locations

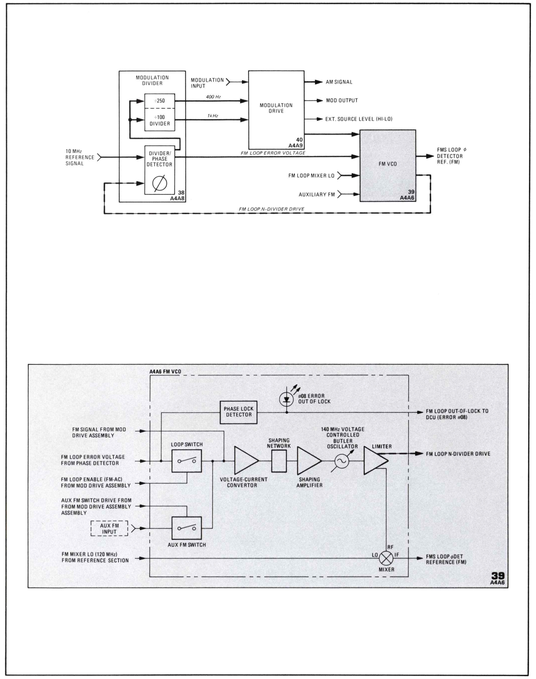


Figure 8-531. A4A6 FM Loop VCO Block Diagrams

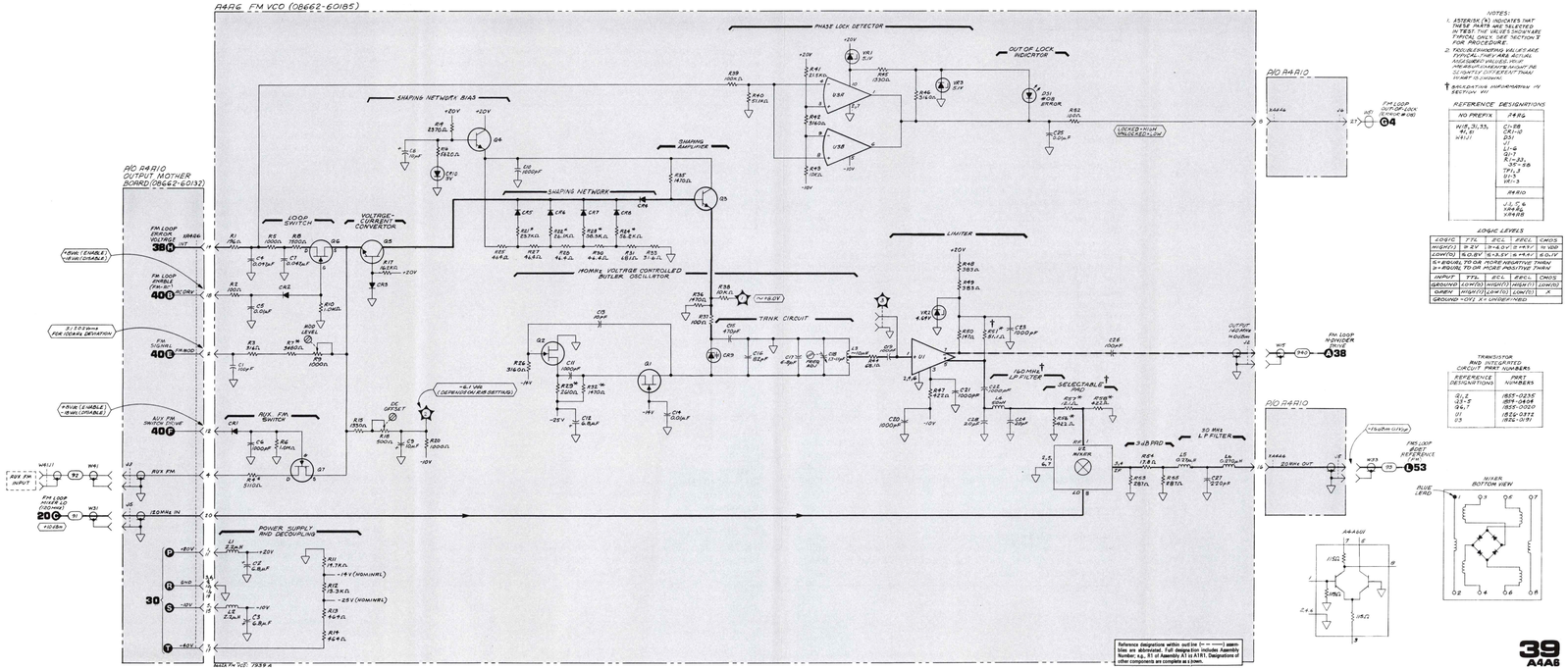


Figure 8-532. A4A6 FM Loop VCO Schematic

SERVICE SHEET 40
A4A9 MODULATION DRIVE

TROUBLESHOOTING HELP

Block Diagram F
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The purpose of the Modulation Drive (A4A9) is to steer the modulation signal to the proper modulating circuits and to vary the amplitude of the modulation signal. The Modulation Drive can accept either internal or external modulation inputs.

The internal modulation signal, 400 Hz or 1000 Hz, comes from the Modulation Divider (A4A8). The signal from the Modulation Divider is a square wave (TTL output). By passing this signal through the appropriate low-pass filter, the square wave signal is converted into a sine wave signal. The sine wave signal is then fed into the Modulation Level DAC. The Modulation Level DAC acts as a digitally controlled potentiometer (attenuator). This circuit controls the amplitude of the modulation signal. The output from the Modulation Level DAC circuit is then routed to the appropriate AM or FM modulation circuits. In the AM mode the amplitude of the modulation signal determines the AM depth. In the FM mode the amplitude of the modulation signal determines the peak deviation.

The external modulation signal is coupled to the Modulation Drive through the front panel Modulation input jack. The external modulation signal can be either AC or DC coupled into the Generator's modulation section. This is controlled by the AC/DC Switch. A 1V peak signal must be applied for calibrated external modulation. The External Source Level Monitor circuit controls the two front panel annunciators which indicate when the applied signal is either above or below 1V peak. For simultaneous FM (internal) plus AM (external) modulation, the external modulation signal is routed around the Modulation Level DAC circuit and applied directly to the AM circuit.

JFET Switches and Switch Drivers

The Modulation Drive uses several JFETs (Q1-4, 6, 13, 14, 16) as analog switches. These JFETs are used to control the passage of analog signals. Figure 8-533 is a block diagram of a JFET used as an analog switch. Switch Drivers (U5, U7, and U8) are used to translate the TTL

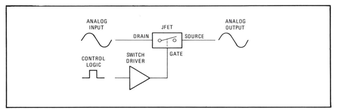


Figure 8-533. Simplified Block Diagram of JFET Used as an Analog Switch

SERVICE SHEET 40 (Cont'd)

level inputs to the appropriate levels to drive the JFET switches on and off. The output from the Switch Drivers swings from approximately −19 Vdc (off) to about +9 Vdc (on).

Figure 8-534 is a schematic of a typical JFET switch and driver circuit.

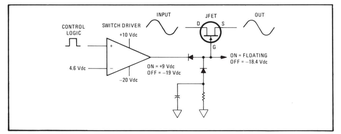


Figure 8-534. Schematic of a Typical JFET Switch and Driver Circuit

To maintain a JFET switch in the ON state, the potential at its gate should be at or near zero volts with respect to its source. When the output from the Switch Driver is about +9 V, both diodes are reversed biased. Since no current can flow through either diode, the gate is essentially left floating. This allows the JFET switch to pass the analog signal.

To drive the JFET switch OFF the Switch Driver's output goes negative by approximately −19 V. This negative voltage forward biases both diodes, clamping the gate at a negative voltage. This negative voltage at the gate effectively pinches off the JFET, preventing the passage of the analog signal.

1 kHz and 400 Hz Low-Pass Active Filter

The 1 kHz and 400 Hz signals from the Modulation Divider (A4A8) are approximately square waves (TTL output). The 1 kHz and 400 Hz Low-Pass Active Filters remove the harmonics from the internal modulation signals to produce purer waveforms (sine waves). Both the 1 kHz and 400 Hz Active Filters are identical in configuration, but the resistor and capacitor values are adjusted for different cutoff frequencies.

DC Offset Circuit

The DC Offset Circuit provides an input offset current to the inverting input of U1C and U1D. This input offset current causes a dc offset at the output of U1C and U1D. This dc offset voltage is used to bias Q11 in its active region. The purpose of Q11 is to amplify the output signal from either the 1 kHz or 400 Hz active filter. Simultaneous 1 kHz and 400 Hz internal modulation rates are not possible in this instrument.

Input Amplifier

The Input Amplifier provides gain and serves as a buffer between the external modulation source and the modulation circuits. The Input Amplifier is a discrete component operational amplifier used in the noninverting configuration. Signal gain is determined by the feedback components R35 and R36. Transistor Q7 and Q8 form a constant

SERVICE SHEET 40 (Cont'd)

current source that provides two precisely matched currents for Q10 and Q9. Q5 serves as an output stage for the amplifier.

External Source Level Monitor

The External Source Level Monitor controls the two front panel annunciators which indicate when the external modulation source is either above or below 1 volt peak. The external source annunciators are only valid if the external source signal is greater than 20 Hz. A repetition rate below 20 Hz causes the external source annunciators to flash (flash rate is dependent on repetition rate).

The External Level Monitor consists of a pair of retriggerable monostables and two comparators which form a window comparator circuit. This circuit determines if the positive peak (E-peak) of the external modulation signal from the Input Amplifier lies between two established voltage limits (the window). As long as E-peak remains within the window the outputs of the monostables U3A and U3B will remain in the high state. If E-peak lies outside the window one of the monostable outputs, depending whether E-peak is above or below 1V peak, will go low signaling the DCU to turn on the corresponding annunciator.

R46 through R50 form a voltage divider network that establishes the upper and lower voltage limits. If E-peak is within the window, comparator U2B will change state every time E-peak crosses the lower voltage limit. This causes monostable U3B to be continuously retriggered so that its output (pin 5) remains in the high state. If E-peak is below the lower voltage limit the output of U2B remains low, disabling U3B. This makes the output of U3B (pin 5) low, causing the DCU to turn on the external source LO annunciator.

If E-peak exceeds the upper voltage limit, indicating that the external source is greater than 1V peak, comparator U2A will go high every time E-peak crosses the upper voltage limit. This causes monostable U3A to be continuously retriggered so that its output (pin 4) remains low. This low causes the DCU to turn on the external source HI annunciator.

Modulation Level DAC

The Digital to Analog Converter (DAC) U9 and operational amplifier U4 form a digitally controlled attenuator. This attenuator is used to vary the level of the modulation signal. The degree of attenuation is determined by the digital input code, MAØ through MA9.

U9 is a 10-Bit DAC that internally consists of a resistor ladder network and a series of analog switches that route currents into a common output node as directed by the digital input code. The magnitude of the output current is dependent on the digital input code and the potential at the Vref input (pin 15). Operational amplifier U4 converts the current from the DAC into a voltage.

Modulation Level Control lines MAØ through MA9 provide a total of 1024 possible attenuation settings, although not all bits are used. A digital input code of 1000 corresponds to the minimum attenuation setting possible in this instrument (see Figure 8-535). All other output

SERVICE SHEET 40 (Cont'd)

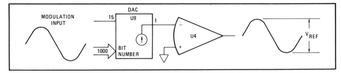


Figure 8-535. Modulation Level DAC at Minimum Attenuation Setting

levels are referenced to this level. For example, for a digital input code of 500 the output level will be 500/1000 (50%) of the reference level. Figure 8-536 illustrates this example. To provide better resolution at lower modulation levels (below 10% of reference level) the x 0.1 Output Switch is enabled to divide the output signal from U4 by a factor of 10. To compensate for this additional attenuation the digital input code is multiplied by a factor of 10 (see Figure 8-536). Multiplying the digital input code by 10 increases the resolution.

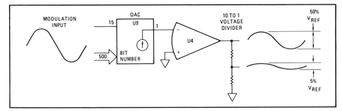


Figure 8-536. Modulation Level DAC at 50% or 5% Output Level

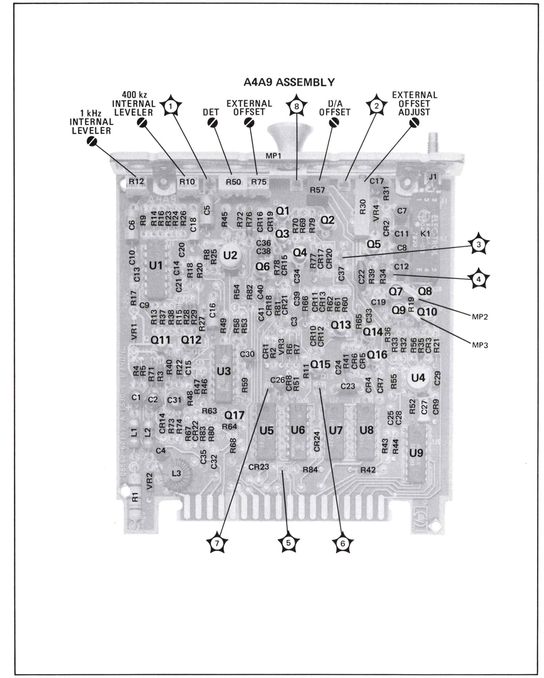


Figure 8-537. A4A9 Modulation Drive Component Locations

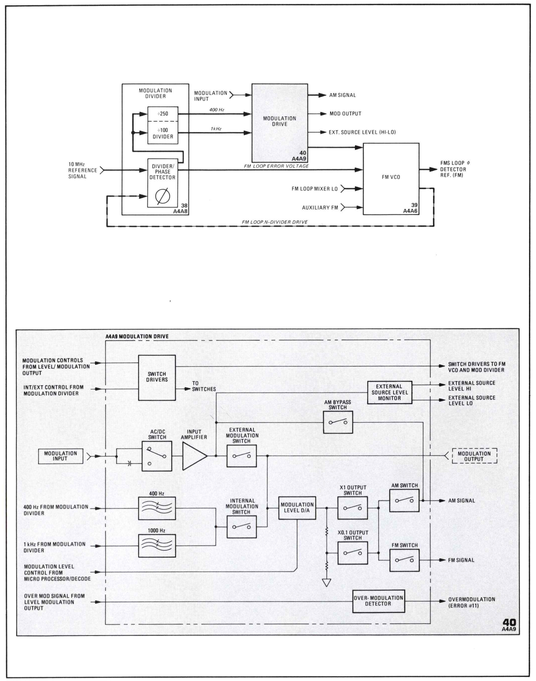


Figure 8-538. A4A9 Modulation Drive Block Diagrams

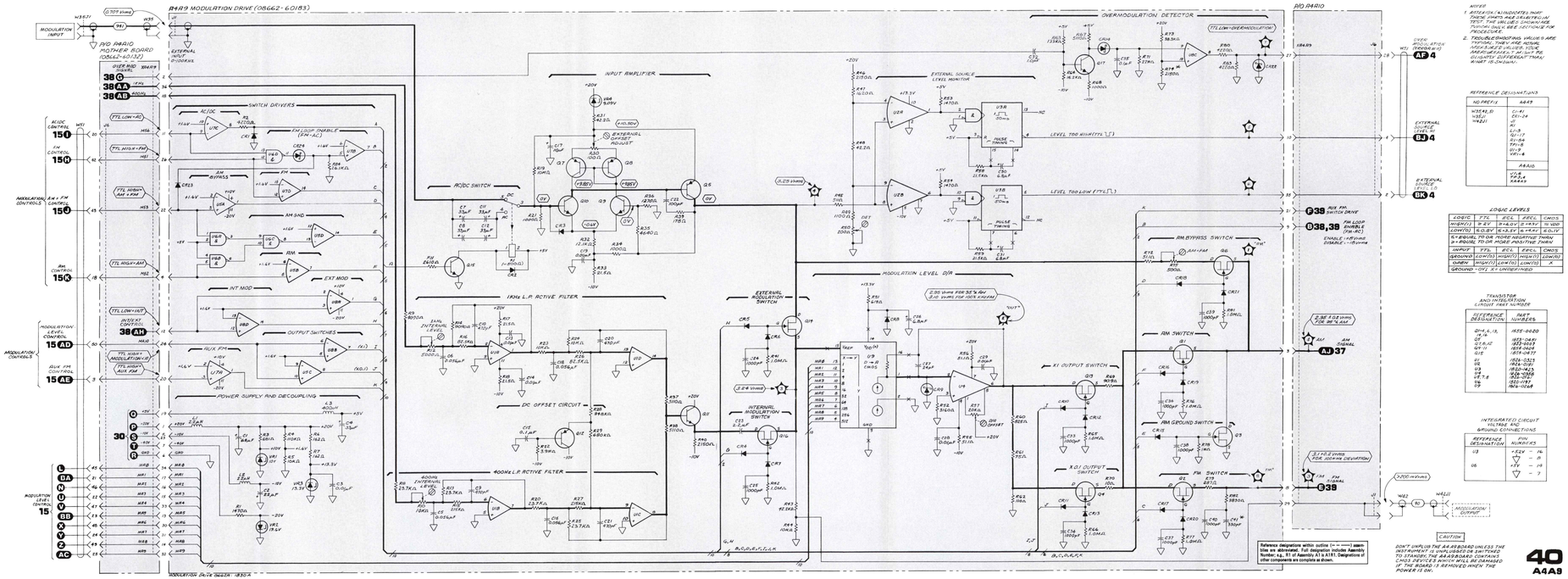


Figure 8-539. A4A9 Modulation Drive Schematic



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FRACTIONAL-N LOOP (SS41 - 45)
LOW FREQUENCY LOOPS (SS46 - 54)
POWER SUPPLY (SS55 - 57)

SERVICE MANUAL

8662A Synthesized Signal Generator

10 kHz — 1280 MHz

P/O Section VIII
Service Sheets

41-57

Fractional-N Loop
Low Frequency Loops
Power Supply
Internal Views



HEWLETT PACKARD

SERVICE SHEET 41
A5A4 FRACTIONAL-N LOOP REFERENCE DIVIDER ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram G
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The Reference Divider divides the 10 MHz reference signal down to 100 kHz which is used as the reference signal to the phase detector. This assembly also generates the sample pulse signal that clocks the sample-hold circuit at the proper time.

Shaper

The shaper network consists of a diode clamping network and a differential amplifier. It provides the analog-to-TTL conversion.

Reference Divider

U1 and U4 form the ÷100 circuit which divides the 10 MHz input signal to produce the 100 kHz phase detector reference signal.

Sample Pulse Generator

The function of the sample pulse generator is to produce a 500 ns pulse that is delayed by 1 μs from the leading edge of the phase detector reference signal. This is accomplished by detecting a state in the ÷100 divider which corresponds to the desired delay time.

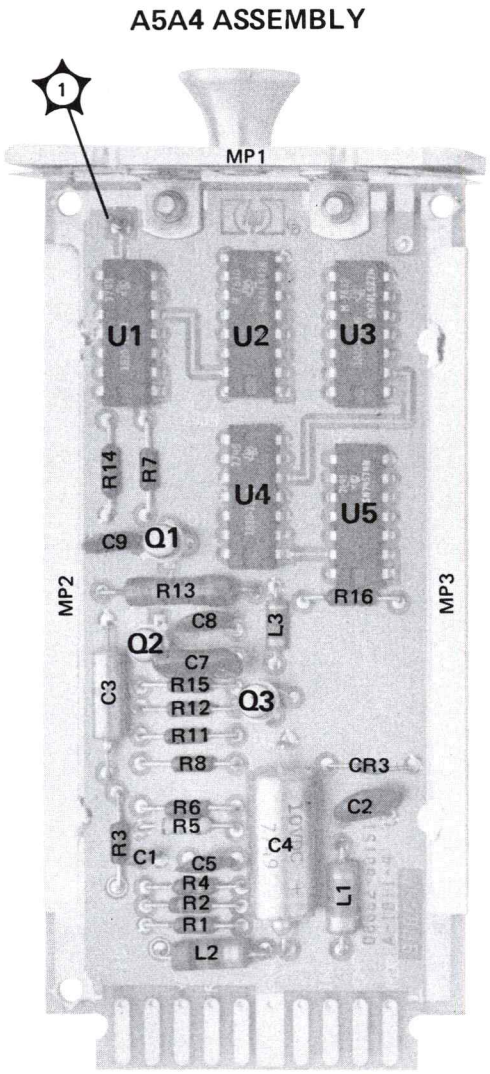
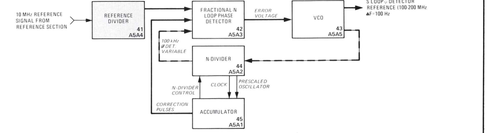


Figure 8-601. A5A4 Fractional-N Loop Reference Divider Assembly Component Locations



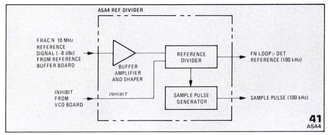


Figure 8-602. A5A4 Fractional-N Loop Reference Divider Assembly Block Diagrams

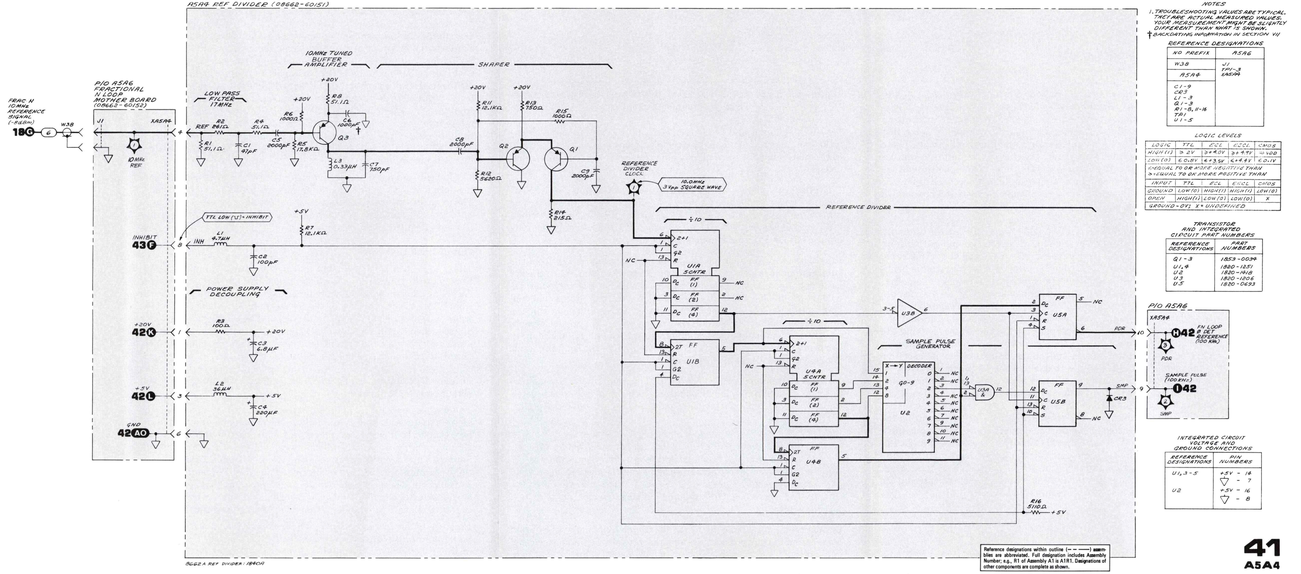


Figure 8-603. A5A4 Fractional-N Loop Reference Divider Assembly Schematic

SERVICE SHEET 42
A5A3 FRACTIONAL-N LOOP PHASE DETECTOR ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram G
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The purpose of the Fractional-N Loop Phase Detector (A5A3) is to develop the FN Loop Error Voltage which is used to tune the VCO. This FN Loop Error Voltage (tuning voltage) is developed by integrating currents from the Phase Detector circuit, the Fractional-N Correction Pulse Width to Current Converters, and the Bias Sink circuit. These currents are integrated together by the Current Summing Amplifier to develop a voltage. The Sample and Hold circuit samples the voltage output from the Current Summing Amplifier once each reference period and at the same time during each reference period. The sampled voltage becomes the FN Loop Error Voltage.

When the Fractional-N Loop (FN Loop) is phase-locked, the tune voltage must be a constant dc value. This means the voltage output from the Current Summing Amplifier must be the same at every sample period. In order to meet this condition the total of the currents being integrated must be the same each reference period. To look at it another way, the currents entering the summing node must equal the currents leaving the summing node in order for the tune voltage to remain constant. This concept, that when the FN Loop is phase-locked, the currents entering the summing node equal the currents leaving the node is true for all conditions, that is, for the condition when the loop runs without a fractional part and for the condition when it has a fractional part. The difference is that when the loop operates with no fractional part the output from the Phase Detector circuit remains constant. However, when the loop operates with a fractional part, the output from the Phase Detector circuit no longer remains constant but varies from reference period to reference period. To compensate for the changing phase detector output the outputs from the Fractional-N Correction Pulse Width to Current Converters must also change. For example, if the Phase Detector circuit supplies less current to the summing node, the Fractional-N Correction Pulse Width to Current Converters must supply more current so that the current entering the summing node is always a constant value.

Phase Detector

The Phase Detector consists of a pair of flip-flops, U5A and B, and gates U4D and U8C. The purpose of the Phase Detector is to generate a pulse width proportional to the phase difference between its two input signals, the FN Loop IF (VCO/N) and the FN Loop Ø Det Reference (reference). Normally the FN Loop operates with a slight phase offset when the loop is phase-locked. This phase offset is due to the constant current being drawn from the summing node by the Bias Sink circuit. Figure 8-604 shows the phase relationship between

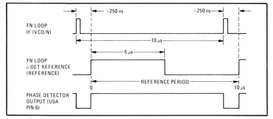


Figure 8-604. A5A3 Fractional-N Loop Phase Detector Input and Output Waveforms (Phase-Locked and No Fractional Part)

the VCO/N signal and the reference signal when the loop is phase-locked and has no fractional part. Note that the two signals are equal in Frequency but are out of phase. This phase offset is normally about 250 ns.

This phase offset causes the Phase Detector (U5A) to generate a 250 ns negative-going pulse every reference period (See figure 8-604). The other Phase Detector output (U5B) is normally only a glitch (which is filtered out) when the loop is phase-locked. U5B should only generate a pulse output during the acquisition of lock.

In a phase-locked condition the amount of current drawn from the summing node is equal to current driven into the node. When the FN Loop operates without a fractional part, the phase detector generates a constant pulse width every reference period. This results in a constant amount of current being driven into the summing node from the phase detector current source (I_{DET}) each reference period. Currents from the Fractional-N Correction circuit (I_1, I_2 and I_3) also remain constant, therefore, the total current entering into the summing node is always a constant value each reference period.

Now when the loop operates with a Fractional part, the VCO/N signal and reference signal no longer equal each other, hence the phase detector no longer generates a constant pulse width each reference period.

NOTE

If the N-Divider (A5A2) is in the divide by N mode, the VCO/N signal starts to lag the reference frequency, which results in a series of decreasing pulse width signals from the phase detector. Conversely, if the N-Divider is dividing by N-1, the pulse width from the phase detector starts to increase.

For example, if the N-Divider is in the divide by N mode, the output pulses from the phase detector start to decrease in duration each reference period. This causes the phase detector current source, I_{DET}, to be connected to the summing node for shorter periods each reference period. At the same time correction current from the Fractional-N Correction circuit is increasing (Correction Pulses duration increasing). The net result is that the decreasing phase detector current is compensated by the increasing correction currents so that the total current contributions from the Phase Detector and the Fractional-N Correction circuits to the summing node are always a constant value.

Level Translators, Diode Switches and Current Sources

Following the Phase Detector are Level Translators, and Diode Switches and Current Sources. These circuits convert the digital outputs from the Phase Detector into currents. There are two types of Level Translators and Current Sources used. One type uses an active current source and a differential amplifier arrangement to switch the Diode Switch on and off. Q4 and U3 form an active current source while CR17 and CR19 form the Diode Switch. Q1, Q2 and Q3 make up the differential amplifier that translates the TTL levels to the appropriate levels required to drive the Diode Switch on and off. When the output from the Phase Detector goes LOW, CR17 is reverse-biased and CR19 is forward-biased, connecting the Current Source to the summing node. In the opposite state when the output is HIGH, CR17 is forward-biased and CR19 becomes reverse-biased, disconnecting the Current Source from the summing node.

The Levels Translator, Diode Switch and Current Source which follow the output of U5B work in a similar manner, as described previously. The major difference is that the active current source is replaced simply by a resistor, and that the level shifting is done with a diode string instead of a differential amplifier.

Out-of-Lock Detector

The Out-of-Lock Detector monitors the two outputs from the Phase Detector to determine if the loop is unlocked. The Out-of-Lock Detector detects two unlock conditions. One condition is when the pulse width from U5A exceeds about 700 ns. The other condition is when the output from U5B exceeds 100 ns. Note that the Loop should never be in a phase-locked condition when U5B generates a pulse. Monostable U7 stretches either the 100 ns or 700 ns pulse to give a continuous indication that an unlocked condition exists.

Fractional-N Correction Pulse Width To Current Converters (Fractional-N Correction)

The purpose of the Fractional-N Correction circuit is to develop the signals that counteract the changing phase detector output when the loop is operating with a fractional part. The Fractional-N Correction circuit is comprised of Level Translators, Diode Switches and Current Sources. These circuits convert the Correction Pulses (TTL levels) from the Accumulator (A5A1) into currents. The Level Translators, Diode Switches and Current Sources are the same types which follow the Phase Detector circuit. For discussion of these circuits, refer to the Section titled Level Translators, Diode Switches and Current Sources.

Each one of the Correction Current Sources, I_1, I_2, and I_3, is connected to the summing node once during each reference period. The sequence of these currents are as follows: Correction current I_3, Correction current I_2, and Correction current I_1. How long each of the Current Sources remains connected to the summing node depends on the negative pulse duration of its corresponding Correction Pulse.

Current Summing Amplifier

The Current Summing Amplifier is an integrator circuit. C34 is the integrating capacitor. When the loop is phase-locked the currents

being integrated are: I_{DET}; I_3; I_2; I_1 and currents from the feedback network C32 and R54.

Due to the different magnitudes of the various current sources and the different times the current sources are connected to the summing node, the output from the Current Summing Amplifier is continuously ramping up and down. Figure 8-605 illustrates the integrator waveform showing the contribution of the different currents.

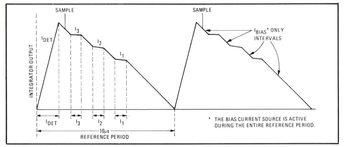


Figure 8-605. Current Summing Amplifier Output Waveform showing the contributions of the different currents.

Sample and Hold

The circuits which make up the Sample and Hold circuit are the Diode Switch, Differential Amplifier, Guard Voltage Network, and the Buffer Amplifier. During each reference period, the four diodes which comprise the Diode Switch are all forward-biased and the output of the Current Summing Amplifier is sampled. This sample voltage (VS) is stored in hold capacitor C47. During the hold period the Diode Switch is reversed-biased and the hold capacitor remains stored. The Buffer Amplifier, U1, which follows the hold capacitor, provides isolation and a low output impedance.

The Buffer Amplifier is a unity-gain, noninverting amplifier. Feedback from this output is fed back to the summing node through C32 and R54 for loop stabilizations.

Switching of the Diode Switch is controlled by the Differential Amplifier. During the sample period, the Sample Pulse line goes high, causing the Differential Amplifier to supply current to the Diode Switch. The Differential Amplifier also provides current to the Guard Voltage Network during the hold period.

The purpose of the Guard Voltage Network is to ensure that the voltage to be sampled does not itself forward-bias the Diode Switch during the hold period. The guard voltages (the collector voltages of Q7 and Q11) are balanced and centered around the last sample voltage. About 2 ma of current flows through the Guard Voltage network during the hold period. This causes a voltage drop of 4 V (guard voltages) across CR28 and R82 and across CR27 and R81 the guard voltages equal +6V and −2V for a sample voltage of +2Vdc (guard voltages = Vs ± 4Vdc).

TROUBLESHOOTING

When a Fractional-N Loop problem has been traced through the block diagram troubleshooting procedure to this assembly, use the following procedure to isolate the cause of the problem.

1. Mount the A5A3 assembly on an extender board from the service kit. Move the slide switch on A5A3 to the TEST position (up) which opens the loop.
2. Monitor TP3 with an oscilloscope. The waveform should be a dc level with small spikes. Measure the frequency of the signal at pin 14 of the edge connector.

   Turn the PRETUNE-GAIN adjustment on the top of the A5A5 VCO assembly while monitoring the frequency at pin 14. Move the frequency above and below 100 kHz and check that the voltage at TP3 goes to the values shown in the following table. If the voltages at TP3 are normal, continue troubleshooting with step 3. Otherwise, there is a problem with the basic phase detector circuitry so continue troubleshooting with step 4.

Edge Connector Pin 14 Frequency (kHz)	A5A3 TP3 (Vdc)	A5A3 TP2 (Vdc)	A5A3 TP1 Vdc)
>100 kHz	+18	+16	+15
<100 kHz	−7	−7	−7

3. Repeat the measurement made in step 2 while monitoring TP2 and then TP1. Compare the measured values to the normal values in the table above.

   If the voltage at TP2 is not normal, the differential amplifier or diode switch is bad. Shorting TP5 and TP5A together holds the amplifier and diode switch in the ON condition for troubleshooting.

   If the voltage at TP1 is not normal but the voltage at TP2 is normal, the problem is in U1 or associated circuitry.
4. Turn the PRETUNE-GAIN adjustment on A5A5 so the frequency at pin 14 of the A5A3 edge connector is greater than 100 kHz. Check that there are pulses on A5A3 TP4.

   Change the frequency at pin 14 to less than 100 kHz. Check that there are pulses on A5A3 TP8.

   If pulses are not present at one of the test points, troubleshoot from U5 to find the cause of the problem. If both pulses are present, the problem is with U2 or associated components.

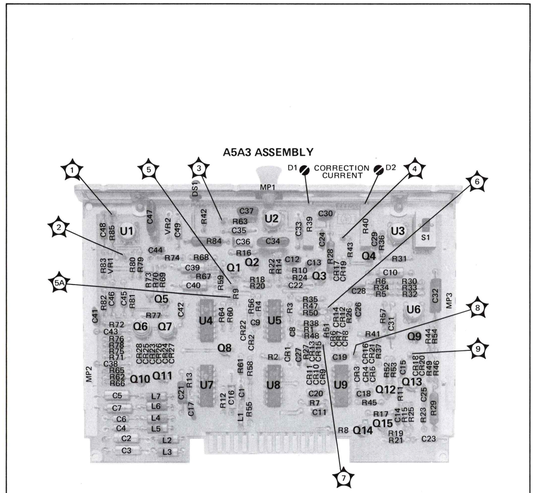


Figure 8-606. A5A3 Fractional-N Loop Phase Detector Component Locations

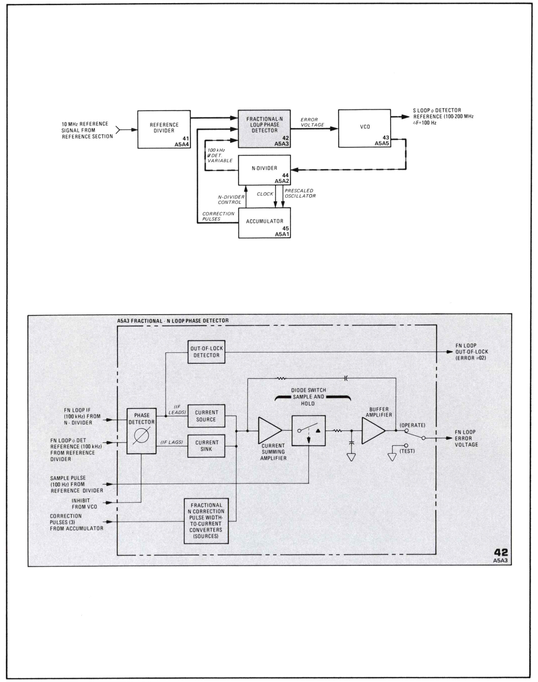


Figure 8-607. A5A3 Fractional-N Loop Phase Detector Block Diagrams

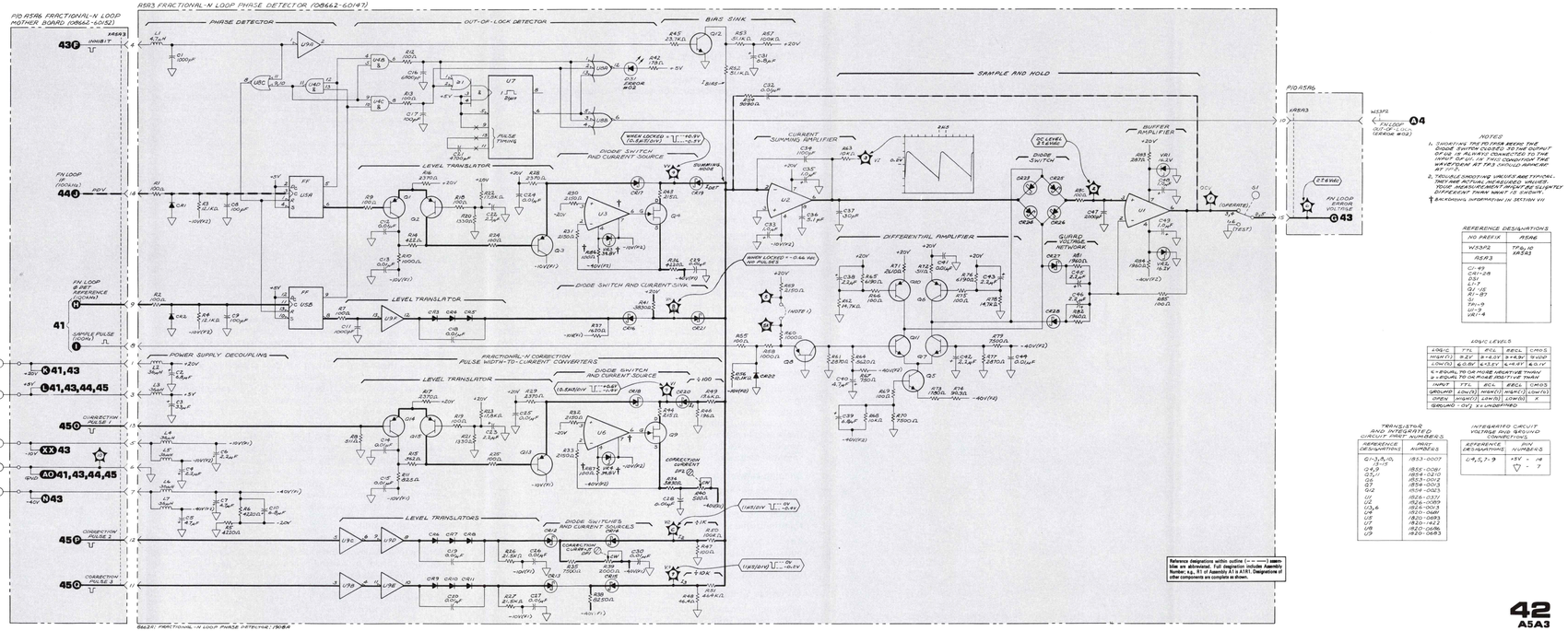


Figure 8-608. A5A3 Fractional-N Loop Phase Detector Schematic

SERVICE SHEET 43
A5A5 FRACTIONAL-N LOOP VCO ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram G
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The purpose of the VCO (A5A5) is to generate an output frequency between 100 MHz and 200 MHz. The primary inputs are the pretune information, Digit Frequency DF4 and DF5, and the FN Loop Error Voltage. The output from the Pretune D/A Converter is used to tune the VCO close to the desired frequency and then the FN Loop Error Voltage is used to phase lock the loop.

Voltage-Controlled Hartley Oscillator (VCO)

Varactors CR10, CR11, and CR12, transistor Q11, and associated components comprise a voltage-controlled Hartley oscillator. Three varactors are used in parallel to provide the wide capacitance range required to tune the VCO. Feedback is obtained by tapping the inductive branch (L7) of the Tank Circuit. C32 and R84 couple the feedback signal back to the emitter of Q11 to sustain oscillation.

The VCO is both pretuned and phase locked by controlling the reverse bias voltage on the varactor diodes. An increase in the reverse bias voltage causes a reduction in the junction capacitance of the varactor diodes. This reduction increases the resonant frequency of the Tank Circuit, causing the VCO to oscillate at a higher frequency.

Signal Splitter and Buffer Amplifiers

The signal developed across the resonant Tank Circuit is coupled to Q6 by tapping inductor L7. Q6 amplifies the signal and applies the signal to the center tap winding of T1. T1 splits the power and adds isolation between the buffer amplifiers. The output from the Loop Buffer Amplifier is used to phase lock the loop. The output from the Output Buffer Amplifier goes to the Low Frequency Loop Section where it is combined with other signals.

Shaping Network

Due to the nonlinear tuning characteristics of the varactor diodes a Shaping Network is required. The Shaping Network conditions the pretune and error signals applied to the varactor in order to ensure that the frequency change is linear with the applied tuning voltage.

The Shaping Network consists of a ladder of diodes that are reverse-biased at successively higher voltage. As the voltage at the collector of Q12 increases, the diodes turn on consecutively and present a lower impedance to the tuning signal.

Current to Voltage Converter

Common-base amplifier Q12 sums the output of the Pretune D/A Converter, current from the +20V source (R53) and the FN Loop Error Voltage from the phase detector. The voltage at the emitter (summing point) is always near zero volts since the base of Q12 is biased one diode drop below ground.

SERVICE SHEET 43 (Cont'd.)

Pretune D/A Converter

The output from the Pretune D/A Converter roughly tunes the VCO to a frequency within the capture range of the phase lock loop. The Pretune D/A Converter cannot, by itself, set the VCO precisely.

Op amp, U1, is connected in the inverting amplifier configuration. Its output voltage is programmed by Frequency Digits DF4 and DF5. Figure 8-609 is a simplified schematic of the Pretune D/A Converter Circuit.

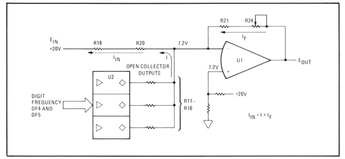


Figure 8-609. Simplified Pretune D/A Converter Circuit

To better analyze how this circuit works, assume that the op amp (U1) is ideal. That is, its gain and bandwidth are both infinity, the input currents and offset are both zero, and there is zero potential difference between the two input terminals. The output voltage, E_{OUT}, is dependent on the feedback current, I_F, that flows through R21 and R24. In the ideal inverting amplifier configuration the feedback current must equal the input current ($I_{IN} = I_F$). The magnitude of the input current I_{IN} is dependent on the potential across R18 and R20. In this circuit the magnitude of I_{IN} remains constant at all times.

If the outputs of U2 are all HIGH (open), there is no current flowing through the pull-up resistors, R11-R16. Hence, the input and feedback currents equal each other. Now, when any of the outputs of U2 goes LOW, current starts flowing into the (−) input node through the pull-up resistors. I_{IN} is no longer equal to I_F, I_{IN} now equaling $I_F + I$. Since the value of I_{IN} has to remain constant, the feedback current has to decrease so equilibrium is maintained. A decrease in I_F causes the output voltage, E_{OUT}, to decrease in magnitude.

Speed Control Circuit

The Speed Control Circuit monitors the output from the Pretune D/A Converter circuit. When a change in the pretune voltage is detected, the Speed Control Circuit drives the J-FET switch (Q9) ON. U4B and U4D are comparators. U4B detects a negative going transition while U4D detects a positive going transition. When either transition is detected, the monostable U3 is triggered. This causes comparator U4A to go HIGH which then turns ON J-FET switch Q9.

Speed-Up Switch and Low-Pass Filter

J-FET Q9 is connected in parallel with R42, so when Q9 is turned ON C27 is allowed to charge or discharge at a faster rate. Hence, voltage

SERVICE SHEET 43 (Cont'd.)

stored on the capacitor tracks the pretune voltage at a faster rate. Q13 and Q14 form a buffer amplifier that couples the pretune voltage to the emitter of Q12.

To maintain the J-FET switch in the ON state, the gate is biased with a positive voltage. To turn the J-FET switch OFF, the gate is biased with a negative voltage.

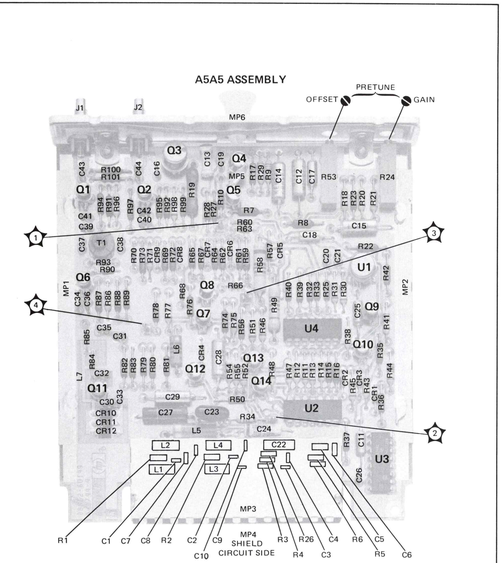


Figure 8-610. A5A5 Fractional-N Loop VCO Component Locations

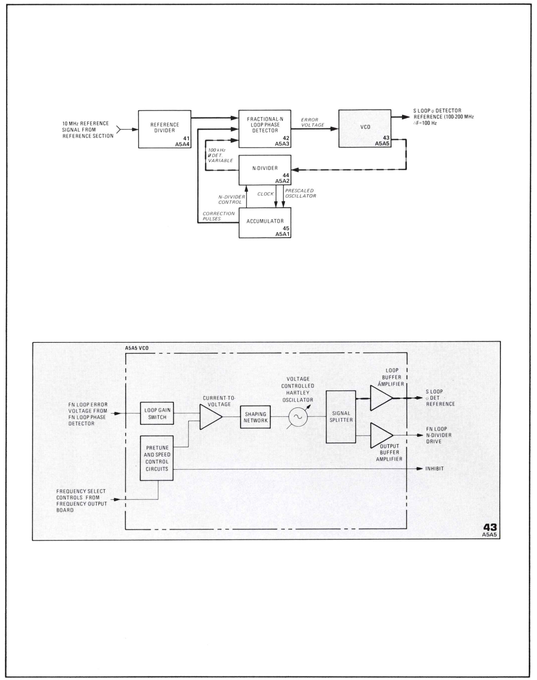


Figure 8-611. A5A5 Fractional-N Loop VCO Block Diagrams

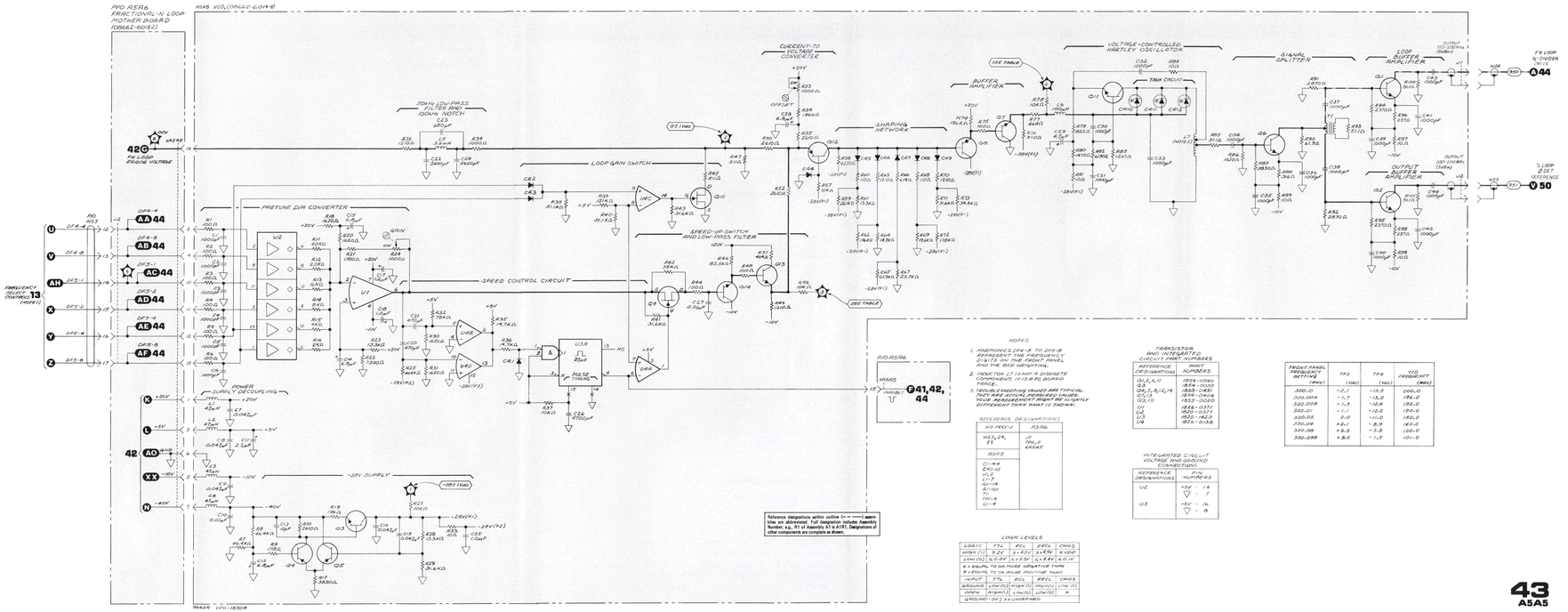


Figure 8-612. A5A5 Fractional-N Loop VCO Schematic

SERVICE SHEET 44
A5A2 FRACTIONAL-N LOOP N-DIVIDER ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram G
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The purpose of the N-Divider (A5A2) is to divide the Fractional N (FN) Loop VCO frequency (FN Loop N-Divider Drive) down to 100 kHz. The 100 kHz output signal, FN loop IF, is one input to the FN Loop's phase detector. The N-Divider consists of programmable digital dividers (counters) which divide down the VCO frequency. The N-Divider can divide by integers from 1001 through 2000. The frequency digits, DF3, DF4 and DF5, determine the divide by N number. In addition the divide by N number can be changed to N-1 by the N-Divider Control (NDC) signal from the Accumulator (A5A1).

Fractional division is accomplished by dividing by N for a number of times and then by N-1 for a number of times. The fractional N is then the average of N and N-1. The N-Divider can divide by a fractional part that has three significant places, for example, a fractional N of 1000.001.

÷ 10/11 Prescaler Counter

The ÷ 10/11 Prescaler Counter, U1, is an ECL device which can be programmed to divide by 11 or 10. At the beginning of each reference period the ÷ 10/11 Prescaler Counter divides by 11. It later starts dividing by 10 and remains in the ÷ 10 mode until the end of the reference period. How long it continues to divide by 11 is determined by the ÷ 10/11 Control Circuit. One output from the ÷ 10/11 Prescaler Counter, the Prescaled Oscillator signal (PSO), goes to the Accumulator (A5A1) where it is used as a clock. Note during the time when the Correction Pulses are generated this clock equals the VCO frequency divided by 10.

÷ 10/11 Control Circuit

The purpose of the ÷ 10/11 Control Circuit is to control the modulus (10 or 11) of U1. Frequency digit DF3 along with the NDC line determine how long U1 divides by 11 each reference period. Frequency digit DF3 presets the Programmable Decade Counter (U8) while the NDC line controls the terminal count of the Terminal Count Decoder (18). Normally the terminal count is 18 except when the NDC line goes high. When the NDC line goes high the terminal count changes from 18 to 17. Changing the terminal count of the Terminal Count Decoder (18) from 18 to 17 effectively causes the N-Divider to divide by N-1.

U8 starts to count up from its preset value to the terminal count. When counter U8 reaches the terminal count the Terminal Count Latch (U7B) is set and on the next clock the Terminal Count Latch output goes high. This causes counter U1 to start dividing by 10.

SERVICE SHEET 44 (Cont'd.)

Programmable Counters

The Programmable Counter counts all the pulses out of the ÷ 10/11 Prescaler Counter. Frequency digits DF4 and DF5 preset the Programmable Decade Counters U6 and U9 respectively. These counters count from the preset count to the count of 196. The count of 196 is determined by the Terminal Count Decoder (196). When the count reaches 196 the Terminal Count Switch is set up to change state on the next pulse from U1. The output from the Terminal Count Switch (U3B) is fed back to reset both the Programmable Counter and the ÷ 10/11 Control Circuit.

When the loop is phase-locked the output from the Terminal Count Switch is a 50 to 100 ns pulse with an average pulse repetition rate of 100 kHz.

TROUBLESHOOTING

When a Fractional-N Loop problem has been traced through the block diagram troubleshooting procedure to this assembly, use the following procedure to isolate the cause of the problem.

There are two types of procedures covered by this procedure.

1. No output pulses produced by A5A2 assembly. Begin troubleshooting with section I of the procedure.
2. Output pulses produced by A5A2 assembly are at the wrong frequency. Begin troubleshooting with section II of the procedure.

No output pulses.

1. Mount the A5A2 assembly on its extender board.
2. Use a logic probe and check for pulses at the outputs of U3B (pins 9 and 7). If pulses are present, the problem is between U3B and the edge connector. If no pulses are present, continue with step 3.
3. Check the output of U2A pin 12 (TP2). This signal should be a TTL pulse train. Check that the signal assumes valid high and low TTL logic levels. If this signal is not normal, the problem is in the prescaler (U1) or translator (U2A), or one of the counters (U6B, U8B, U3B) is pulling down the output of U2A. If this signal is normal, continue with step 4.
4. Connect a jumper between TP4 and TP4A which will allow counters U6 and U9 to free-run. Check that these counters are counting by touching a logic probe to the outputs. Flip-flop U3A should be set. The outputs of U5A (pin 12) and U5C (pin 8) should be normally low but go high when the counters reach the value they are decoding so a logic probe touched to these pins should blink.

   If the counter circuitry is normal, the problem is with the terminal count switch.

Output pulses of wrong frequency.

1. Mount the A5A2 assembly on its extender board.
2. Connect an extender cable from the service kit between A5A2J1 and A3A4J2. This cable routes the output of the LF N-loop to the input of the A5A2 N-divider assembly.

SERVICE SHEET 44 (Cont'd.)

3. Set the 8662A front panel frequency to 327.8 MHz. This sets the LF N-loop output to 200.0 MHz.
4. Short test points TP4 and TP4A together. This holds flip-flop U7B in the set condition (TP1 high) which keeps counter U1 in the ÷ 10 mode. Measure the frequency at TP2 with the high impedance input of a frequency counter. The frequency should be exactly 20.0 MHz. If it is not, the problem is with flip-flop U7B, counter U1 or associated components.
5. Remove the short between TP4 and TP4A. Connect a jumper between TP3 and ground. This holds flip-flop U7B in the clear condition (TP1 low) which keeps counter U1 in the ÷ 11 mode. Measure the frequency at TP2. The frequency should be 18.181818 MHz (200 ÷ 11). If it is not, the problem is with flip-flop U7B, counter U1 or associated components.
6. Remove the jumper from TP3. View the signal at TP1 on an oscilloscope. The waveform should be a TTL negative going pulse approximately 1.1 μsec wide. Set the frequency increment to 100 Hz. Pushing the INCREMENT ↑ key should decrease the pulse width in 55 μsec steps.

   If there are no pulses on TP1, the problem could be the pulses coming from flip-flop U3B. Check TP3 for TTL negative going pulses (approximately 50 μsec wide). The normal period of these pulses is approximately 10 μsec, but any period greater than 1.5 μsec should allow the pulses on TP1, described above, to be produced. If the TP3 pulses are not normal, continue troubleshooting with step 7.
7. Remove the jumper from TP3. Short test points TP4 and TP4A together which makes the output of U2A (pin 12) exactly 20.0 MHz and puts counters U6 and U9 into a free-run mode. The output of U6 (pin 12) should be a 2.0 MHz signal and the output of U9 (pin 12) should be a 200.0 kHz signal.

A5A2 ASSEMBLY

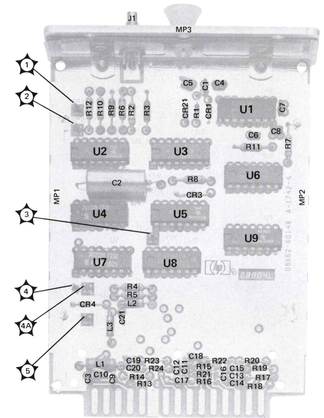
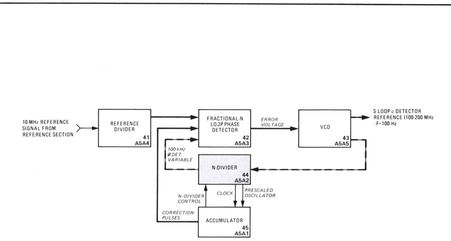


Figure 8-613. A5A2 Fractional-N Loop N-Divider Component Locations



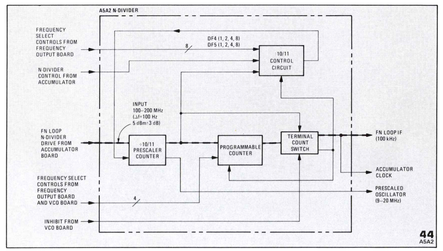
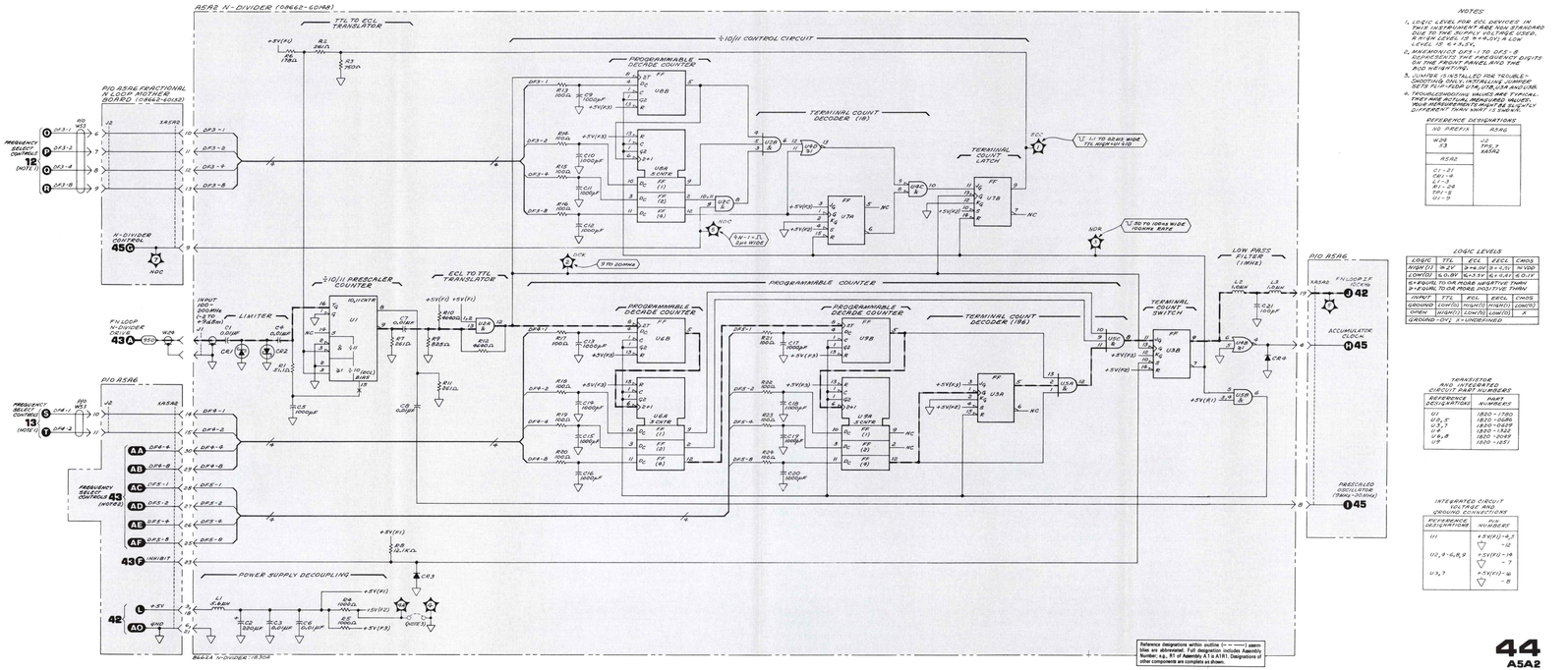


Figure 8-614. A5A2 Fractional-N Loop N-Divider Block Diagrams



NOTES

1. LOGIC LEVELS FOR ECL DEVICES IN THIS INSTRUMENT ARE NON STANDARD DUE TO THE SUPPLY VOLTAGE USED. A HIGH LEVEL IS -1.4 TO -1.0 V, A LOW LEVEL IS -1.8 TO -1.5 V.
2. MNEMONICS DF5-1 TO DF5-8 REPRESENT THE FREQUENCY SELECT CONTROL WORD (BINARY AND THE BCD NEGATIVE).
3. CLOSE 15-INSTALLED PINS "TROUBLE-SHOOTING ONLY." INSTALLING JUMPER SETS TP17=TP18, U7A=U7B, U9A=U9B.
4. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MIGHT BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.

REFERENCE DESIGNATORS

I/O PREFIX	A5A6J
W26	J2
S3	TP5, A5A6J
A5A2	
C1-21	
CR1-8	
J1-3	
L1-5	
TP1-5	
U1-9	

LOGIC LEVELS

LOGIC	TTL	ECL	EECL	CMOS
HIGH (1)	2.2V	-1.0 TO -1.2V	-0.8 TO -1.2V	>0.7VDD
LOW (0)	0.8V	-1.6 TO -1.8V	-1.4 TO -1.6V	<0.3VDD

X = EQUAL TO OR MORE NEGATIVE THAN
Y = EQUAL TO OR MORE POSITIVE THAN

INPUT	TTL	ECL	EECL	CMOS
GROUND	LOW(0)	HIGH(1)	HIGH(1)	LOW(0)
OPEN	HIGH(1)	LOW(0)	LOW(0)	X
GROUND (0V)	X = UNDEFINED			

TRANSISTOR AND INTEGRATED CIRCUIT CHART NUMBERS

REFERENCE DESIGNATORS	PART NUMBERS
U1	1820-1780
U2,5	1820-1608
U3,7	1820-0629
U4	1820-1322
U6,8	1820-2049
U9	1820-1281

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATORS	PIN NUMBERS
U1	+5V(1)-4,7 ▽ -12 ▽ -16
U2,5-6,8,9	+5V(1)-16 ▽ -7
U3,7	+5V(1)-16 ▽ -8

Figure 8-615. A5A2 Fractional-N Loop N-Divider Schematic

SERVICE SHEET 45
A5A1 FRACTIONAL-N LOOP ACCUMULATOR ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram G
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The purpose of the Accumulator (A5A1) is to determine when to ÷ N or ÷ N-1. The Accumulator computes the phase difference between the VCO/N (FN Loop IF) and the 100 kHz reference (FN Loop Reference). This information is used to develop the N Divider Control signal (NDC) and the Correction Pulses. The Accumulator consists of three major sections which are the Algorithmic State Machine, Summing Circuitry, and the Digital to Pulse Converter.

Algorithmic State Machine

The Address Generator along with the State Controller form a small Algorithmic State Machine (ASM). The ASM generates a set of control signals or instructions which properly sequences the Summing Circuitry and the Digital to Pulse Converter. The control signals or instructions are determined by the program stored in ROM (U6).

The ASM generates a total of seventeen instructions. The seventeenth instruction is a halt command which resets and disables the Address Generator (U1 and U2). The ASM remains in the halt state until the end of a reference period. A clock pulse, labeled Accumulator Clock, is generated at the end of each reference period. This pulse restarts the Address Generator and the whole sequence is repeated again.

Summing Circuitry

The fractional portion of the VCO frequency contains the information needed to develop the N Divider Control (NDC) and the Correction pulses. The fractional portion of the VCO frequency is entered into the Accumulator in BCD form (DF0 through DF2). These BCD lines, DF0 through DF2, carry information which corresponds to the front panel frequency digits D0 through D2. The Summing Circuitry takes the BCD data, adds it to the previous sum, and stores it in the Accumulator Registers (U10, U7, and U5). Each reference period the content of the Accumulator Registers is incremented by the fractional portion. The number stored in the Accumulator Registers corresponds to the difference in phase between the VCO signal and the reference signal. When the accumulated total reaches or exceeds unity an NDC signal is generated.

To better understand the operation of the Summing Circuit, let's go through an example. When analyzing the operation of the Summing Circuitry it is better to view it in terms of reference periods. Let's assume that the Accumulator Registers initially contains the number zero and the fractional portion equals the number 207, that is, DF0 = 7, DF1 = 0, and DF2 = 2. At the beginning of the reference period the Input Multiplexer selects the four BCD lines which corresponds to the DF0 and steers the BCD data to the BCD Adder. The BCD Adder adds the DF0 number (7) to the number stored in U5. Since U5 contains the number zero, the resulting sum is just the number DF0. The sum is then latched into U10. At the same time the previous content stored in U10 is shifted into U7 while the previous content of U7 is shifted into U5 (shift right). This sequence is then repeated for both DF1 and DF2, respectively. Figure 8-616 shows the content of the Accumulator Registers after the end of one reference period. Note at the end of the reference period, DF0 is stored in U5, DF1 is stored in U7, and DF2 is stored in U10.

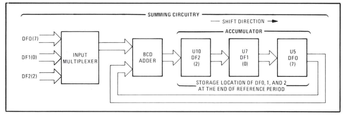


Figure 8-616. Summing Circuitry Simplified Block Diagram Showing the Content of the Accumulator after each Reference Period.

At the beginning of the next reference period DF0 is again selected first and steered to the BCD Adder. DF0 is added to the content stored in U5 which now contains the result of the previous addition of DF0. Again this sequence is repeated for DF1 and DF2. The net result is that the content of the Accumulator Registers is incremented by the fractional portion every reference period. Table 8-601 illustrates this point.

Table 8-601. Accumulator Registers Content Versus Reference Periods

No. of Ref. Periods	FRACTIONAL N LOOP: INTEGER PORTION DF9	...	DF6	FRACTION PORTION (Accumulator Register): DF5	DF4	DF3	DF2	DF1	DF0
0	X		X	X	X	X	0	0	0
1							2	0	7
2							4	1	4
3							6	2	1
4							8	2	8
5	CARRY, NDC COMMAND GENERATED ⟶ 1						0	3	5
6							2	4	2
7							4	4	9

X - IRRELEVANT

Whenever the addition of DF0 and DF1 results in a carry, the carry is circulated back to the BCD Adder and is added to the next most significant digit. The NDC signal is generated only when the addition of DF2 results in a carry. During the interval when the addition of DF2 occurs the N Divider Control Detector receives a clock pulse. This pulse latches the carry information and outputs it to the N Divider (A5A2).

Digital To Pulse Converter

The purpose of the Digital to Pulse Converter is to develop the Correction Pulses 1, 2, and 3. The Correction Pulses are fed into the Fractional-N Loop Phase Detector (A5A3) which develop the signal that counteracts the changing phase detector output. The Digital to Pulse Converter converts the BCD information stored in the Accumulator Registers into pulses. These pulses occur only once during each reference period. The Decoder circuit controls the sequence in which the Correction Pulses are outputed while the Programmable Counter (U3) and the 15 Decoder (U4A and U4C) control the duration or width of the pulses.

The Decoder is comprised of three NAND gates (U12) which form a one to three multiplexer circuit. The Correction Pulses are generated one at a time. The Decoder steers the Correction Pulses to one of the three outputs. The order in which the pulses are outputed is Correction Pulse 3, Correction Pulse 2, and Correction Pulse 1.

The Programmable Counter along with the 15 Decoder determines the pulse width (negative going) of each Correction Pulse. The 15 Decoder circuit causes the counter to reset when it reaches the count of 15. The Programmable Counter is preset by the compliment of the BCD number stored in register U5. The Program Counter is clocked by the Prescaled Oscillator (PSO) signal. During the interval when the Correction Pulses are being developed, the PSO frequency equals the FN Loop VCO frequency divided by ten. The time it takes for the Program Counter to count from its preset value to 15 determines the pulse width. The pulse width can be calculated by the following formula:

Pulse Width = 10 × (number in U5 + 1) × VCO Cycle Wide

For example if U5 contains the number 0, a 10 VCO cycle wide pulse is generated. If U5 contains the number 9, a 100 VCO cycle wide pulse is generated. Note if the FN Loop operates with no fractional part, the pulse width of the Correction Pulses remains constant from reference period to reference period, however if the loop is operating with a fractional part, the Correction Pulses will vary in duration every reference period. Also note, the pulse duration will be the longest when the phase difference is at its maximum value.

TROUBLESHOOTING

When a Fractional-N Loop problem has been traced through the block diagram troubleshooting procedure to this assembly, use the following procedure to isolate the cause of the problem. Signature analysis is used to troubleshoot this assembly. The normal operation of the A5A1 assembly provides the stimulus needed to drive the HP 5004A Signature Analyzer. Any special set-up requirements are listed under the signature tables.

Set-up

1. Mount the A5A1 assembly on an extender board from the service kit.
2. Set the Signature Analyzer switches as follows:

HP 5004A	Pushbuttons
START	⌐ (OUT)
STOP	⌐ (IN)
CLOCK	⌐ (OUT)
HOLD	(OUT)
SELF TEST	(OUT)

3. Connect the Signature Analyzer to the A5A1 assembly as follows:

HP 5004A	A5A1 Assembly
STOP	U11 pin 6
START	U11 pin 6
CLOCK	U2 pin 6
GND	TP4A

4. Run a cable from the Signal Generator rear panel 10 MHz reference output to the A5A2J1 connector.

Initialization

1. Set frequency to 320.0 MHz.
2. Short TP1 and TP1A. Remove any other jumpers connected to these test points.
3. Remove short and connect jumper from U11 pin 6 to TP1A.
4. Set frequency to test value.

Test Procedure

1. Touch the SA probe to +5V on the A5A1 assembly.

signature: OHA5

If this signature is correct, the set-up is correct so continue troubleshooting with step 2. Otherwise, there is a problem with the set-up or the state controller circuitry on A5A1. SA cannot be used until the +5V signature is correct. Troubleshoot the state controller using the information in the timing diagram (Figure 8-617).

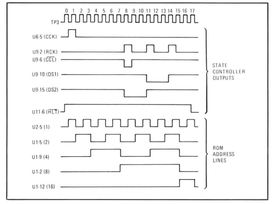


Figure 8-617. State Controller Timing Diagram

2. Check the state controller by verifying the signature at the output of U9. Correct signatures are shown in the signature tables.

If these signatures are correct, continue troubleshooting with step 3. Otherwise, there is a problem in the state controller so check the signatures at U9 (input), U6 and U1 to isolate the cause of the problem.

3. Set the 8662A front panel frequency to 320.0999596 MHz. Short TP1 and TP1A together. Check the signatures at the output of U7 and U10. Correct signatures are shown in the signature tables.

If these signatures are correct, continue troubleshooting with step 4. Otherwise, there is a problem in the summing circuitry so check the signatures at U14, U15 and U16 to isolate the cause of the problem.

4. Perform the initialization procedure for checking U5 specified in the signature table. Check signatures at frequency settings of 320.099960 and 320.099990 MHz. The initialization procedure must be performed each time the frequency setting is changed.

If these signatures are not correct, U5 is the likely cause. Otherwise, the problem is in one of the circuit elements that cannot be checked by signature analysis. Those elements not checked by this procedure are:

U13A	U8A	U12A
U13B	U8B	U12B
U11B	U3A	U12C
	U3B	

5. Set the 8662A front panel frequency to 320.0999596 MHz. This causes all the circuitry on the A5A1 assembly to be active and a logic probe or oscilloscope can be used to check proper circuit operation.

Accumulator (A5A1) Signatures

U1—	1	....	**U5—	9	2P86	U9—	1	....	U14—	7	CFF8
	2	C2C5		10	7U39		2	2P8C		8	....
	3	....		11	729F		3	....		9	C16H
	4	....		12	C16H		4	P8C9		10	P56O
	5	1182		13	0000		5	A6H3		11	P8F5
	6	....		14	0HA5		6	77F8		12	0000
	7	....		15	0000		7	7A6H		13	P8F5
	8	....		16	....		8	....		14	P56O
	9	3409					9	....		15	CFF8
	10	....					10	CFF8		16	....
	11	....	U6—	1	P8C9		11	C16H			
	12	01UF		2	A6H3		12	1C79			
	13	....		3	1C79		13	5CA9	U15—	1	....
	14	....		4	5CA9		14	P56O		2	P56O
				5	2C5F		15	P8F5		3	....
				6	000U		16	....		4	0000
				7	....					5	0HA5
				8	....					6	0HA5
				9	....	U10—	1	....		7	P8F5
				10	21H4		2	....		8	....
				11	1182		3	....		9	P56O
				12	3409		4	P8F5		10	0000
				13	C2C5		5	P56O		11	0000
				14	01UF		6	CFF8		12	0HA5
							7	C16H		13	....
							8	....		14	C16H
			U7—	1	....		9	....			
				2	....		10	2P8C			
				3	....		11	....	U16—	1	....
				4	CFF8		12	59A8		2	P56O
				5	C16H		13	540H		3	....
				6	540H		14	C16H		4	0HA5
				7	59A8		15	CFF8		5	0000
				8	....		16	....		6	0HA5
				9	....					7	CFF8
				10	2P8C					8	....
				11	....	U14—	1	0000		9	C16H
				12	P56O		2	0000		10	0000
				13	P8F5		3	0000		11	0HA5
				14	59A8		4	C16H		12	0000
				15	540H		5	....		13	....
				16	....		6	0000		14	C16H

* Test Frequency 320.09996 MHz
** Test Frequency 320.09999 MHz

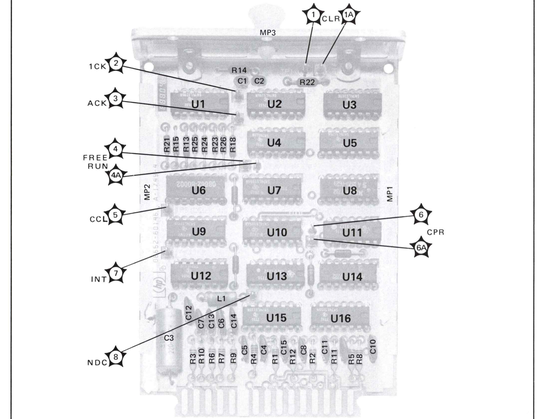


Figure 8-618. A5A1 Fractional-N Loop Accumulator Component Locations

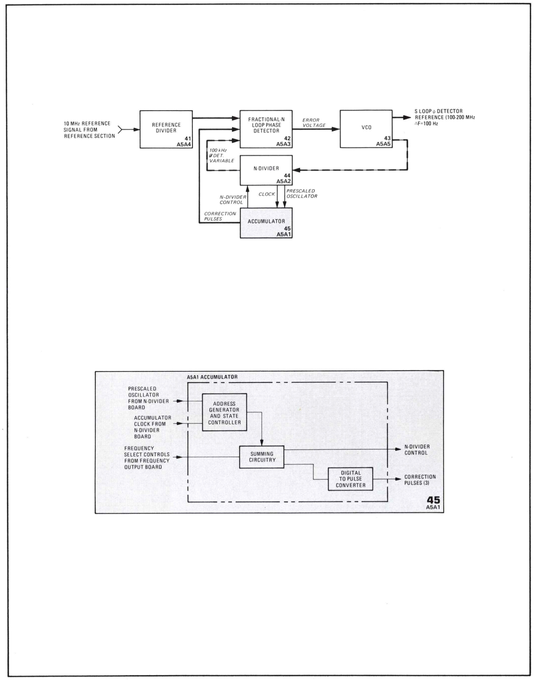


Figure 8-619. A5A1 Fractional-N Loop Accumulator Block Diagrams

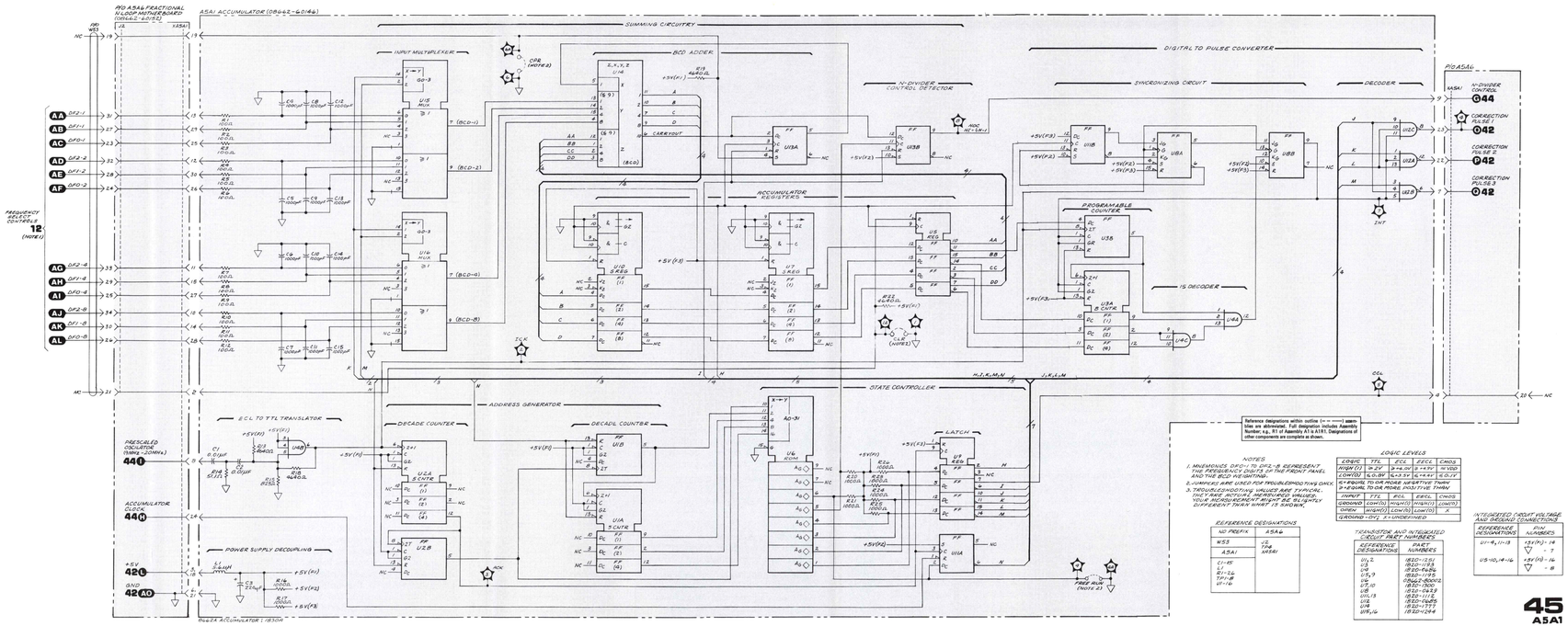


Figure 8-620. A5A1 Fractional-N Loop Accumulator Schematic

SERVICE SHEET 46
P/O A3A3 N LOOP DIVIDER/PHASE DETECTOR ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram H
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

This portion of the N Loop Divider/Phase Detector Assembly contains the N loop programmable divider circuitry. The output (which goes to service sheet 47) is the 10 MHz phase detector variable (VCO frequency divided by N). The inputs consist of the N loop divider drive from the N Loop VCO Assembly (service sheet 48) and the frequency select controls from the Digital Control Unit.

The circuitry on this service sheet takes the 122 MHz to 221 MHz N loop divider drive from the VCO (service sheet 48) and divides it down to 10 MHz by means of the programmable N loop divider. In order to produce the 10 MHz output, the divider circuitry must be capable of dividing the 122 MHz to 221 MHz input by 12.1 to 22.1 in one-tenth of a unit steps.

In order to fractionally divide between 12 and 23, fractional-N circuitry is utilized. The fractional-N divider employs a unique method for generating fractional division. Control circuitry causes the input frequency to be divided by one number for a measured number of cycles and then by another number for a second period of cycles. These two count cycles, when averaged over a period of time, result in a fractional divide count.

Divider Circuitry

The divide by 12 to 23 circuitry is composed of U1-U8 and U12. U1, U2, and U3 make up a divide by 3, divide by 4 circuit. The control circuitry looks at the output of this section and switches back and forth between the two divide modes in order to produce divide values between 12 and 23. For example, suppose a divide value of 17 is desired. The circuit divides by four, two times, and then by three, three times. Thus, for every 17 input pulses, one pulse is produced at the output of U12A.

Control Circuitry (For Fractional-N)

U13, U16, U18, U19, and U20 are the fractional-N control circuits. U13-U19 vary the control signal (TP10) to U20 so that fractional division can be accomplished. U13 adds two to the input. U18 and U19 form the accumulator circuit (U18 is a latch; U19 is an adder). The adder's outputs are at pins 6, 7, 9, 10, and 11. Each time there is an output from the divider (pin 8 of U21), the count sum is added to the least significant digit programmed. Whenever a carry occurs, the divider is triggered to divide by a number that is one greater. In other words, the control circuitry tells the divide by 12 to 23 section when to shift up by one divide number to achieve fractional division.

For example, to obtain a divide by 12.1 value, the divide by 12 to 23 circuit must divide by 12 for 9 divider output cycles and then by 13 for 1 divider output cycle. The U16A output at pin 5 goes to pin 13 of U20. This is the N/N + 1 line. It tells the divider whether it should divide by

SERVICE SHEET 46 (Cont'd.)

N or N + 1. When the line is HI, the circuit is dividing by N + 1, when it is LO, the circuit is dividing by N. (See Fractional-N Loops Section for more detailed description of how Fractional-N works.)

Shift Register and Decoder Circuitry

The shift register and decoder circuitry in the divider section is composed of U6, U7, and U8. U6 generates the appropriate output to control the divide by 3, divide by 4 circuitry. When TP4 is HI, the 3/4 circuit divides by 4. The 12/23 divide number is changed through pin 12 of U7 and pin 6 and 9 of U8 by data from the control section decoder formed by U12. This decoder decodes information from pin 2 and 14 of U20. Signals from gate U4D and pins 2, 3, 14, and 15 of U11 control U7 and U8, the outputs of which are decoded by U6.

ECL to TTL Translator and Squaring Gates

Q3 and Q4 are buffers which convert the ECL output of U12A to TTL levels. The actual output of the divider passes through gates U4A, U4B, and U4C, which square up the output and change the 15% to 20% duty-cycle of the divider output signal to 50%.

TROUBLESHOOTING

When a Low Frequency N Loop problem has been traced through the block diagram troubleshooting procedure to this assembly, use the following procedure to isolate the cause of the problem.

Procedure

1. Mount the A3A3 assembly on an extender board from the service kit. Use an extender cable in place of the short cable running to this assembly. Look at TP15 with an oscilloscope. The signal should be a 10.0 MHz TTL signal (high 80 ns, low 20 ns). Check that the signal at U4C pin 14 is a 10.0 MHz ECL signal.

   If the pulses are there and assume valid logic levels (even though the frequency may be wrong), continue with step 2, below. If there are no pulses (either point stuck high or low, or doesn't assume valid logic levels), trace the signal back to find where the signal goes bad.
2. Set the front panel frequency to 323.3450 MHz. Connect a cable from A5A5J2 (disconnect the cable that is normally connected there) to A3A3J1. This connects the stable output of the fractional N loop to the input of the divider. Measure the frequency of the signal at TP15. The frequency should be 10.0 MHz (± 1 count). If the frequency is correct, the divider is functioning normally so continue with step 6, below. Otherwise, there is a problem with the divider so continue troubleshooting with step 3.
3. Set the front panel frequency to 327.80 MHz. The frequency at TP15 should be 10.0 MHz. This frequency setting programs a divide number of 20.0 and input frequency (from fractional N loop) of 200.0 MHz. If the frequency at TP15 is correct, the problem is with the accumulator circuitry (U13, U19, U18 or U16). Otherwise, the problem is in the basic divider circuitry so continue troubleshooting with step 4.

SERVICE SHEET 46 (Cont'd)

4. Remove jumper W1 (to the left of U2). The frequency at TP5 should be 66.66667 MHz. The 3/4 counter is held in the ÷3 mode with the jumper removed.

   Connect a jumper from +5 V to the top pad where the jumper was connected. The frequency at TP5 should be 50.0 MHz. The 3/4 counter is held in the ÷4 mode with +5 V applied.

   If the counter operates normally, replace the jumper and continue troubleshooting with step 5. Otherwise, there is a problem with U1, U2, U3 or associated components.
5. Set the front panel frequency to 320.80 MHz. Set the frequency increment to 1 MHz. Press the INCREMENT ↑ and INCREMENT ↓ keys and check the frequency digit decoder outputs shown in the table below. If any outputs are wrong, troubleshoot to find the cause. Otherwise, the problem is in one of the shift registers (U7 or U8) or the U6 decoder.

Frequency Digit Decoder Outputs
(Front-panel frequency setting = 320.80 MHz)

1 MHz DIGIT	U11-15	U11-2	U11-3	U4-15	U12-13	U12-9	U12-3
0	H	L	H	L	L	H	L
1	L	H	L	L	L	H	L
2	H	H	L	H	L	H	L
3	L	L	H	L	H	H	L
4	H	L	H	L	H	H	L
5	L	H	L	L	H	H	L
6	H	H	L	H	H	H	L
7	L	L	H	L	H	H	H
8	H	L	H	L	H	H	H
9	L	H	L	L	H	H	H

6. Set the front panel frequency to 326.810 MHz. This setting programs the fractional-N loop output to 190.0 MHz and the A3A3 divide number to 19.0, so the output of the divider should be 10.0 MHz. Set the front panel frequency increment to 0.1 Hz and press the INCREMENT ↑ key. The ERROR LED on top of the A3A3 assembly should blink at a 100 Hz rate and the waveform at TP1 should be a 100 Hz square wave (amplitude ± 0.7 Vdc). Each time the frequency is incremented, the frequency of the blinking LED and the waveform at TP1 will increase by 100 Hz. Press the INCREMENT ↑ key until the frequency display is below 326.810 MHz. The LED and TP1 behave exactly the same as described, above. When the frequency is exactly 326.810 MHz, the signal at TP1 should be a dc value somewhere in the range of ± 0.7 Vdc (most likely value is +0.7 Vdc or −0.7 Vdc). The LED may be either lit or off but should not be blinking. If this circuitry is functioning normally, continue with step 7. Otherwise, there is a problem with the phase detector circuitry so continue troubleshooting this circuitry to find the cause.

SERVICE SHEET 46 (Cont'd)

NOTE

The waveforms shown on the schematic for TP12 and TP13 are taken with the Phase Lock Loop in an out-of-lock condition and are not representative of the waveforms for step 7 of this procedure.

7. Set the front panel frequency to 326.810 MHz and frequency increment to 10 Hz. Look at TP13 on an oscilloscope (DC coupled, 0.5 V/div vertical, 1 msec/div horizontal). There should be no waveform present and the level should be near ground (±1/2 division with the settings given).

   Press the INCREMENT ↑ key. Negative going pulses should appear on TP13 (amplitude of approximately 1.0 V). Pressing the INCREMENT ↑ key again should cause the frequency of the pulses to increase.

   Set the front panel frequency to 326.810 MHz and look at TP12 with an oscilloscope. There should be no waveform present and the level should be near ground (±1/2 division). Press the INCREMENT ↓ key. Positive pulses should appear on TP12 (amplitude of approximately 2.0 V). Look closely since they are faint at the scope settings given, above. Pressing the INCREMENT ↓ key again should cause the frequency of the pulses to increase.

   If either or both of these waveforms is not correct, there is a problem in the frequency detector circuitry. Troubleshoot this part of the circuitry to find the cause of the problem.

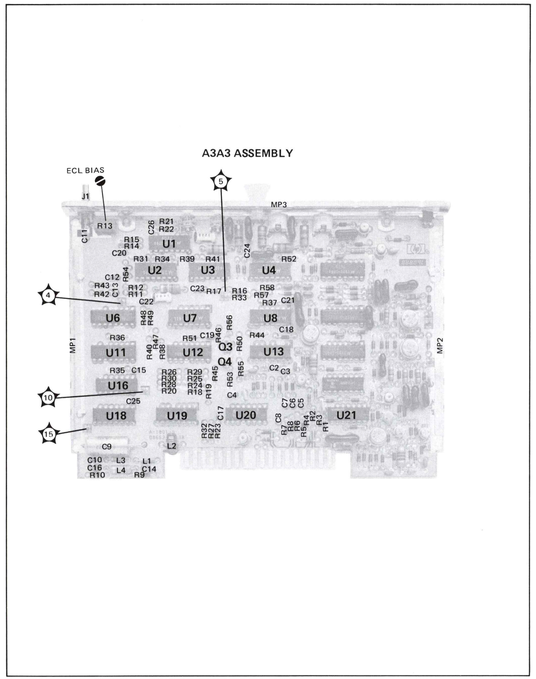


Figure 8-621. P/O A3A3 N Loop Divider/Phase Detector Component Locations

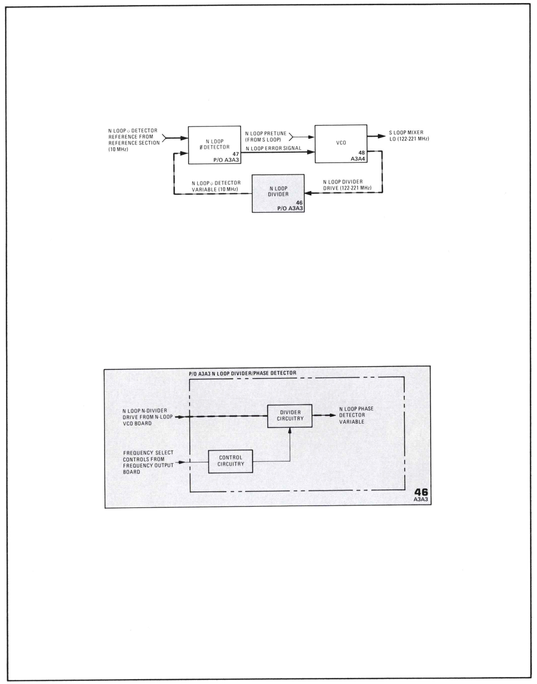
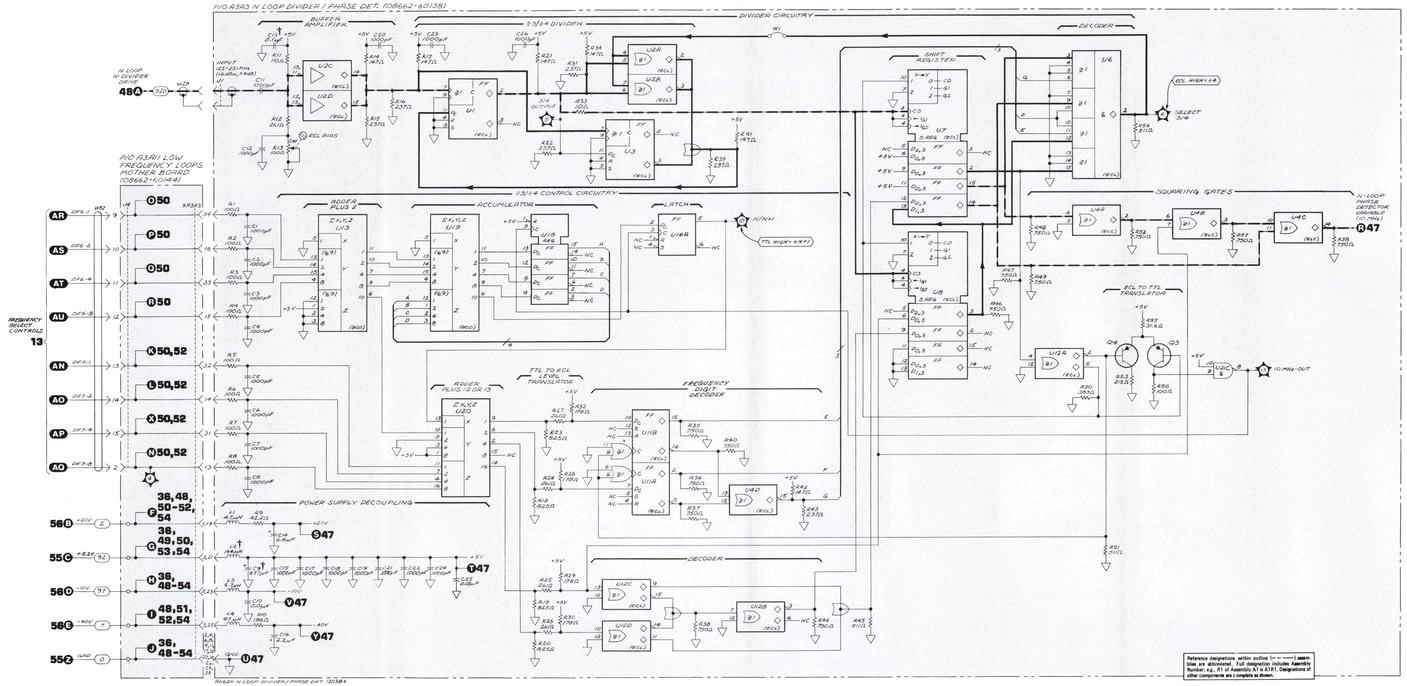


Figure 8-622. P/O A3A3 N Loop Divider/Phase Detector Block Diagrams



NOTES

1. LOGIC LEVELS FOR ECL DEVICES IN THIS INSTRUMENT ARE NON-STANDARD DUE TO THE SUPPLY VOLTAGE USED. A HIGH LEVEL IS 3.4 ± 0.2 V AND LOW LEVEL IS 4.5 ± 0.2 V.
2. MNEMONICS DP0-1 TO DP7-8 REFER TO THE DIVIDE RATIO (TWO DIGITS ON THE FRONT PANEL) USING THE BCD WEIGHTING.
3. TROUBLESHOOTING VOLTAGES ARE TYPICAL; THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MIGHT BE SLIGHTLY DIFFERENT.
4. ▽ INDICATES TOP OF BOARD.
5. BREAKING INDICATION IN SECTION W1

REFERENCE DESIGNATIONS

NO PREFIX	A3J11
W29,52	U4
A3P3	TP4
	XA3A3
C-J46	
U-4	
R3,4	
R14,15,16	
U7-14,15,16	
13,14,A1,A2	
W1	

LOGIC LEVELS

LOGIC	TTL	ECL	EECL	CMOS
HIGH (1)	2.4V	-0.8±0.2 V	4.2±0.2 V	10 VDC
LOW (0)	0.0V	-1.6±0.2 V	3.4±0.2 V	0.0 V

G = EQUAL TO OR MORE NEGATIVE THAN
P = EQUAL TO OR MORE POSITIVE THAN

INPUT	TTL	ECL	EECL	CMOS
GROUND	LOW (0)	HIGH (1)	HIGH (1)	LOW (0)
OPEN	HIGH (1)	LOW (0)	LOW (0)	X

GROUND = 0 V, X = UNDEFINED

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	HP PART NUMBERS
Q3,4	1853-0034
Q5,8	1820-0798
Q6,7	1820-0796
Q9,10	1820-0802
U1,2	1820-0817
U3	1820-0801
U5,19	1820-1777
U6	1820-0797
U7	1820-0793
U8	1820-0809
U21	1820-0681

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U1-4,6, 11,12	+5V - 14 ▽ - 8
U5,16,19	+5V - 8 ▽ - 4
U16,21	+5V - 14 ▽ - 7
U20	+5V - 5 ▽ - 12

Figure 8-623. P/O A3A3 N Loop Divider/Phase Detector Schematic

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P/O A3A3

SERVICE SHEET 47
P/O A3A3 N LOOP DIVIDER/PHASE DETECTOR ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram H
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

This service sheet contains the circuitry for the phase detector portion of the N loop. Inputs include the 10 MHz N loop phase detector reference signal from the reference section (service sheet 18) and the 10 MHz phase detector variable from the N Loop Divider (service sheet 46). The phase detector reference signal splits and goes to both the phase and frequency detector circuits, as does the phase detector variable signal. The outputs from this section are phase and frequency error signals which are sent to the N Loop VCO (service sheet 48).

Frequency Detector Circuitry

The frequency detector circuitry determines if the frequency at the output of the N loop divider is above or below the 10 MHz reference signal. If the N loop frequency is more than several MHz from the reference, the loop won't lock by itself because the signal is out of the phase detector's range. The frequency detector section determines which direction to tune the frequency so that the signal is within the phase detector's range. Q1 and Q2 form the 45° phase shifter circuits. U5, U9 and U14 are used as dual exclusive-or gates.

Of the two 45° phase shifter circuits, one shifts the detector reference signal in the +45° direction and the other shifts in the −45° direction. This puts the resulting signals to the dual exclusive-or gates 90° out of phase with each other. The exclusive-or gates function similarly to double-balanced mixers. The signals at their outputs are filtered by the 2 MHz low-pass filters. These filtered outputs are the difference frequencies between pin 10 on U5D and the reference divider inputs to Q1 and Q2. The signals sent to the comparators are triangle waves and are measurable at TP7 and TP9, where the phase difference is still 90°. These triangle waves are converted to square waves by comparators U10 and U15. The outputs from these comparators enter U16, a control flip-flop.

If TP11 goes HI when TP8 is LO, then a LO is transferred to pin 9 of U16B to trigger monostable U17A. U17A produces a 4.5μs pulse that turns OFF Q6 and causes CR11 and CR12 to turn ON. Q6 turns OFF when CR9 turns ON, which occurs when pin 13 goes HI and pin 4 goes LO. Current flows from the summing junction of the N Loop VCO, causing the frequency to go up. At the same time, pin 5 of U17B is LO. This keeps CR10 OFF so that no current flows into the junction of R119 and R120. When the loop is locked, U17A and U17B are not triggered and there is no current flowing through R118, R119, or R121. When pin 5 of U17B goes HI, current is sent to the junction through CR10 and the frequency decreases.

SERVICE SHEET 47 (Cont'd)

Phase Detector Circuitry

The input to the phase detector section is composed of limiters Q5 and Q10. These produce square waves at TP14 and TP16. From here the signals enter the phase detector formed by Q11 and Q12. This phase detector acts like an exclusive-or gate. When TP14 and TP16 have different voltages (either Q5 or Q10 is HI) one of the two phase detector transistors turns ON and sums current into R85 and R86, causing the emitter of Q9 to go HI. The output voltage from Q9 is LO when both inputs are the same.

Q9 is used in a low impedance emitter-follower configuration and acts to drive the 1 MHz and 6 MHz notch filters. The six notch filters (which follow Q9) filter the spurs generated in the N loop fractional-N circuitry. These spurs occur at sub-multiples of the reference frequency. CR5 and CR6 limit the phase range over which the phase detector can tune the oscillator. The phase error signal at pin 10 goes to the summing junction on the N Loop VCO Assembly (service sheet 48).

Out-of-Lock Circuitry

When the output of the phase detector is HI(indicating an out-of-lock condition), the TTL level translator formed by Q8 and U21 turns ON Q7, causing the out-of-lock lamp to light.

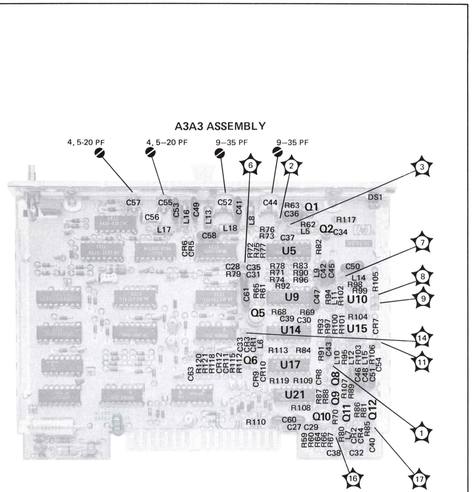
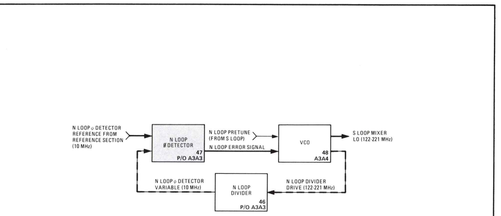


Figure 8-624. P/O A3A3 N Loop Divider/Phase Detector Component Locations



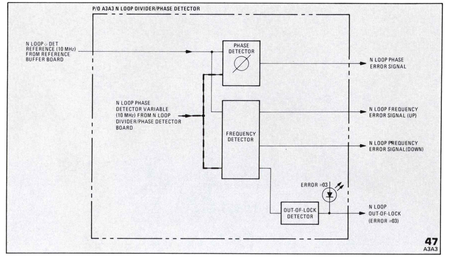
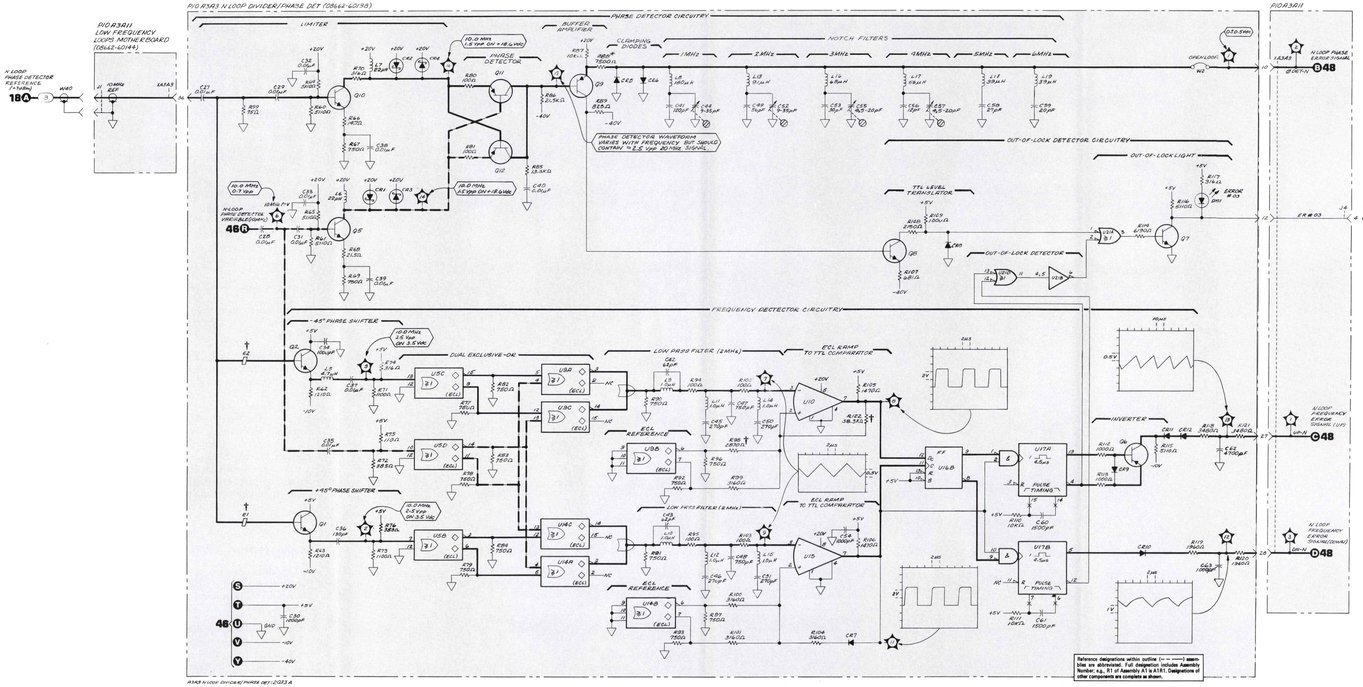


Figure 8-625. P/O A3A3 N Loop Divider/Phase Detector Block Diagrams



NOTES

1. LOGIC LEVELS FOR ECL DEVICES IN THIS INSTRUMENT ARE NONSTANDARD DUE TO THE SUPPLY VOLTAGE USED. A HIGH LEVEL IS −0.8V; A LOW LEVEL IS −1.8 V.
2. TROUBLESHOOTING VALUES ARE TYPICAL. ACTUAL VALUES MAY VARY. WHEN MAKING MEASUREMENTS, INSERT 20 Ω SCALLY DIFFERENT THAN WHAT IS SHOWN.
3. ASTERISK (*) INDICATES THAT THESE PARTS ARE SELECTED. TYPICAL VALUES SHOWN ARE TYPICAL ONLY. SEE SECTION V FOR PROCEDURE.

† BRACKETING (WIDER) SHOWN IN SECTION VII

REFERENCE DESIGNATIONS

NO PREFIX	A3A3 CONT
W40	TP1-3,6-9
W50	U2,3,5,6, 12-15, 18-20
A3A3	MP1
C67-69 C71-74 C111	A3A11
E1,2 E5,6,9 E11-12 E59-182	J2,3 J4 XA3A3

LOGIC LEVELS

LOGIC	TTL	ECL	FECL	CMOS
HIGH(1)	2.4V	3 to 4.5V	3 to 4.8V	70 10V
LOW(0)	0.0.8V	0 to 3.5V	0 to 4.4V	0.01V
0 = BIGGEL TO OR MORE NEGATIVE THAN				
1 = BIGGEL TO OR MORE POSITIVE THAN				
INPUT	TTL	ECL	FECL	CMOS
GROUND	LOW(0)	HIGH(1)	HIGH(1)	LOW(0)
OPEN	HIGH(1)	LOW(0)	LOW(0)	X
GROUND =0V, X = UNDERMINED				

TRANSISTOR AND INTEGRATED CIRCUITS PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1, 2, 3, 8	1854-0404
Q5, 6	1854-0243
Q4	1853-0007
Q7, 9, 10	1853-0041
U1	1820-1801
U2, 14	1820-1802
U3, 15	1820-0124
U4	1820-0493
U7	1820-0819
U11	1820-2081

INTEGRATED CIRCUITS VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U1, 11, 14	+5V = 14 ⏚ = 8
U14, 21	+5V = 14 ⏚ = 7
U17	+5V = 16 ⏚ = 8

47
P/O A3A3

Figure 8-626. P/O A3A3 N Loop Divider/Phase Detector Schematic

SERVICE SHEET 48
A3A4 N LOOP VCO ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram H
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

This service sheet contains the voltage controlled oscillator and associated circuitry for the Low Frequency N Loop. There are four frequency control inputs to this board and two outputs. The outputs extend from 122 MHz to 221 MHz. One output is the N loop N-divider drive, the other is the S loop mixer local oscillator input. The frequency control inputs are summed, shaped, amplified, and filtered before being used to control the frequency of the voltage controlled oscillator.

Current Summing Junction

The inputs to this assembly go through a summing junction and are amplified by Q10. Q10 converts the summed currents to a control voltage.

One of the four inputs is a pretune (pin 15) that coarsely tunes the oscillator to within a couple of MHz of the correct frequency for locking. The other three inputs are loop signals. The signal at pin 11 is the phase error signal from the phase detector that is located on the N Loop Divider Board. The other two signals are from the frequency detector circuitry on service sheets 46 and 47. One of them sums current into the summing junction and makes the frequency decrease, the other one removes current from the emitter of Q10 and makes the frequency increase. These inputs are at board pins 10 and 9, respectively. The pretune line has a gain adjustment which allows the range of the VCO to be set. The maximum tune range is approximately 100 MHz with the 7 volt (maximum) pretune voltage.

Shaping Network and Buffer Amplifier

The shaping network (in the collector circuit of Q10) is a diode-resistor network composed of CR2, CR3, R12, R13, R16, and R19. This network shapes the VCO pretune voltage so that a change in voltage causes a linear change in the VCO output frequency.

Following the shaping network is an emitter-follower stage formed by Q6. It drives the filter network that removes the spurious signals from the loop and drives the phase lag network consisting of R29, R31, and C19. The actual varactor voltage (at TP2) goes through R33 to the oscillator tank at CR7 and CR8. This is a negative voltage of between −2 volts and −18 volts (−2 volts is the limit for the low frequency end and −18 volts is the limit for the high frequency end).

SERVICE SHEET 48 (Cont'd)

Gain Set Switch

Q9 is a transistor switch that increases the loop gain voltage as determined by the conduction threshold of CR3. When Q9 turns ON, it shunts R25 so that the gain from the emitter of Q6 to TP2 is increased by approximately 6 dB. This causes loop gain to increase and compensate for the decrease in capacitance of the varactors, which occurs close to the high frequency end.

Charge-Discharge Switch

Transistors Q5 and Q8 switch current into C19 through R26 and R31. These transistors are biased so that when the voltage at TP4 is 2 volts greater than the voltage on C19, either Q5 or Q8 turn ON and quickly charge C19. This increases switching speed.

Voltage Controlled (Hartley) Oscillator

The oscillator itself is formed by Q7, which is a common gate FET amplifier. Capacitor C22 is a bypass capacitor for the varactors. L8 is a tapped inductor. The feedback loop feeds through C24 to the source of the FET. R27 and R28 set the dc current in the FET.

Signal Splitter

The output of the VCO is tapped from inductor L8 very close to ground and goes through R34 to transformer T1, which is a power splitter. This splitter supplies half-power to each of the two amplifiers and provides substantial isolation between them.

Output and Loop Buffer Amplifiers

The two buffer amplifiers are identical. The loop buffer amplifier consists of Q3 and Q1 and the output buffer amplifier consists of Q4 and Q2. The two transistors within each amplifier assembly are cascaded. The output of each amplifier is attenuated by a 3 dB pad before being output from the assembly. One of the outputs is sent to the N loop divider to provide feedback to the N loop phase detector; the other is sent to the sum loop mixer (LO input).

Minus 26 Volt Supply

The −26 volt on-board supply is derived from the main −40 volt supply. It is used as a reference voltage (for the frequency breakpoints) by the shaping network.

P/O N Loop Divider/Phase Detector
A3A3
SERVICE SHEET 47

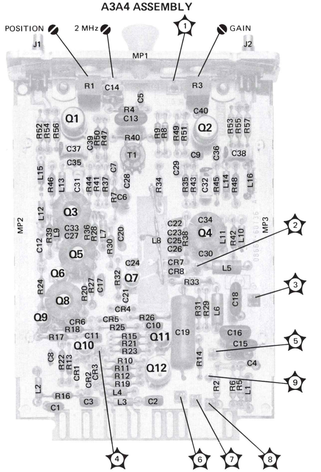
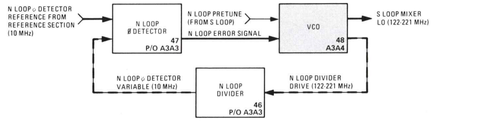


Figure 8-627. A3A4 N Loop VCO Component Locations



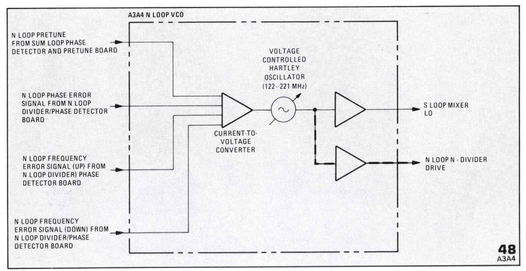
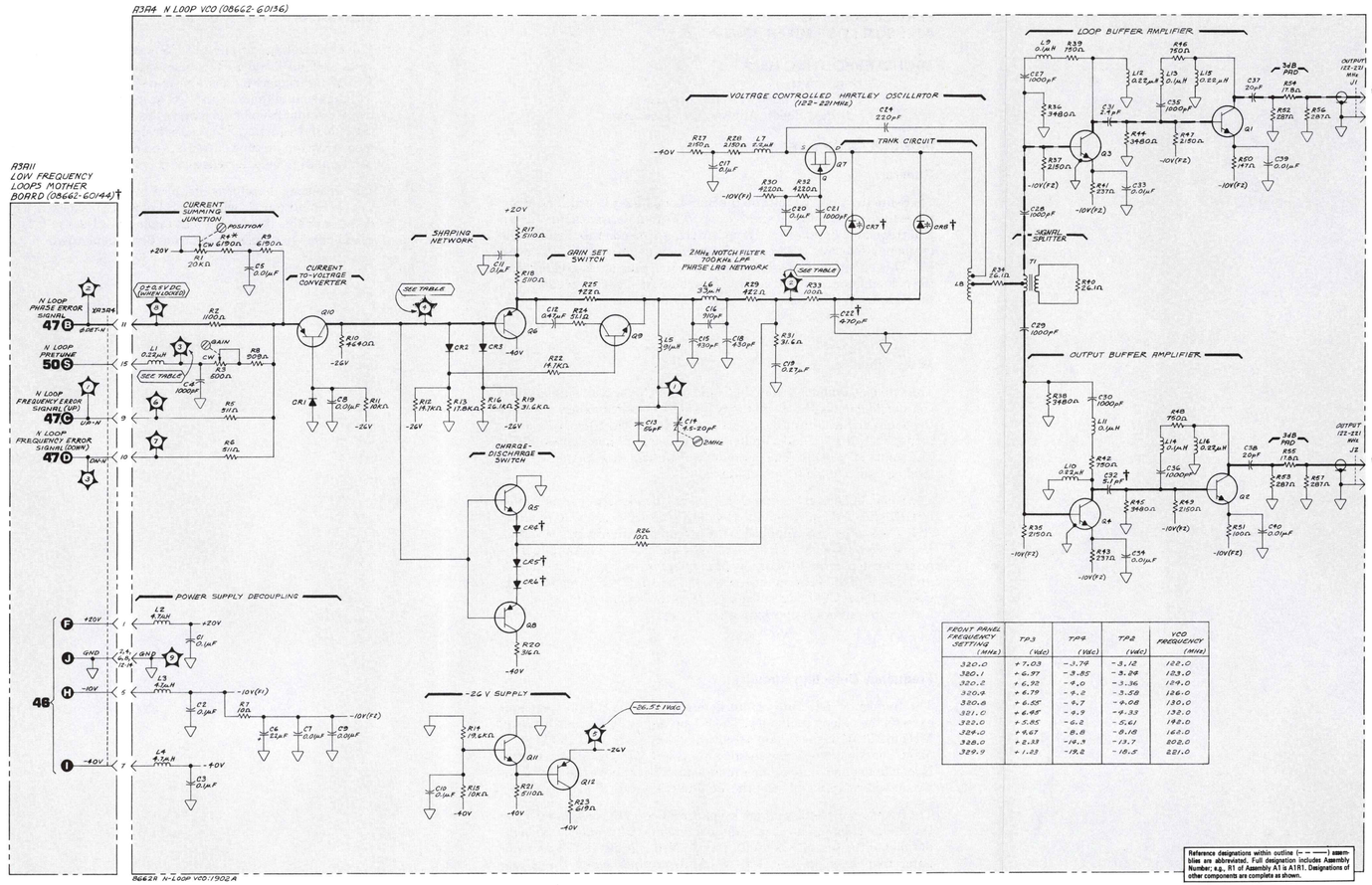


Figure 8-628. A3A4 N Loop VCO Block Diagrams



NOTES

1. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MIGHT BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
2. ASTERISK(*) INDICATES THAT THESE PARTS ARE SELECTED AT TEST. THE VALUES SHOWN ARE TYPICAL ONLY. SEE SECTION V FOR PROCEDURES.
† BACKDATING INFORMATION IN SECTION VII

REFERENCE DESIGNATIONS

NO PREFIX	A3A4
W29,30	C1-22,24 27-40 CR1-8 J1,2 L1-6 Q1-12 R1-57 T1 TP1-9
	A3A11
	TP1-3 XA3A6

NOT ASSIGNED: C23, C25, C26

FRONT PANEL FREQUENCY SETTING (MHz)	TP3 (Vdc)	TP4 (Vdc)	TP2 (Vdc)	VCO FREQUENCY (MHz)
320.0	+7.03	-3.74	-3.12	122.0
320.1	+6.97	-3.85	-3.24	123.0
320.2	+6.92	-4.0	-3.36	124.0
320.4	+6.79	-4.2	-3.58	126.0
320.6	+6.55	-4.7	-4.08	130.0
321.0	+6.45	-6.9	-4.33	132.0
322.0	+5.85	-6.2	-5.41	142.0
324.0	+4.67	-8.8	-8.18	162.0
328.0	+2.33	-14.3	-13.7	202.0
329.9	+1.23	-19.2	-18.5	221.0

TRANSISTOR PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1,2	1854-0297
Q3,4	1854-0395
Q5,6,11	1854-0404
Q7,8,10	1853-0451
Q9	1855-0236
Q12	1853-0012

Q7 BOTTOM VIEW

Reference designations within outline (– – – –) assemblies are abbreviated. Full designation includes Assembly Number; e.g., R1 of Assembly A1 is A1R1. Designations of other components are complete as shown.

48 A3A4

Figure 8-629. A3A4 N Loop VCO Schematic

SERVICE SHEET 49
A3A5 SUM LOOP MIXER ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram H
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

There are two main circuits on the Sum Loop Mixer Board. The mixer takes the Sum Loop VCO and N Loop VCO signals, mixes them down to a frequency band of 1 MHz to 2 MHz, and sends this band to the frequency detector. The frequency detector is composed of U2 through U6. This circuit detects when the sum loop frequency is greater than the N loop frequency and sends a Sum loop frequency error signal to the Sum Loop VCO Assembly (Service Sheet 51).

Mixer Circuitry

The sum loop mixer RF from the Sum Loop VCO (service sheet 51) and the sum loop mixer LO from the N Loop VCO (service sheet 48) enter the board via the J2 and J1 inputs, respectively. The S loop RF passes through a 10 dB pad and a limiter formed by U1. U1 has a gain of 10 dB and limits at +1 dBm. The output of this limiter stage is then capacitively coupled to the RF input of mixer U7.

The S loop LO signal from the N Loop VCO (service sheet 48) is limited by CR1 and CR3 and attenuated by the 3 dB pad formed by R7, R9, and R11. The signal is then applied to the LO input of the mixer. The output IF from the mixer varies between 1 MHz and 2 MHz. The output of the mixer is filtered by a 10 MHz low-pass filter formed by C14, L3, C15, L4, and C16, and then enters the limiter/buffer amplifier formed by transistors Q1 and Q2. The resulting signal is the sum loop IF signal. The level of this signal is approximately 4 Vp-p.

Frequency Detecting Circuitry

The frequency detecting circuit determines if the S loop frequency exceeds the N loop frequency. The S loop normally extends from 120 MHz to 220 MHz; the N loop's frequency range is from 122 MHz to 221 MHz. The S loop frequency should always be 1 MHz to 2 MHz below the N loop frequency. If it becomes more than 2 MHz above the N loop, the S loop will reverse and send the VCO in the wrong direction.

The frequency detecting circuit keeps the S Loop VCO frequency below that of the N loop. The decade divider circuits (U2 and U3) divide the outputs of the two VCOs by 10. The divided signals at TP1 and TP2 enter frequency detector U4, which determines when the S loop frequency is greater than the N loop frequency. When the S loop frequency is greater, the output at pin 12 of U4 goes HI, causing a ramp voltage to be applied to pin 2 of comparator U5.

SERVICE SHEET 49 (Cont'd)

The ramp voltage at pin 2 of U5 is compared against the reference voltage at pin 3, and a TTL pulse is generated at the pin 7 output. This TTL pulse triggers monostable one-shot U6, producing a 3.4 μs pulse which is sent to the S Loop VCO as a frequency error signal. A pulse train is output from U6 as long as the S loop frequency is greater than the N loop frequency. This pulse train is filtered, summed with the S loop error and pretune currents, and converted to a voltage so that it can be used to help decrease the S Loop VCO frequency.

The frequency detector is disabled by the frequency detector enable line (at board pin 11) when the S Loop VCO is locked. The frequency detector enable line is also sent to pin 14 of U2 and U3, turning OFF the dividers to prevent spurs from being generated.

N Loop VCO A3A4 SERVICE SHEET 48

A3A5 ASSEMBLY

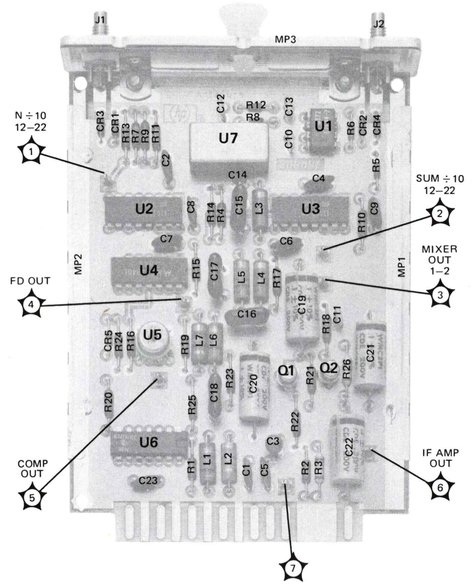
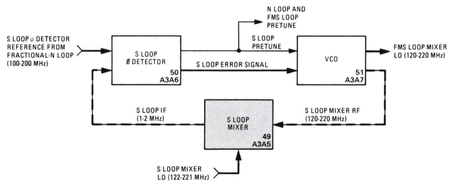


Figure 8-630. A3A5 Sum Loop Mixer Component Locations



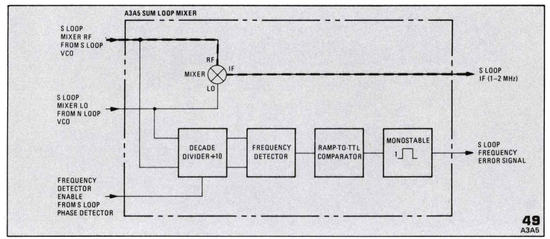
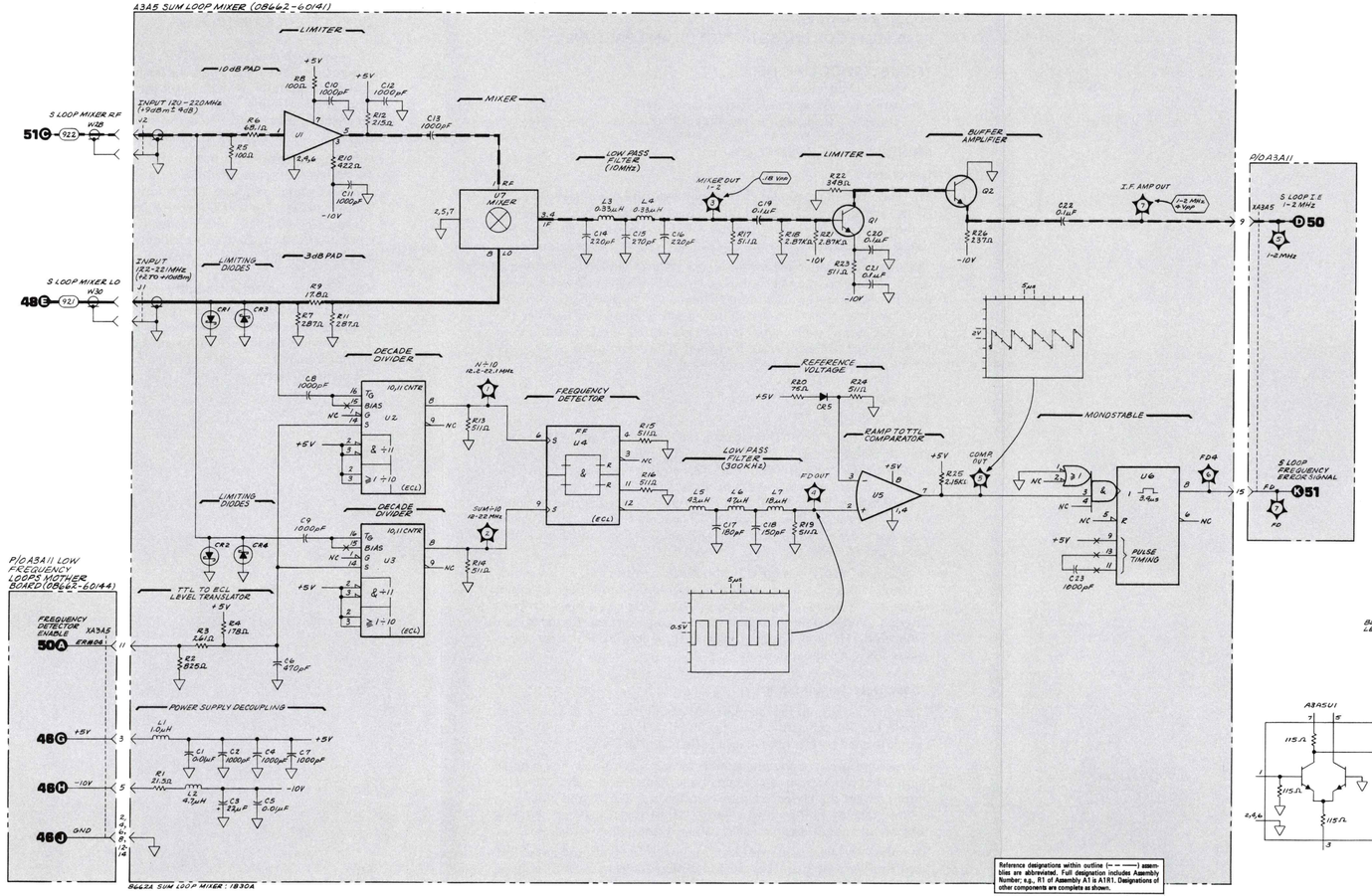


Figure 8-631. A3A5 Sum Loop Mixer Block Diagrams



NOTES

1. LOGIC LEVELS FOR ECL DEVICES IN THIS INSTRUMENT ARE NON-STANDARD DUE TO THE SUPPLY VOLTAGE USED. A HIGH LEVEL IS ≥ 4.0V, A LOW LEVEL IS ≤ +3.5V.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MIGHT BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.

REFERENCE DESIGNATIONS

NO PREFIX	A11
W28, 30	TP5,7 XA3A5
A5	
C1-23 CR1-2 J1,2 L1-17 Q1,2 R1-26 TP1-7 U1-7	

LOGIC LEVELS

LOGIC	TTL	ECL	EECL	CMOS
HIGH(1)	≥ 2V	≥ +4.0V	≥ +4.9V	≈ VDD
LOW(0)	≤ 0.8V	≤ +3.5V	≤ +4.6V	≤ 0.1V

1 = EQUAL TO OR MORE NEGATIVE THAN
2 = EQUAL TO OR MORE POSITIVE THAN

INPUT	TTL	ECL	EECL	CMOS
GROUND	LOW(0)	HIGH(1)	HIGH(1)	LOW(0)
OPEN	HIGH(1)	LOW(0); LOW(0)		X

GROUND = 0V; X = UNDEFINED

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1, 2	1854-0404
U1	1826-0372
U2, 3	1820-1780
U4	1820-1364
U5	1826-0034
U6	1820-0704

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U2,3	+5V - 4,5 ▽ -10/13
U4	+5V - 1,14 ▽ - 7
U6	+5V - 14 ▽ - 7

BLUE LEAD

MIXER BOTTOM VIEW

A3A5U1

49
A3A5

Figure 8-632. A3A5 Sum Loop Mixer Schematic

SERVICE SHEET 50
A3A6 SUM LOOP PHASE DETECTOR AND PRETUNE

TROUBLESHOOTING HELP

Block Diagram H
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

There are two independent circuits on the Sum Loop Phase Detector Board. One is a pretune circuit that coarsely tunes the three oscillators in the low frequency loops to within 3 MHz of the correct frequency so that the search and lock time for the loop is decreased.

The upper portion of the service sheet shows the phase detector circuitry. This section has two inputs. One is the S loop IF signal input and the other is the fractional-N loop VCO output (S Loop phase detector reference). The S loop IF signal is compared against the reference signal, and error pulses are generated at the output to keep these two signals at the same frequency. The error pulses generate an error voltage which is sent to the S Loop VCO (service sheet 51).

Pretune Circuitry

The pretune circuit consists of transistors Q1 through Q14. Q1 through Q8 are controlled by BCD lines from the Frequency Output Board via pins 10-13 and 25-28. The BCD weighted currents at the collectors of transistors Q1 through Q8 in the D/A converter are summed at TP4. These weighted currents are subtracted from the current that would normally flow through Q10 from R44 and R45. The net current out of Q10 appears as a voltage across R47. As more transistors are turned ON, less current flows through Q10 and the voltage across R47 approaches 0 volts.

Q9 sets a reference voltage that clamps the emitter of Q10 to 10 volts. Q11 and Q14 form a dual emitter-follower buffer amplifier. Its output range is 1.2 volts to 7.0 volts. After passing through a 1 MHz low-pass filter, this voltage is sent to the VCO summing junctions for the N loop, S loop and FMS loop. This pretunes the three oscillators to frequencies where the loops should lock.

Phase Detector Circuitry

The reference signal for the phase detector circuitry comes from the Fractional-N Loop at 100 MHz to 200 MHz. It is divided by 100 by a circuit formed by U1 and U2 and is then sent to U4A.

The second input to the phase detector circuitry is the sum loop IF signal that comes from the S Loop Mixer Board (service sheet 49). This signal enters the board via pin 9 and goes to pins 1 and 2 of U3, a schmitt trigger. The input waveform is converted to a square wave by this circuit so that it can be used by the digital phase detector.

The phase detector is formed by flip-flops U4A, U4B and gate U3B. One flip-flop is latched HI by the S loop phase detector reference signal and one is latched HI by the S loop IF signal. Once both flip-flops are set, the output of U3B goes HI, resetting them. As a result, the output of the flip-flops is a signal with a pulse width equal to the time difference

SERVICE SHEET 50 (Cont'd)

between the signals driving U4A and U4B. The pulse width is wide when there is a large phase or frequency difference and is narrow when both signals are in phase. A ramp shaped signal appears at TP3 and TP6 (only one; never both) depending on the direction of the frequency phase shift.

The ramp waveform at either TP3 or TP6 is sent to the differential amplifier integrator formed by Q13, Q15, and Q12. The feedback loop for this circuit is composed of C31 and R57. The output of the integrator passes through R65 and R66 before leaving the board as the error voltage to the S Loop VCO (service sheet 51). When locked, this output (at pin 30) is 0 ± 0.5 volts. Diodes CR2 through CR7 limit the total voltage at C31 (in the feedback loop) so that the charge time of C31 is not increased if a transient occurs during locking.

Out-of-Lock Detector Circuitry

The out-of-lock detector formed by U3C and U5C produces a pulse that triggers the monostable one-shot formed by U6 when the pulses from U4 are wide. U6 in turn lights the out-of-lock LED. A signal is also output from pin 25 and is sent to the Sum Loop IF Board, enabling the frequency detector circuitry.

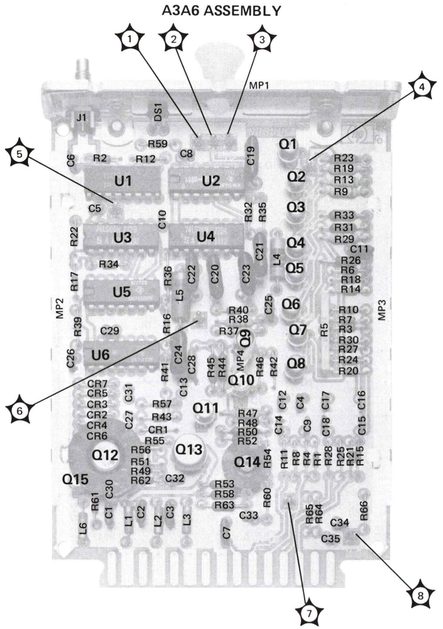
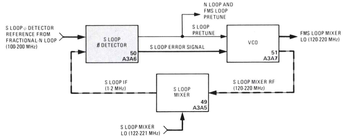


Figure 8-633. A3A6 Sum Loop Phase Detector and Pretune Component Locations



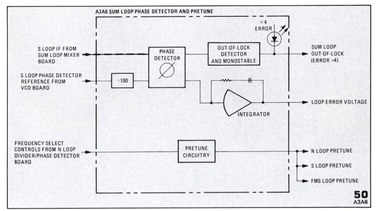
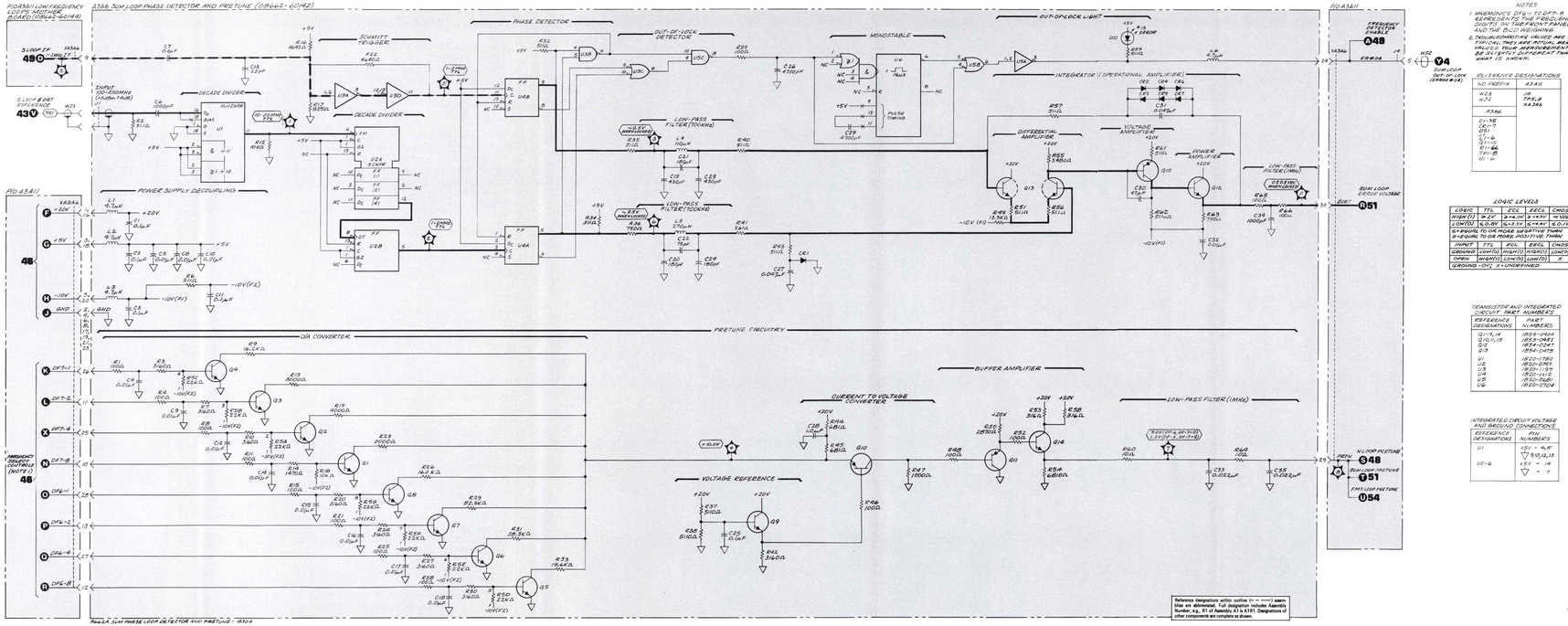


Figure 8-634. A3A6 Sum Loop Phase Detector and Pretune Block Diagrams



NOTES

1. MNEMONICS DF&1 TO DF7-8 REPRESENTS THE FREQUENCY DIGITS ON THE FRONT PANEL AND THE BCD ASSIGNING.
2. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENT MIGHT BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.

REFERENCE DESIGNATIONS

NO PREFIX	A3A6
W28 thru W32	J4 thru J8
A3A6	
C1-16	
C18-19	
C21	
C23-26	
C28-29	
C31	
C33-34	
C36-46	
C48-49	
CR1-2	
CR4	
L1-8	
Q1-16	
R1-66	
R68-69	
TP1-8	
U1-6	

LOGIC LEVELS

LOGIC	TTL	FCL	ECL	CMOS
HIGH (1)	≥ 2V	≥ +4.5V	≥ +4.7V	≈ VDD
LOW (0)	≤ 0.8V	≤ +3.5V	≤ +4.4V	≤ 0.1V

0 = EQUAL TO OR MORE NEGATIVE THAN
1 = EQUAL TO OR MORE POSITIVE THAN

INPUT	TTL	FCL	ECL	CMOS
GROUND	LOW (0)	HIGH (1)	HIGH (1)	LOW (0)
OPEN	HIGH (1)	LOW (0)	LOW (0)	1

GROUND = 0V; X = UNDEFINED

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1-9, 14	1854-0404
Q10-11, 15	1853-0481
Q12	1854-0241
Q13	1854-0478
U1	1820-1780
U2	1820-0767
U3	1820-1199
U4	1820-1112
U5	1820-1481
U6	1820-0704

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U1	+5V = 14; ▽ = 8
U2-6	+5V = 14; ▽ = 7

Figure 8-635. A3A6 Sum Loop Phase Detector and Pretune Schematic

SERVICE SHEET 51
A3A7 SUM LOOP VCO ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram H
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

This board contains the voltage controlled oscillator and associated circuitry for the FM Sum Loop. There are three frequency control inputs to this board and two outputs. One output is the FM sum loop mixer RF; the other goes to the high frequency loops section. The frequency control inputs are summed, shaped, amplified and filtered before being used to control the frequency of the voltage controlled oscillator.

Current Summing Junction

The inputs are combined at the summing junction before entering amplifier Q10. Q10 amplifies the summed currents from the three frequency control inputs and converts them to a control voltage.

One of the three inputs is the sum loop frequency error signal (pin 11) which comes from the Sum Loop Mixer Board (service sheet 49). The other two are the pretune signal (pin 10) and the sum loop error signal (pin 9). Both come from the Sum Loop Phase Detector Board (service sheet 50). The pretune line has a gain adjustment which allows the range of the VCO to be set. The maximum tune range is approximately 100 MHz (+1.2 to +7.0 Vdc pretune voltage range).

Shaping Network and Buffer Amplifier

The shaping network in the collector of Q10 is a diode-resistor network composed of CR5, CR6, R13, R15, R17, and R20. This network shapes the pretune voltage so that a change in voltage produces a linear change in output frequency. Normally, varactors CR13 and CR14 in the VCO give it a non-linear output. The diode network, however, cancels out the non-linearity by switching in the diodes at the appropriate points.

Following the shaping network is an emitter-follower stage formed by Q7. This stage drives the filter network that removes the spurious signals from the loop and drives the phase lag network consisting of R32 and C20. The varactor voltage (at TP3) goes through R34 to the oscillator tank at CR13 and CR14. This is a negative voltage of −2 volts to −18 volts (−2 volts is the limit for the low frequency end and −18 volts is the limit for the high frequency end).

Gain Set Switch

Q6 is a transistor switch which increases the loop gain voltage as determined by the threshold point of CR6. Q6 turns on and shunts R26 so that the gain of Q7 at TP3 is increased by approximately 6 dB. This causes the loop gain to increase and compensate for the decrease in gain of the varactors, which occurs close to the high frequency end.

SERVICE SHEET 51 (Cont'd)

Charge-Discharge Switch

Transistors Q5 and Q9 switch current into C20 through R24. These transistors are biased so that when the voltage at TP4 is two volts greater than the voltage at C20, either Q5 or Q9 turn on to quickly charge C20. This increases switching speed.

Voltage Controlled (Hartley) Oscillator

The oscillator itself is formed by Q8, which is a common gate FET amplifier. Capacitor C23 is a bypass capacitor for the varactors. L8 is a tapped inductor. The feedback loop feeds through C25 to the source of the FET. R28 and R30 set the dc current in the FET. R31 and R33 set the dc voltage at the gate.

Signal Splitter

The output of the VCO is tapped from L8 very close to ground and goes through R36 to transformer T1, which is a power splitter. This splitter supplies half power to each of the two amplifiers and provides substantial isolation between them.

Output and Loop Buffer Amplifiers

The loop buffer amplifier consists of Q1 and Q3. The output buffer amplifier consists of Q2 and Q4. The two transistors within each amplifier assembly are cascaded. The output of each amplifier is attenuated by a 3 dB pad before being output from the assembly. One of the outputs is sent to the FM sum loop mixer (LO input), the other to the sum loop mixer (RF input).

Minus 26 Volt Supply

The −26 volt on-board supply is powered by the main −40 volt supply. It is used as a reference voltage for the frequency breakpoints by the shaping network consisting of CR5 and CR6.

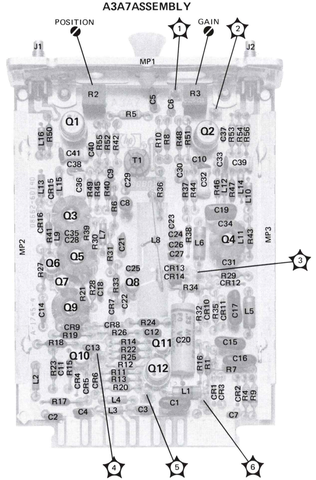
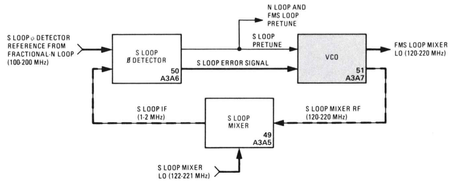


Figure 8-636. A3A7 Sum Loop VCO Component Locations



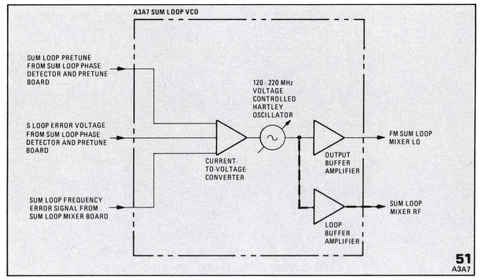
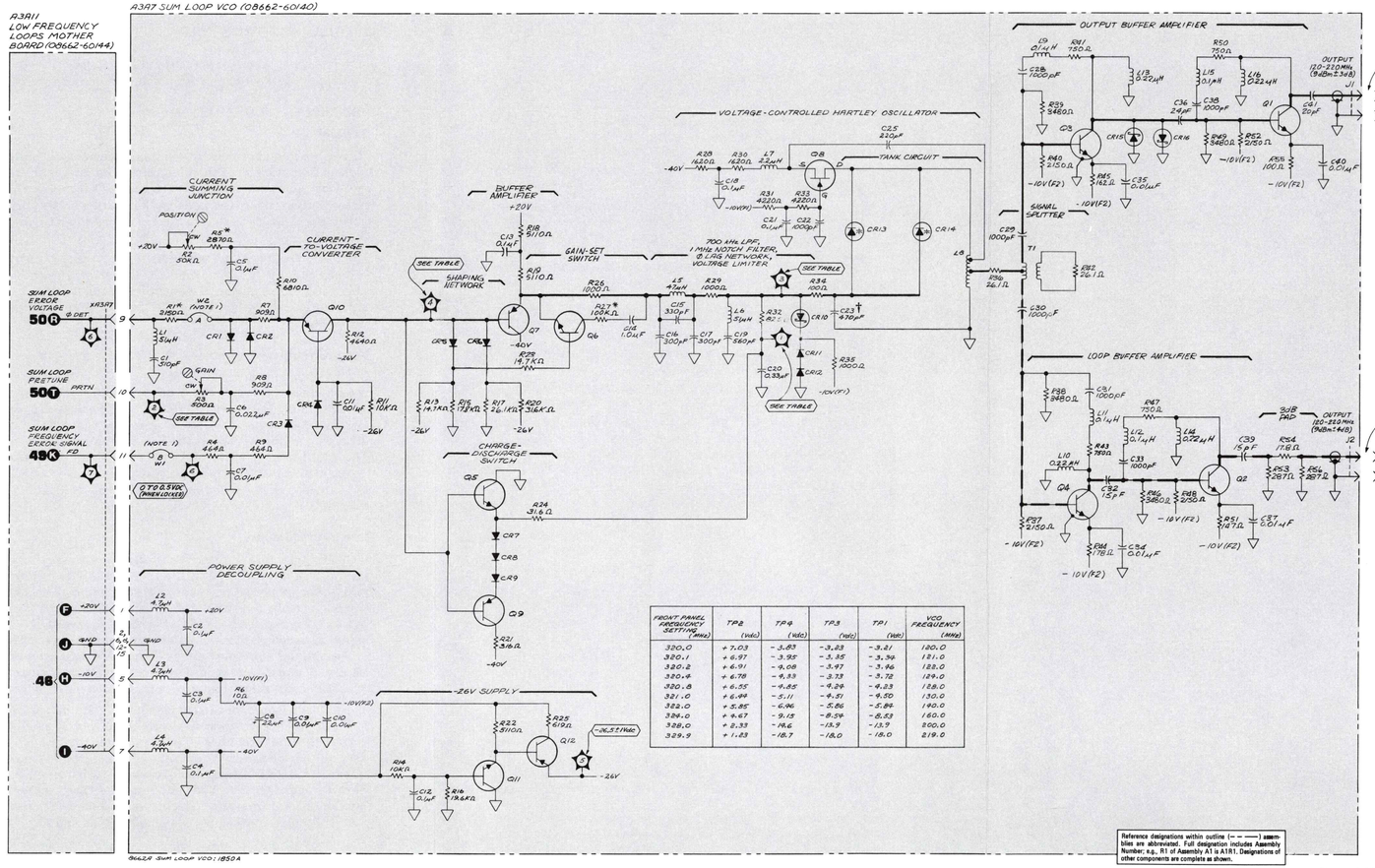


Figure 8-637. A3A7 Sum Loop VCO Block Diagrams



FRONT PANEL FREQUENCY SETTING (MHz)	TP2 (Vdc)	TP4 (Vdc)	TP3 (Vdc)	TP1 (Vdc)	VCO FREQUENCY (MHz)
320.0	+7.03	-3.93	-3.23	-3.21	120.0
320.1	+6.97	-3.92	-3.25	-3.24	121.0
320.2	+6.91	-4.08	-3.97	-3.96	122.0
320.4	+6.78	-4.33	-3.73	-3.72	124.0
320.8	+6.55	-4.85	-4.29	-4.23	128.0
321.0	+6.44	-5.11	-4.51	-4.50	130.0
322.0	+5.85	-6.46	-5.86	-5.84	140.0
324.0	+4.67	-9.13	-8.54	-8.53	160.0
328.0	+2.33	-14.6	-13.9	-13.9	200.0
329.9	+1.23	-16.7	-16.0	-16.0	219.0

NOTES
1. JUMPERS W1 AND W2 ARE REMOVED FOR TROUBLESHOOTING ONLY.
2. ASTERISK (*) INDICATES THAT THESE PARTS ARE SELECTED IN TEST. THE VALUES SHOWN ARE TYPICAL ONLY. SEE SECTION V FOR PROCEDURE.
3. TROUBLESHOOTING VALUES ARE TYPICAL. THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MIGHT BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
† BREAKDOWN INFORMATION IN SECTION VII

REFERENCE DESIGNATIONS

NO PREFIX	A3A11
W27, 28	TP6, 7
A3A7	XA3A7
C1-23, 25, 28-41	
CR1-16	
U1, 2	
L1-16	
Q1-12	
R1-56	
T1	
TP1-6	
W1, 2	

NOT ASSIGNED: C24, C26, C27

TRANSISTOR PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1, 2	1854-0247
Q3, 4	1854-0346
Q5, 6, 11	1854-0404
Q7, 9, 10	1855-0481
Q8	1855-0235
Q12	1853-0012

Q8 BOTTOM VIEW

Figure 8-638. A3A7 Sum Loop VCO Schematic

SERVICE SHEET 52
A3A9 FM SUM LOOP MIXER ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram H
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

There are two separate circuits on this service sheet. The upper portion of the schematic shows the integrator. The integrator takes the FM sum loop phase and frequency error signals from the FM Sum Loop Phase Detector Board (service sheet 53) and generates an FM sum loop error current which is sent to the FM Sum Loop VCO Board (service sheet 54).

The lower portion of the schematic shows the mixer circuitry. This section takes the FM sum loop VCO signal (service sheet 54) and the sum loop VCO signal (service sheet 51) and mixes them to produce the FM sum loop IF which is sent to the FM sum loop phase detector (service sheet 53).

Mixer Circuitry

The FM sum loop mixer RF (FMS loop VCO output) enters the board via J1, passes through the 3 dB attenuator pads and a 250 MHz low-pass filter before entering pin 1 of mixer U1. The FM sum loop mixer LO (sum loop VCO output) enters the board via J3 and is passed through a 300 MHz low-pass filter before entering pin 8 of the mixer. The signal outputs from pins 3 and 4 of the mixer are passed through a 3 dB pad and a 40 MHz low-pass filter before leaving the board as the FM sum loop IF at J2. The output level of this 20 MHz IF signal is −16 dBm ± 3 dB.

Integrator Circuitry

Q1A and Q1B form a discrete differential amplifier within the integrator circuitry. One input to the amplifier is a frequency error signal (pin 8); the other is a phase error signal (pin 6). The signal at pin 8 should normally be at 0 volts when locked. At 0 volts, CR1 and CR2 are biased OFF and the base of Q1B is close to 0 volts. The phase error signal at pin 6 operates the differential amplifier to control the phase of the signal. The output voltage of the differential amplifier is amplified by Q7 and Q4 and is used to drive the voltage to current converter (Q3). The constant current source for the converter is formed by Q6.

The FM sum loop error current which flows through pin 3 of the board is the difference between the current flowing through Q6 and the current flowing through Q3. The current flowing through Q3 is dependent on the voltage at the output of the integrator. The output of the integrator is controlled by feedback. When Q5 turns OFF, less current flows through Q3 for a given voltage at TP3. Q5 is turned ON and OFF by digital lines from the Microprocessor Board which enter the FM Sum Loop Mixer/Assembly via pins 9, 10, 19, and 20.

A3A9 ASSEMBLY

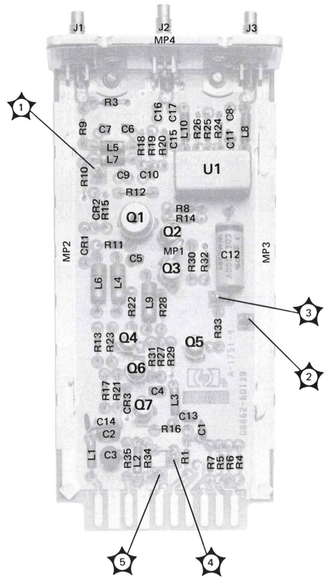
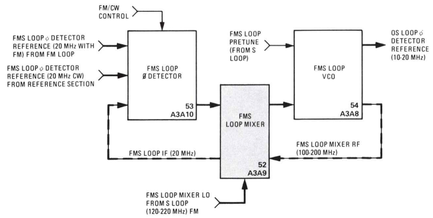


Figure 8-639. A3A9 FM Sum Loop Mixer Component Locations



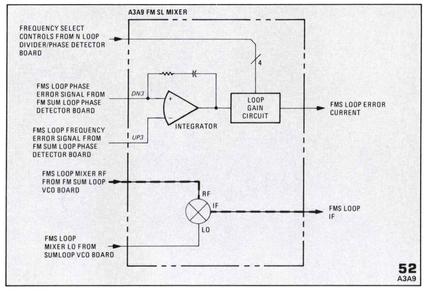


Figure 8-640. A3A9 FM Sum Loop Mixer Block Diagrams

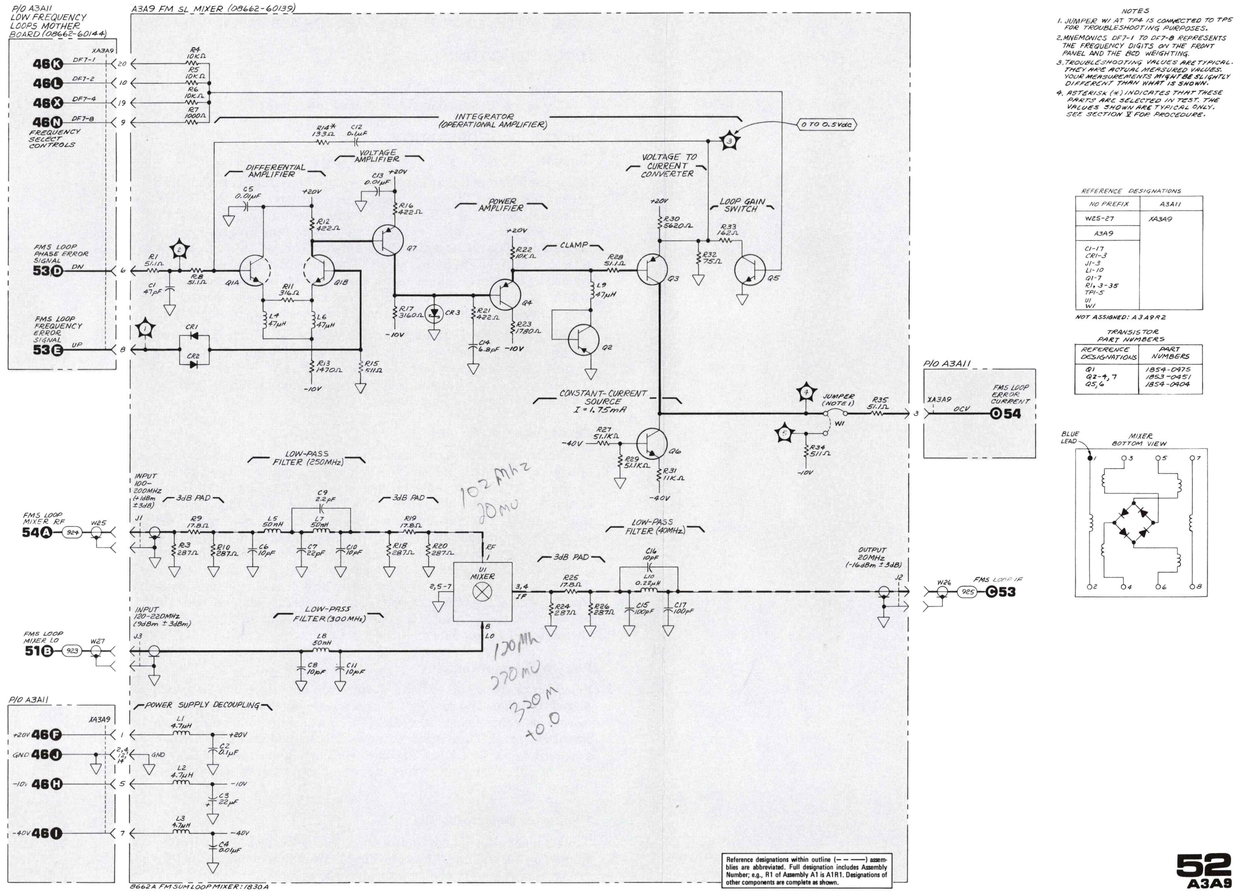


Figure 8-641. A3A9 FM Sum Loop Mixer Schematic

SERVICE SHEET 53
A3A10 FM SUM LOOP PHASE DETECTOR ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram H
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

It is on the FM Sum Loop Phase Detector Board that either the 20 MHz continuous wave (CW) signal from the reference section or the 20 MHz FM signal (generated within the modulation section) is summed with the 120 MHz to 220 MHz (1 Hz step resolution) Low Frequency Sum Loop signal. The net result is a 100 MHz to 200 MHz CW or FM signal at the output of the FM Sum Loop VCO (service sheet 54). This signal is divided by the decade divider on the same board to produce the 10 MHz to 20 MHz (0.1 Hz step resolution) reference signal that is used by the Output Sum Loop Phase Detector in the high frequency loops section.

Inputs to the Phase Detector Board include the FM sum loop CW and FM phase detector reference signals (pins 10 and 8), the FM sum loop IF from the Sum Loop Mixer at J1 and the FM/CW control at pin 15. Outputs include the FM sum loop phase error signal (pin 14) and the FM sum loop frequency error signal (pin 12).

Phase Detector Circuitry

The FM sum loop IF signal passes through a 20 MHz low-pass filter and through 60 MHz and 100 MHz notch filters before being amplified by the 20 MHz bandpass amplifier formed by Q1. The notch filters eliminate spurious signals from the FM Sum Loop Mixer Board. Following the bandpass amplifier, the signal passes through a 3 dB pad before splitting in two directions. One path is through Q2, which toggles one flip-flop of the frequency detector formed by U1. The other path is to the RF input of phase detector U2 (the LO input will be discussed subsequently). The output of the phase detector passes through R30 and a 20 MHz low-pass filter before leaving the board to be sent as an error signal to the integrator on the FM Sum Loop Mixer Board (service sheet 52).

FM/CW Selector Circuitry

Selection of either the FM or CW sum loop phase detector reference signals is handled by the FM/CW selector circuitry formed by U4. This selector is controlled by the FM/CW control line which enters the board via pin 15. The outputs of the selector are at pins 6 and 3. These two outputs are wire ORed and the resulting signal is sent to the LO input of phase detector U2 and the second toggle input (pin 6) of frequency detector U1.

Frequency Detector Circuitry

The frequency detector outputs a pulse whenever the FM sum loop IF frequency differs from either the FM or CW sum loop phase detector reference signals (whichever happens to be selected). The output from the frequency detector is sent to comparators U3A and U3B. The square wave outputs of the comparators are sent to an inverter circuit

SERVICE SHEET 53 (Cont'd)

that sums the currents to produce a voltage at the junction of R39 and R42. This voltage outputs as the FM sum loop frequency error signal at pin 12. When the system is in lock, the output at this point is about ± 0.5 volts. Q5 is used as an OR gate for the outputs of the two comparators. Whenever either of the comparators goes HI, Q5 turns on and lights the out-of-lock LED indicator.

A3A10 ASSEMBLY

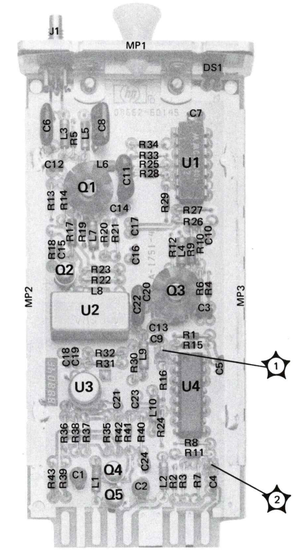
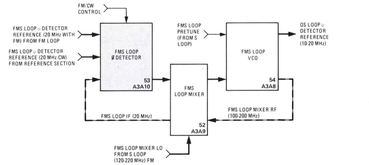


Figure 8-642. A3A10 FM Sum Loop Phase Detector Component Locations



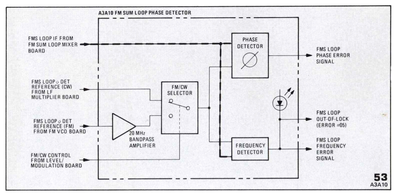
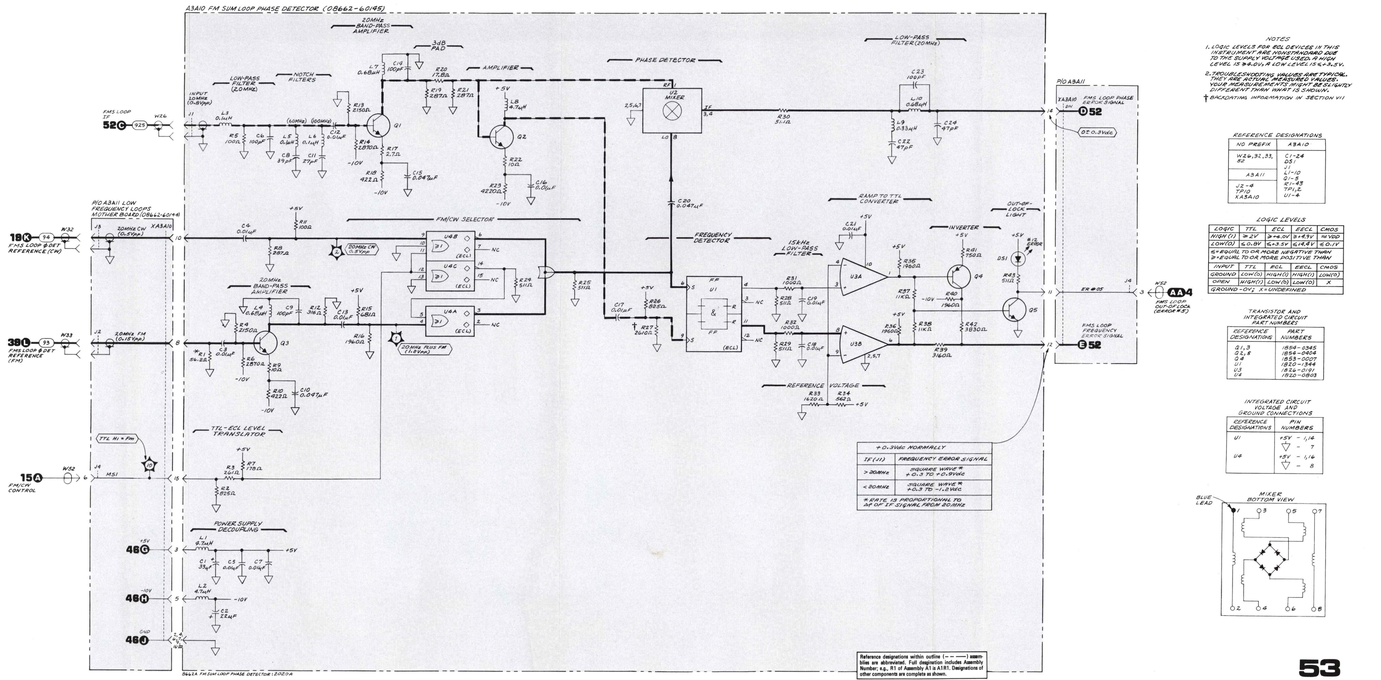


Figure 8-643. A3A10 FM Sum Loop Phase Detector Block Diagrams



NOTES

1. LOGIC LEVELS FOR ECL DEVICES IN THIS INSTRUMENT ARE NONSTANDARD DUE TO THE SLIGHLY HIGHER LOGIC 0 HIGH LEVEL IS ≥ -0.6V, A LOW LEVEL IS ≤ -1.5V.
2. TROUBLESHOOTING VOLTAGE ARE TYPICAL, THEY ARE ACTUAL MEASURED VALUES. THEY MAY VARY ± 10% UNLESS OTHERWISE SPECIFIED. SOME MAY VARY ± 50%.

† INDICATING INFORMATION IN SECTION VII

REFERENCE DESIGNATORS

NO PREFIX	A3A10
W26, 31, 33, 52	C1-C4 DS1 J1 L1-L10 Q1-Q5 R1-R3 TP1,2 U1-U8
A3A11	
C2-8 TP12 K3A10	

LOGIC LEVELS

LOGIC	TTL	ECL	ECL	CMOS
HIGH (1)	≥ 2V	≥ -0.6V	≥ -0.9V	≥ VDD
LOW (0)	≤ 0.8V	≤ -1.5V	≤ -1.6V	≤ 0.1V

K = EQUALS TO OR MORE NEGATIVE THAN
> = EQUAL TO OR MORE POSITIVE THAN

INPUT	TTL	ECL	ECL	CMOS
GROUND	LOW (0)	HIGH (1)	HIGH (1)	LOW (0)
OPEN	HIGH (1)	LOW (0)	LOW (0)	X

GROUND = 0V, X = UNDEFINED

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1, 3 Q2, 4 Q5 U1 U2 U3, 4 U5 U6 U7 U8	1854-0345 1854-0404 1853-0007 1820-1197 1820-0181 1820-0803

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U1	+5V = 14 - = 7
U4	+5V = 16 - = 8

MIXER BOTTOM VIEW

Figure 8-644. A3A10 FM Sum Loop Phase Detector Schematic

SERVICE SHEET 54
A3A8 FM SUM LOOP VCO ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram H
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The FM Sum Loop VCO utilizes back-to-back varactors instead of bypass capacitors used on the other two VCO assemblies. This allows greater bandwidth and higher frequency modulation of the oscillator.

There are two inputs to the Sum Loop VCO Board. One is a pretune from the Sum Loop Phase Detector Board which enters the FM Sum Loop Board via pin 10. This input is fed through a linearizer circuit and is then buffered by Q3 and Q4. The resulting voltage at TP3 is used to pretune the voltage controlled oscillator within lock range. The FM sum loop error current enters the board via pin 9 and passes through a 40 MHz low-pass filter, formed by L7 and C8, before being summed with the loop pretune signal. This signal provides fine tuning to the VCO and guides it to final lock.

Signal splitter T1 (in the output section of this board) divides the power of the signal tapped at L12 and distributes it to limiters U2 and U1. Limiter U2 has two outputs. One of them is a test output with a frequency range of 100 MHz to 200 MHz. The other output is passed through a divide-by-ten circuit to provide the 10 MHz to 20 MHz phase detector reference (0.1 Hz step resolution) signal needed by the Output Sum Loop in the high frequency loops section. The output of limiter U1 passes through a 300 MHz low-pass filter and outputs from the board to the FM Sum Loop Mixer (service sheet 52), providing feedback for the FM Sum Loop.

A3A8 ASSEMBLY

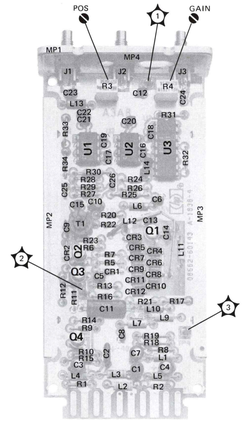
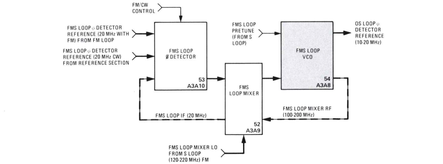


Figure 8-645. A3A8 FM Sum Loop VCO Component Locations



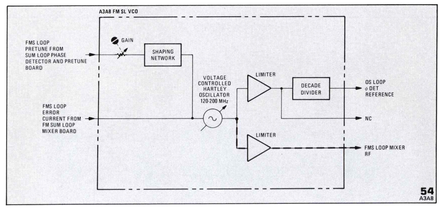
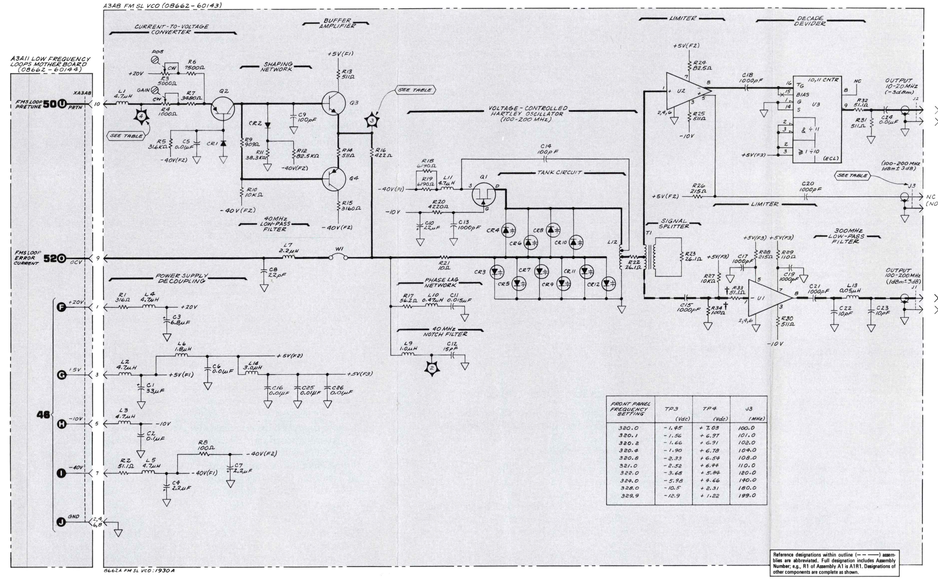


Figure 8-646. A3A8 FM Sum Loop VCO Block Diagrams



NOTES
1. RF CONNECTOR J3 IS USED IN TROUBLE-SHOOTING ONLY.
2. TROUBLESHOOTING VALUES ARE TYPICAL THEY ARE ACTUAL MEASURED VALUES. YOUR MEASUREMENTS MIGHT BE SLIGHTLY DIFFERENT THAN WHAT IS SHOWN.
↑ INDICATING INFORMATION IN BOTTOM VIEW

REFERENCE DESIGNATIONS	
NO PREFIX	A11
W10,25	X3A3A8
A10	
C1-36, C41-76, C81-96, L1-5, 9-14, 61-64, 81-86, 101-106, TP2-4, U1-3, W1	

LOGIC LEVELS

LOGIC	TTL	ECL	PECL	CMOS
HIGH(1)	≥ 2V	≥ -1.0V	≥ +4.2V	≥ 70%
LOW(0)	≤ 0.8V	≤ -1.5V	≤ +3.9V	≤ 0.1V

X = EQUAL TO OR MORE NEGATIVE THAN
P = EQUAL TO OR MORE POSITIVE THAN

OUTPUT	TTL	ECL	PECL	CMOS
GROUND (LOW(0))	HIGH(1)	HIGH(1)	LOW(0)	
OPEN	HIGH(1)	LOW(0)	LOW(0)	X
GROUND -10V	X	UNREGARDED		

TRANSISTOR AND INTEGRATED CIRCUIT PART NUMBERS

REFERENCE DESIGNATIONS	PART NUMBERS
Q1	1855-0236
Q2,4	1853-0481
Q3	1854-0404
U1,2	1826-0372
U3	1827-1340

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

REFERENCE DESIGNATIONS	PIN NUMBERS
U3	+5 (VP) 4,5 -12 7

Q1 BOTTOM VIEW

54 A3A8

Figure 8-647. A3A8 FM Sum Loop VCO Schematic

SERVICE SHEET 55
A7A3 AND A7A4 POWER SUPPLY MOTHERBOARD AND INVERTER ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram I
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

Circuitry on the Power Supply Motherboard and Inverter Board rectify and invert the ac line voltage prior to regulation. Before reaching these boards, the line voltage is passed through a filter assembly (A10) and a voltage selection switch (S2), which allows operation at 115Vac or 220Vac. Power entering the supply motherboard via pins 7-9 is rectified and coarsely filtered to produce ± 160 Vdc. In the case of 115Vac operation, voltage doubling is implemented during rectification. The ± 160 Vdc is then chopped by inverter/regulator switches Q3 and Q4 to drive the main power supply transformer (A7A3T3).

The ac voltages at the multiple secondary taps of the transformer are rectified, filtered, and sent to the Linear Regulator Board (service sheet 62). The +5.2 Vdc line is regulated exclusively by the switching action of the supply. Fast and slow sense lines, as well as foldback and feedback sense lines, are derived from various points along the +5.2 Vdc line. These sense lines are sent to the Control Board (service sheet 63) which uses the information they provide to generate two pulse-width modulated signals (180° out of phase) that are fed back to drive the inverter/regulator circuitry (formed by Q1, Q2, Q3, and Q4) on the Inverter Assembly.

The output voltage of the 30Vac transformer (T1) is rectified, filtered, and regulated to supply the dc oven heater voltage for the 10 MHz reference crystal oscillator and to power sections of the Linear Regulator and Control Boards. Circuitry within the auxiliary regulator section on the Control Board (service sheet 57) prevents the instrument from being operated when the line voltage falls below 80Vac (for 115Vac operation), or 160Vac (for 220Vac operation).

Rectifier, Filter, and Voltage Doubler Circuitry (A7A4)

With the input voltage selection switch in the 220Vac position, input voltage is full-wave rectified by the bridge formed by CR1, CR2, CR3 and CR4 and is coarsely filtered by capacitors C2 and C3 to produce ±160 Vdc. When the selection switch is in the 115Vac position, CR2 and CR3 form a bridge rectifier and voltage doubler. Here again, the result is ± 160 Vdc. CR5 and CR6 serve to protect capacitors C2 and C3 from reverse voltage generated during foldback current limiting.

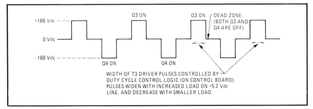
Overvoltage Crowbar

The overvoltage protection circuitry (crowbar) disables the instrument in the event that the rectified dc voltage exceeds ± 185 Vdc. At this point Q1 fires and switches 5Ω across the input line, blowing line fuse F1.

SERVICE SHEET 55 (Cont'd)

Switch Drivers and Inverter/Regulator Switches (A7A3)

In order to drive T3, pulses from the pulse-width modulation circuitry (duty-cycle control logic) on the Control Board are transformer coupled (via A7A3T1 and A7A3T2) to the inverter/regulator switch driver circuitry formed by Q1 and Q2. QS1 and Q2 are turned alternately ON and OFF to drive Q3 and Q4 180° out of phase. This action switches the ± 160 Vdc to produce a 20 kHz alternating drive current through the primary of T3 (see figure below). Q3 and Q4 are turned on by about 350mA of current at their bases. To reduce the turn-off time of the two transistors, however, two amperes of reverse current is required to turn them off.



Switching Waveform at the Primary of T3 (also see Power Supply Overview)

A resistive-capacitive divider formed by R1, R2, C1, and C2 indirectly references the primary of T3 to ground, isolating the high voltage section from chassis ground and preventing T3 from overheating due to dc currents caused by imbalances in the switching circuits that drive T3. The circuit formed by R11, R12, and C5 serves to lower the Q of the inductance associated with T3, cutting down on ringing at the emitter of Q3 and the collector of Q4.

Secondary Isolation/Stepdown Transformer (T3) Outputs

Voltages at the secondary taps of T3 are referenced to the +5.2 Vdc supply ground. They are full-wave rectified, coarsely filtered, preregulated, and sent to the Linear Regulator Assembly for final regulation. These unregulated voltages are +23 volts, −13 volts, and −45 volts.

The fast and slow sense lines, as well as the foldback and feedback sense lines, are derived from the +5.2 Vdc supply line. The duty cycle control logic on the Control Board regulates the +5.2 Vdc supply by varying the duty cycle of the signals which drive inverter/regulator switches Q3 and Q4. Regulation of the +5.2 Vdc supply is accomplished exclusively through the switching action of the supply; no linear regulators are used on this line.

TROUBLESHOOTING

When a power supply problem has been traced through the block diagram troubleshooting procedure to this assembly, use the following procedure to isolate the cause of the problem.

SERVICE SHEET 55 (Cont'd)

CAUTION

If the LINE fuse is blown, do not insert a new fuse until the cause of the failure has been determined. Inserting a new fuse could cause additional damage if the problem is a shorted diode or transistor on the Power Supply inverter assembly (A7A3). Perform steps 1 through 6 before inserting a new FUSE.

1. Disconnect the line cord from the rear panel of the Generator.
2. Remove the top cover of the instrument.
3. Remove the top cover of the power supply (left-rear cover of instrument).
4. Pull out the A7A3 inverter assembly.
5. Use an ohm meter or continuity checker to check the following components for shorts:

CR5	CR9	CR13
CR6	CR10	Q3
CR7	CR11	Q4
CR8	CR12	

6. If none of these components is shorted, it is safe to install another LINE fuse and continue normal troubleshooting.
7. Disconnect the line cord from the rear panel of the Generator.

WARNING

When the A7A3 Inverter assembly is mounted on its extender board, +160 V and −160 V are exposed on the traces on this board. Use extreme care.

CAUTION

Removing and installing power supply boards with the line cord plugged-in can damage these boards because high voltage is present whenever the line cord is plugged-in.

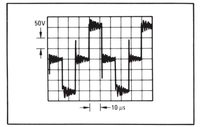
Remove the A7A3 Inverter assembly from the power supply. Insert the extender board for A7A3 (set the switch on the extender board to the "in" position to allow high voltage to appear on the top edge connector of the extender board). Plug-in the line cord. Measure the high voltage at the edge connector of the extender board. Use a DVM with the common lead connected to the chassis.

Pin 5 V = −160 ± 20 Vdc
Pin 7 V = +160 ± 20 Vdc

These values are for 115 VAC line voltage. Higher or lower line voltages produce proportionally more or less dc voltage. If this voltage is not correct, the problem is with the high voltage rectifiers and associated circuitry on A7A4. Troubleshoot this circuitry to find the cause. Otherwise, the problem is on the A7A3 assembly so continue troubleshooting with Step 8.

8. Look at the waveform at pin 3 of transformer T3. This is the output of the switching transistors. The waveform should be as shown in the following figure:

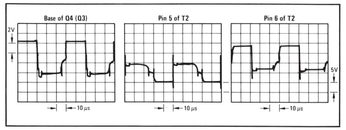
SERVICE SHEET 55 (Cont'd)



Waveform at Pin 3 of T3

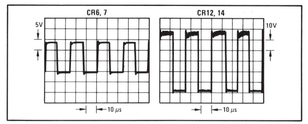
If this waveform is normal, the problem is on the secondary side of transformer T3 so continue troubleshooting with step 10 below. If this waveform is not correct, the problem is with the switching transistor circuitry so continue troubleshooting with step 9.

9. Disconnect the line cord from the rear panel of the Generator. Set the switch on the A7A3 extender board to the "out" position. With the switch in this position, no high voltage reaches the A7A3 assembly and the drive signals to the switching transistors can be observed. Compare the actual waveforms to those shown in the following figure:



Switching Transistor Drive Signals

10. Compare the waveforms at the outputs of the rectifiers on the secondary of transformer T3 to those shown in the following figure:



Transformer Secondary Waveforms

If any waveform is different, there is a problem with rectifier diodes or the transformer. The magnitude and duty cycle of the pulses will vary with line voltage, but the pulse width at the output of all rectifiers should be the same.

SERVICE SHEET 55 (Cont'd)

11. Measure the outputs of the rectifier filters at the bottom edge connector of A7A3. Normal values are:

Rectifier Filter Outputs

A7A3 Connector Pin	DVM DC Reading	DVM AC Reading
21	> +22.5	< 0.05
22	More negative than −12.50	< 0.20
20	More negative than −44.00	< 0.20
17	> +5.40	< 0.040
14, 15, 16	≥ +5.20	< 0.025

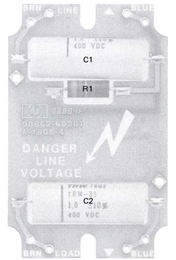
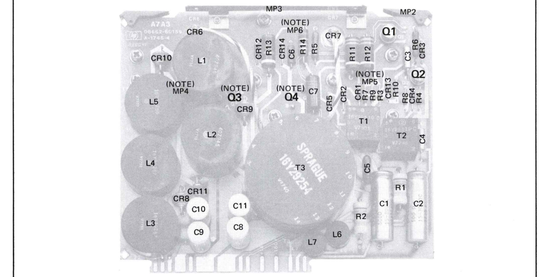


Figure 8-648. A10 Line Filter Component Locations



NOTE: MP4, MP5, MP6, Q3, & Q4 MOUNTED ON BACK OF BOARD

Figure 8-649. A7A3 Inverter Component Locations

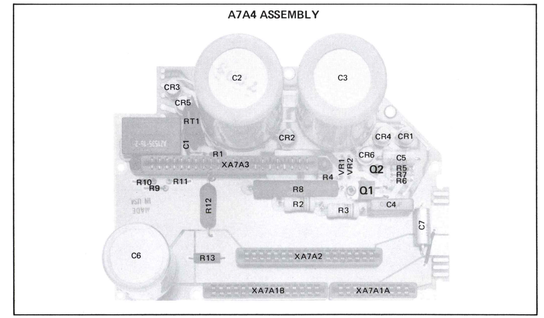


Figure 8-650. A7A4 Power Supply Mother Board Component Locations

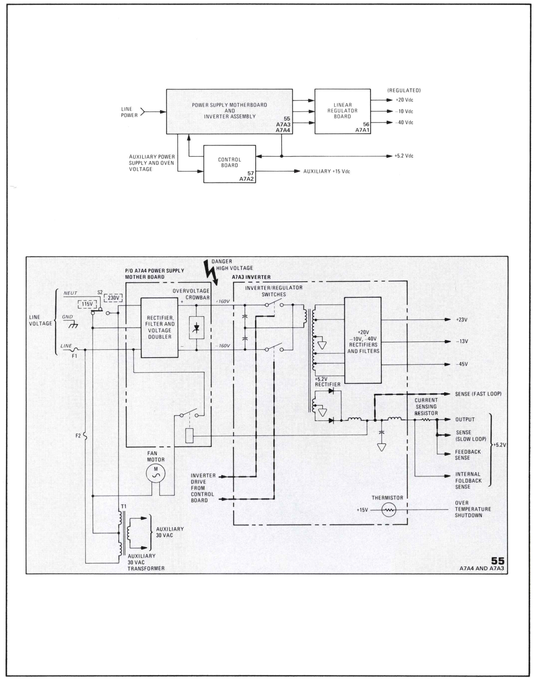


Figure 8-651. Power Supply Inverter, Mother Board, and Line Filter Block Diagrams

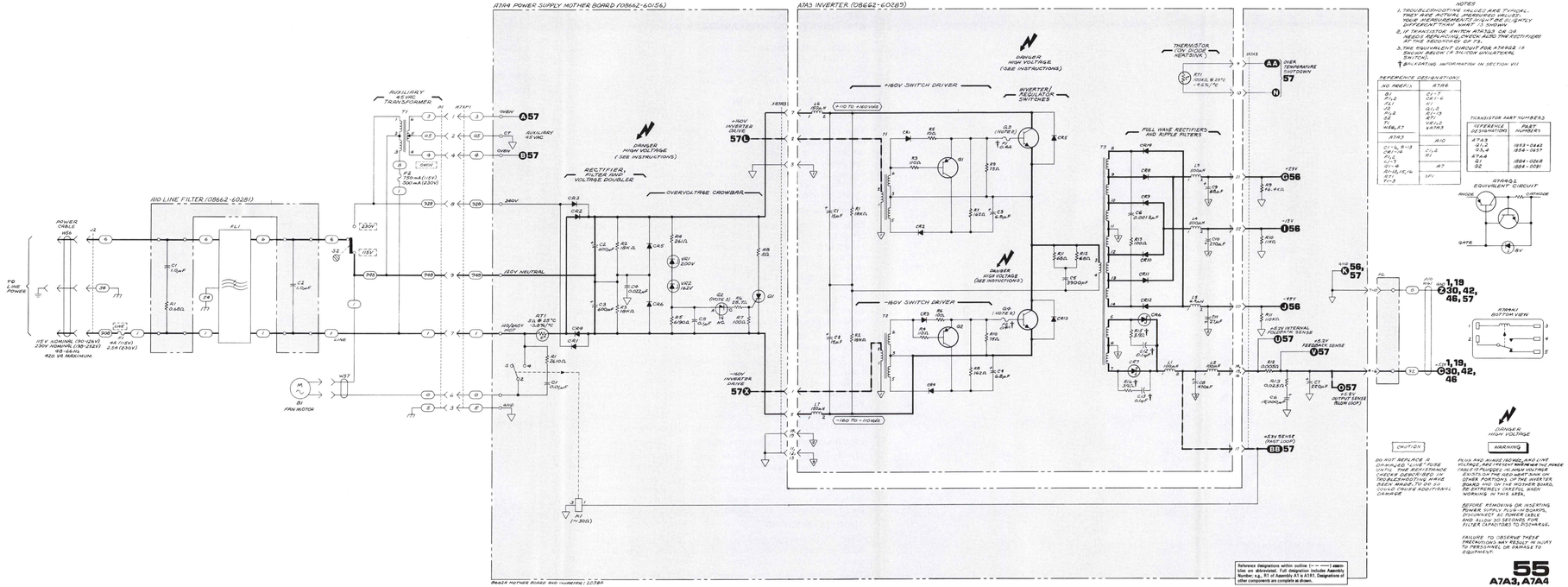


Figure 8-652. Power Supply Inverter, Mother Board, and Line Filter Schematics

SERVICE SHEET 56
A7A1 LINEAR REGULATOR ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram I
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The Linear Regulator board regulates the rectified and coarsely filtered dc voltages sent from the Inverter Board (service sheet 55). There are three series regulator circuits on this board, the outputs of which are +20 Vdc (at 2.5 amperes), −10 Vdc (at 2.5 amperes), and −40 Vdc (at 0.5 amperes). Additional features incorporated into the regulator circuits are foldback current limiting, transient and high input voltage shutdown, and bi-directional crowbar protection.

Linear Regulator Circuits

Each of the series regulators is designed around an integrated comparator amplifier (regulator). U1 and U2 are LM204 equivalents; U3 is a LM305 equivalent. A compound PNP/NPN transistor pair is used in each circuit to boost its current handling capability. Potentiometers R18, R20, and R39 are adjusted to trim the output voltages of the −40 Vdc, −10 Vdc, and +20 Vdc lines, respectively. Transistors Q11 and Q10 control the current limiting action of U2 and U1 in the −10 Vdc and −40 Vdc regulator circuits. Current limiting for the +20 Vdc line is sensed by a resistive divider formed by R23, R24, R27, and R28. Each regulator circuit has a green LED lamp which indicates that voltage is present at its output.

Bi-Directional Crowbar Protection

A crowbar circuit shunts the output of each of the three linear regulators found on this assembly. Each crowbar protects the circuitry fed by its respective regulator should the regulator fail. When the output of a regulation circuit exceeds its nominal output voltage by more than 3 to 4 volts, or falls more than one volt below ground (one volt above ground for the negative supplies), a triac is turned ON, shorting the output to ground. This puts the supply in a current-limit mode.

High Input Voltage Shutdown Circuitry

The high input voltage detector circuitry protects the regulators against excessive input voltage resulting from transients, open circuit conditions, or malfunctions in the switching-regulator circuitry. If the input line voltage even momentarily exceeds a preset value, the high input-voltage shutdown lamp will latch ON and a signal will be sent to the inverter-drive circuitry, shutting down the power supply.

TROUBLESHOOTING

When a power supply problem has been traced through the block diagram troubleshooting procedure to this assembly, use the procedure, below, to isolate the cause of the problem.

There are two basic types of problems that are covered by this procedure:

1. If red LED in the upper left hand corner of the board is lit indicating the input voltage from the A7A3 Inverter assembly was too high,

and the supply was shut-down, it is most likely a problem with the regulator not drawing enough current.
2. The input voltage is normal, but the output voltage is not regulated.

Inverter Input Voltage High

1. Disconnect the line cord from the rear panel of the 8662A.

CAUTION

Removing and installing power supply boards with the line cord plugged-in can damage these boards because high voltage is present whenever the line cord is plugged-in.

Install the A7A1 linear regulator assembly on its extender board. Then plug in the line cord.

If the red LED in the upper left hand corner lights when the line switch is turned on, continue troubleshooting with step 2. Otherwise, continue troubleshooting with step 3.

2. Connect a short jumper between the collector of Q16 and ground. This will allow the control board to turn-on. Turn the line switch to ON and measure the voltage at the test points in the table below, to identify which supply is malfunctioning.

Linear Regulator Inputs

Measure	Normal Voltage
TP4	< +30.0
TP5	< −16.0*
TP6	< −55.0*

*The < sign in this case means lower magnitude or more positive than.

When the malfunctioning supply is identified, troubleshoot the regulator circuitry to find the cause of the problem.

Inverter Input Voltage Normal

3. Turn the line switch to ON. To determine if any of the supplies are in current limit measure the voltage across the current sensing resistors specified in the table below.

Current Limiting Check

Resistor	Max Reading (Vdc)	Supply
R27, 28	1.25	+20V
R36	0.60	−10V
R37	0.60	−40V

If any reading is above the maximum value given in the table, that supply is current limited so continue troubleshooting with step 4. If the readings are normal, there is a problem with the regulator circuitry so troubleshoot to find the cause.

4. The supply could be in current limit because the load is drawing too much current or because the overvoltage crowbar has triggered. Turn the line switch to STANDBY and monitor the output of the supply being tested with an oscilloscope. Set the scope to trigger when the supply turns on and watch how high the voltage rises when the line switch is turned on. Compare this value to the numbers in the table below.

Crowbar Trigger Voltage

Supply	Crowbar Trigger Voltage
+20V	23.7V
−10V	11.0V
−40V	46.4V

If the actual supply voltage exceeded the trigger voltage, the regulator is defective so troubleshoot the regulator circuitry to find the cause of the problem. Otherwise, the load is drawing too much current so look for the problem in one of the other sections of the instrument.

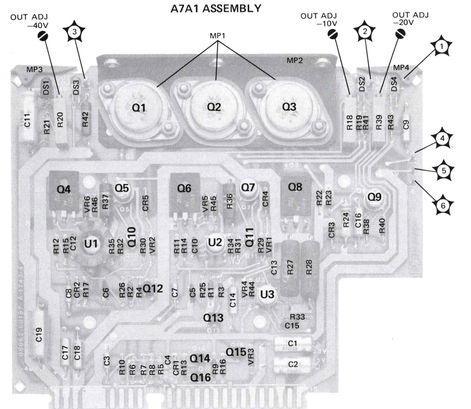
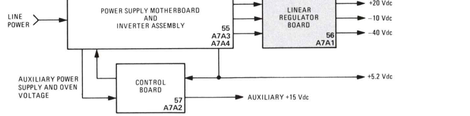


Figure 8-653. A7A1 Linear Regulator Component Locations



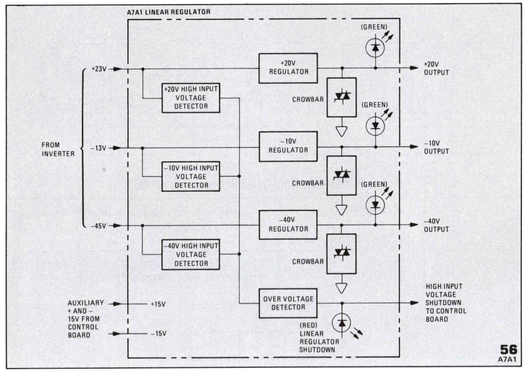


Figure 8-654. A7A1 Linear Regulator Block Diagrams

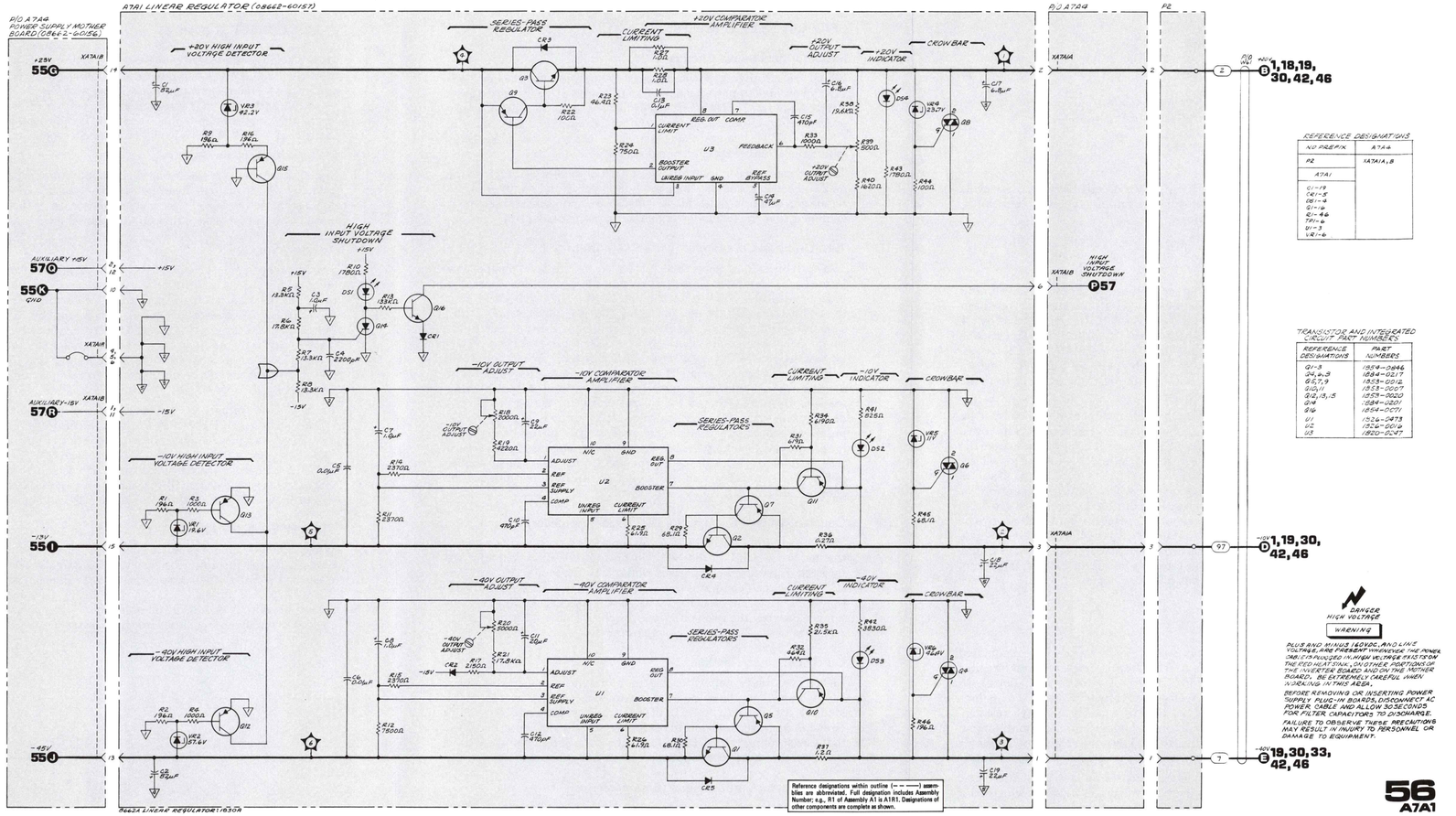


Figure 8-655. A7A1 Linear Regulator Schematic

SERVICE SHEET 57
A7A2 CONTROL ASSEMBLY

TROUBLESHOOTING HELP

Block Diagram I
Table 4-1. Abbreviated Performance Tests
Table 5-2. Post-Repair Adjustment Procedures

PRINCIPLES OF OPERATION

General

The Control Board contains the 40 kHz oscillator circuitry, duty-cycle control logic, inverter/regulator drivers, malfunction-disable circuitry, and auxiliary supply regulators.

Oscillator Circuitry

The switching frequency of the supply is established by a free-running multivibrator (U2) which generates a 40 kHz asymmetrical waveform having a 4:1 duty cycle (20 μs to 5 μs). The 2.5 MHz clock formed by U1 provides update clocking for flip-flops U4A and U4B. The 40 kHz generator is locked to a sub-multiple of the 2.5 MHz oscillator frequency by trigger pulses which reach pin 6 via C21. This assures synchronous operation of the two oscillators, eliminating spurs at the operating frequency of the synthesizer.

Within the pulse-width modulator (duty-cycle control logic formed by U6A and U6B), the 5 μs "off" period of the 40 kHz oscillator serves two functions. First, it alternates routing of turn-on trigger pulses from the turn-on level comparator (formed by Q15 and Q18) to the switching transistors. Second, it establishes a 5 μs "safety band" which disables both drive signals, assuring that both switching transistors are never turned ON at the same time. Any time during the 20 μs period, a drive signal can be started by a turn-on trigger pulse, but it will always be terminated at the next 5 μs period. The period of the drive signals depends on the position of the turn-on trigger pulse in the 20 μs frame. If it occurs early in the frame, the drive pulse will be wide. If it occurs late in the frame, the drive pulses will be narrow.

Duty Cycle Control Logic

The duty cycle control logic generates the pulse-width modulated signals that ultimately drive A7A3T3 (service sheet 55). This circuitry is composed of buffer flip-flops U4A and U4B, driver flip-flops U6A and U6B, and associated NAND gate circuitry (U5 and U7). Flip-flops U4A and U4B act as switching buffers between the duty cycle generator, loop gain amplifier, current foldback limiter, malfunction disable gate, and the driver flip-flops. They assure that control signals to the driver flip-flops are synchronized to occur at the proper times.

The pulse-width modulator circuitry is set up in a quad-state logic arrangement. U4B disables the ± 160 volt driver flip-flops whenever it changes state. U4A enables one of the two driver flip-flops whenever it changes state, but never allows both flip-flops to turn on at the same time. Furthermore, no driver flip-flop is allowed to turn ON twice in a row.

SERVICE SHEET 57 (Cont'd)

Fast and Slow Sense Circuits

Whenever a change in power demand occurs, the fast and slow loops effect a change in power delivered to the input of T3 by varying the duty cycle of the 20 kHz inverter. The fast sense circuit is a direct duty cycle modulated loop which turns the level comparator (Q15 and Q18) ON and OFF for fast and slow reactions to load changes; it also helps to diminish the 120 Hz component on the +5.2 volt line.

The slow sense circuit is an analog loop which senses the output of the +5.2 volt section. The slow loop provides precise (and relatively slow) regulation of the output, while the fast loop handles faster regulation demands. (See the two following circuit descriptions.)

Turn-On Level Comparator (Duty Cycle Trigger)

The turn-on trigger pulses are generated by the level comparator formed by Q15 and Q18. This circuit compares the fast sense line at the junction of the first L-C filter on the +5.2 volt line (service sheet 63) with the dc reference voltage obtained from the loop gain amplifier (U9). The voltage on the +5.2 volt fast sense line has a triangular ripple component which slopes positively when a switching transistor is ON and negatively when both transistors are OFF. When the sense voltage falls slightly below the reference voltage, the comparator generates a turn-on trigger pulse. Immediately, one of the switching transistors turns ON and the output starts to rise again. If load demands increase, the sensed voltage drops more rapidly, the trigger pulses are generated earlier, and the switching transistors stay ON for longer periods to supply the increased power demand. Conversely, a reduced load lengthens the negative slope, causing the turn-on trigger pulses to occur later, and the switching transistors conduct for shorter periods.

Constant Voltage Comparator (Loop Gain Amplifier)

To improve regulation of the +5.2 volt supply, losses occurring betwee. the fast sense point on the +5.2 volt line and the final dc output are factored into a level comparison voltage by the loop gain amplifier (U9). This circuit compares the +5.2 volt zener reference voltage with the +5.2 volt output slow loop sense line (service sheet 55). Any difference between the two voltages is amplified, slowly varying the dc reference to the turn-on level comparator.

Current Foldback Limiter

The current limit comparator (U8) monitors the output current of the supply by sensing the voltage drop across R12 (service sheet 61). If the load current exceeds a preset limit (due to a short-circuit condition) the circuit is energized and acts to reduce the dc reference voltage applied to the level comparator. This in turn causes the output voltage to drop to a level that holds the supply current at a maximum of 3 amperes.

Stabilizing Waveform Shaper (Exponentiator)

The exponentiator (U10) generates a limit-cycle-regulation waveform which is applied to the base of Q18 in the level comparator. If the output of U6A were HI and duty cycle control logic was producing a duty cycle of less than 50% at the 40 kHz rate, the system would become

SERVICE SHEET 57 (Cont'd)

unstable and oscillator U2 could be forced to drop to 20 kHz operation (resulting in a 10 kHz switching rate). Summation of the output of the stabilizing waveform exponentiator shaper with the +5.2 volt slow loop sense line at the base of Q18 causes the trip point of the comparator to be changed just enough to make sure that comparison is made at 40 kHz rather than 20 kHz as would otherwise happen.

Malfunction Disable Gate

Signals from the overvoltage and overtemperature detector circuits are gated by U5B to disable the inverter drive circuitry whenever a shutdown condition arises. This results in power being turned off to all parts of the system except those powered by the auxiliary supply.

Auxiliary Supply

The auxiliary supply circuitry receives 45 Vac from transformer T1 (service sheet 55) located within the power supply on the rear panel of the Signal Generator. The ac is rectified, producing a dc voltage that powers the A8A3 Reference Oscillator oven and drives the ± 15 volt regulators. CR1 through CR4 form a bridge rectifier which produces a positive and a negative voltage with reference to ground. The front panel line switch has no effect on this circuitry and these voltages will be present whenever the Signal Generator is connected to the ac power lines.

When the line switch is in the STANDBY position, Q6 is ON, turning Q7 OFF. When Q7 is OFF, Q3, Q4, and Q5 are also OFF, shutting down the ± 15 volt supplies. When the line switch is turned ON, Q6 turns OFF and allows current (flowing through Q8) to turn ON Q7 and thus turn ON Q3, Q4, and Q5, which brings up the ± 15 volt supplies. If the ac line voltage decreases, a point will be reached where Q8 is biased OFF. This will turn OFF Q7, which shuts down the ± 15 volt supplies.

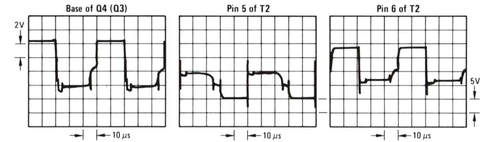
TROUBLESHOOTING

When a power supply problem has been traced through the block diagram troubleshooting procedure to this assembly, use the following procedure to find the defective component. Problem symptoms can be divided into two classes:
1. No pulses at TP6 and TP7 (shutdown).
2. +5.2 V supply not regulated (too high or too low).

SERVICE SHEET 57 (Cont'd)

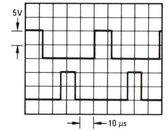
No Pulses at TP6 or TP7.

Check	Normal Condition	If Abnormal,
1. Edge connector A7A2 pin 9	+15.0 ± 1.0 Vdc	Troubleshoot auxiliary supply.
2. Edge connector A7A2 pin 8	−15.0 ± 1.0 Vdc	Troubleshoot auxiliary supply.
3. U1 pin 5	CMOS logic high (+10 Vdc)	Either the overtemperature or 5.2V overvoltage detector has triggered. The overvoltage detector is the most likely. Remove Q9. If U1 pin 5 is still low, Q19 has triggered which means the +5.2 V supply voltage went above 6V. This is an indication that the A7A2 Control board is not regulating properly. If the overtemperature detector has triggered, determine if the detector circuitry is faulty or if the heat sink on the A7A3 is really overheating. Turning the instrument off for awhile will cool everything and the detector shouldn't trigger when the instrument is first turned on.
4. Waveforms on TP2, TP3, TP9	As shown in the figure below	Troubleshoot the digital circuitry which produces these waveforms.



Maximum Duty Cycle Generator Waveforms

5. U5 Pin 5	COMS logic high (+10 Vdc when 5.2 V supply = 0)	Comparator circuitry is defective. Continue troubleshooting in the +5.2 V supply.
6. Waveforms on U7 pins 3 and 11	As shown in the figure below	The problem is in the duty cycle control logic. Inputs are correct and outputs defective.



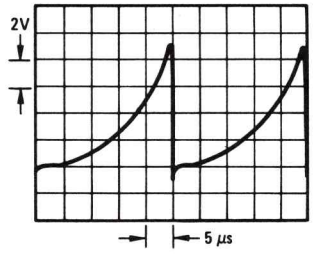
Duty Cycle Control Logic Outputs

7. At this point if there are no pulses on TP6 and TP7, the problem is in the inverter/regulator drivers on A7A2 or the switch circuits on A7A3. Remove the line cord and then remove the A7A3 assembly from the power supply. Now the waveforms at TP6 and TP7 should be like the waveforms in Figure 2 except amplitude should be +15 V. If there are still no waveforms, the drive circuits are defective. If the waveforms are there now, the problem is in the switch circuitry on A7A3. So continue troubleshooting with service sheet 55.

SERVICE SHEET 57 (Cont'd)

5.2 V Supply Not Regulated

1. Turn the line switch to STANDBY, remove the power cord, and remove the A7A3 Inverter assembly from the power supply.
2. Remove the bottom cover from the 8662A. Remove the small pc board that connects the wiring harness to the power supply motherboard. This disconnects the power supply from the rest of the instrument.
3. Install the A7A2 control board on its extender board. Connect a jumper from TP8 to ground (the top (negative) leads of capacitors C3, 4, 9, 10 in the center of the board make good ground points). Having this jumper connected is the same as turning the line switch on.
4. Set an adjustable power supply to 5.2 ±0.1 Vdc and connect the "+" terminal to TP1 and the "–" terminal to ground on A7A2.
5. Plug-in the power cord and follow the procedure in the following table.

Check	Normal Condition	If Abnormal,
1. Q17 Emitter	>5.4 Vdc	Current foldback limiter circuit is defective. No current should be flowing through the current sensing resistor on A7A4 so U8 should produce a positive output.
2. U9 Pin 3	5.20 ± 0.02 Vdc	If the voltage is between 4.6 and 5.8 Vdc, adjust the 5.2V supply pot to bring the voltage into spec. If the voltage is not close or cannot be adjusted, troubleshoot the reference circuit to find the cause of the problem.
3. Waveform on TP11	As shown in the figure below	There is a problem with U10 or associated circuitry.
	 Exponentiator Waveform	
4. Set power supply connected to TP1 ≤5.10 Vdc		
U9 pin 6	>13.0 Vdc	Loop gain amplifier defective.
U4 pin 5	CMOS logic high (+10 Vdc)	Comparator circuitry defective.
5. Set power supply connected to TP1 ≥5.30 Vdc		
U9 pin 6	< 0V	Loop gain amplifier defective.
U4 pin 5	CMOS logic low (0V)	Comparator circuitry defective.

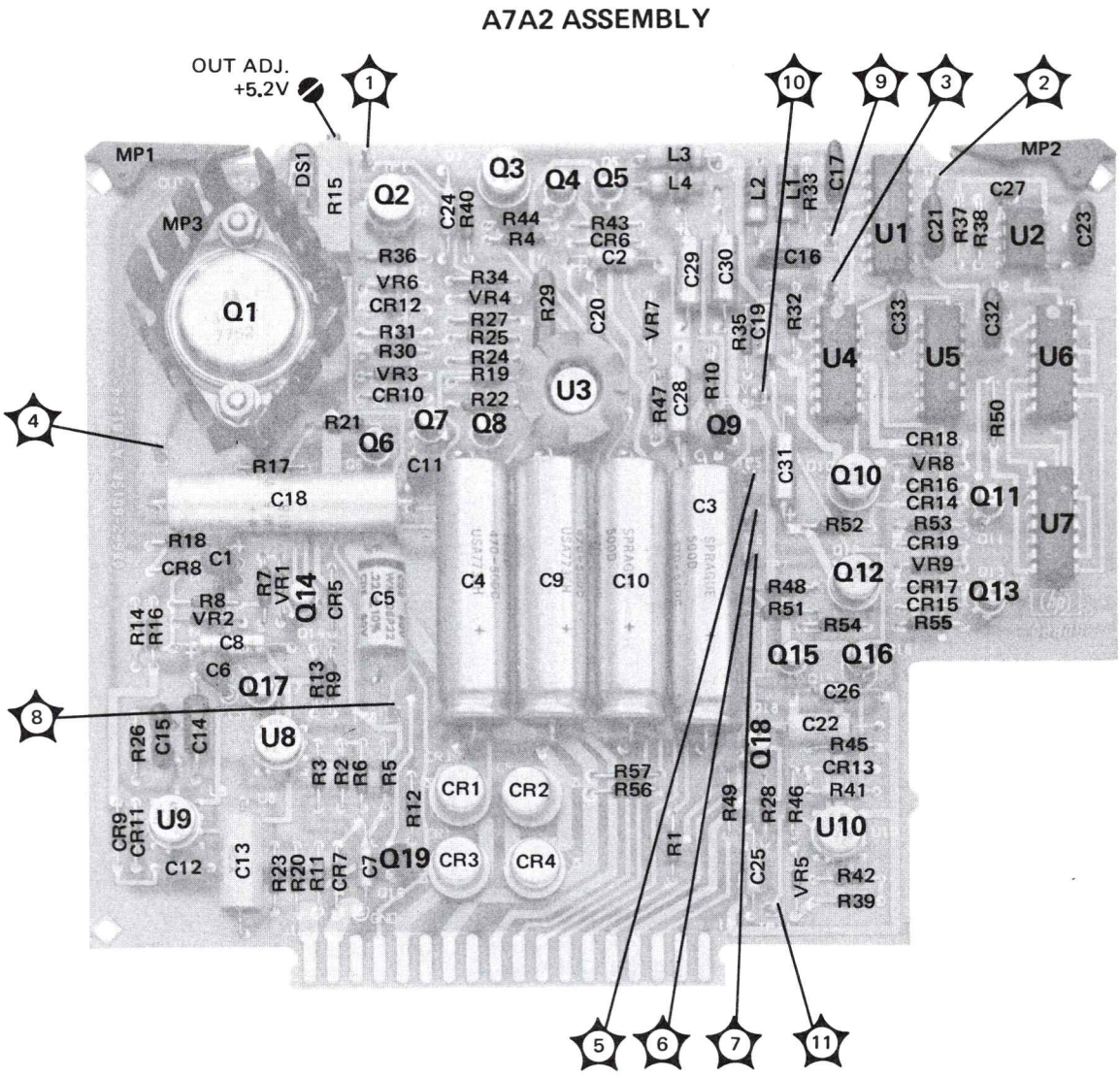


Figure 8-656. A7A2 Control Board Component Locations

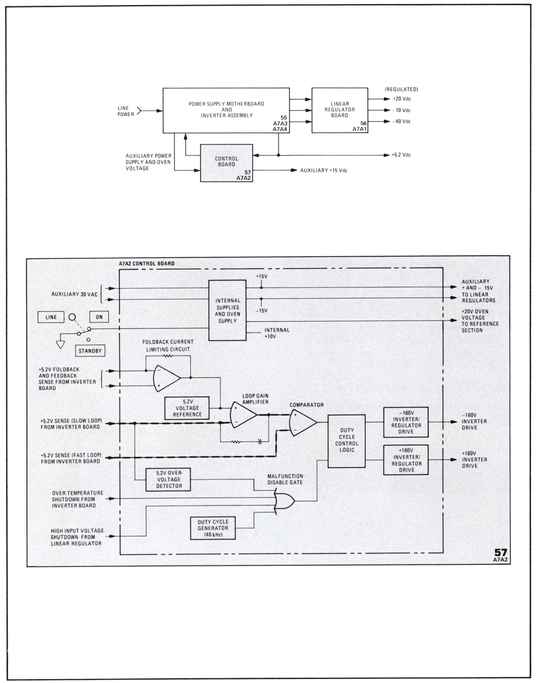


Figure 8-657. A7A2 Control Board Block Diagrams

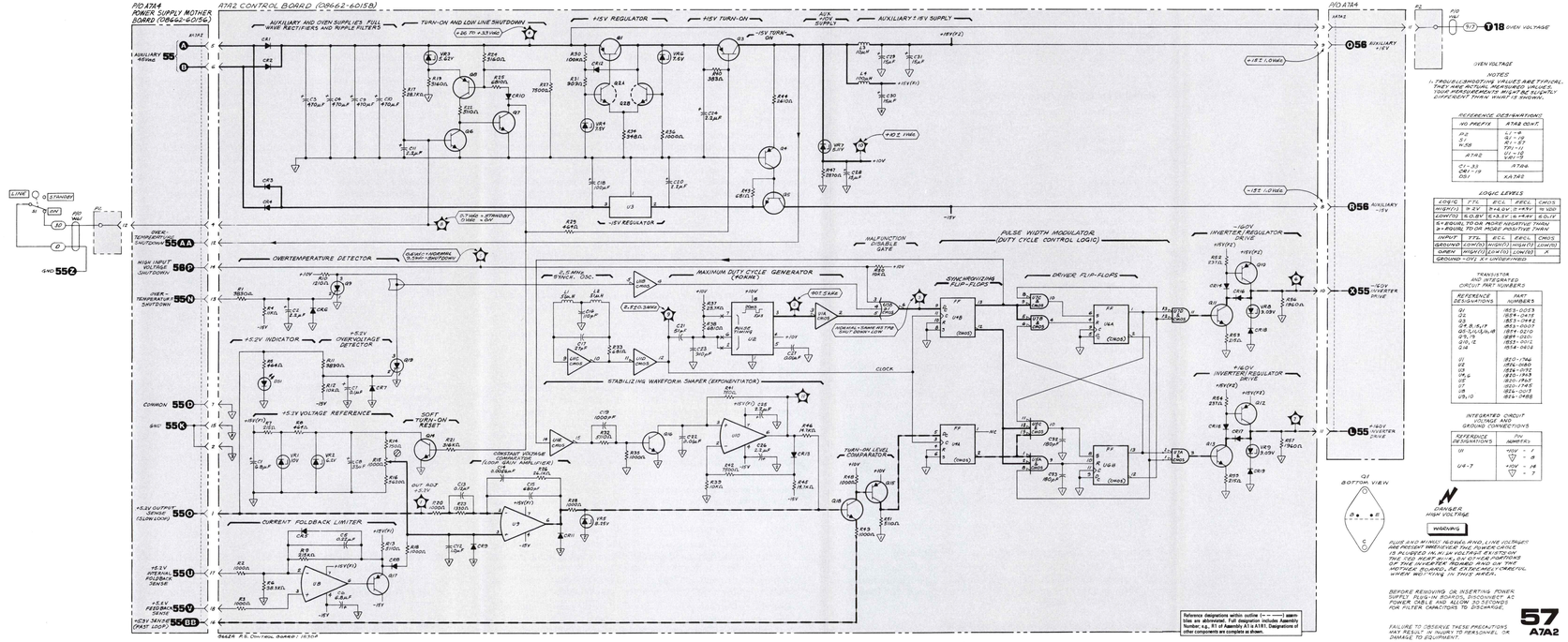


Figure 8-658. A7A2 Control Board Schematic

DISASSEMBLY PROCEDURES

General

This section provides the disassembly and removal procedures necessary for troubleshooting and parts replacement for the signal generator.

Removal Of Top And Bottom Covers

1. Remove the four feet at the back of the instrument.
2. To remove the top cover, remove the screw on the back panel that is located midway between the top two feet (near the top edge of the instrument).
3. Slide the top cover straight off, towards the rear.
4. Remove the two RFI gaskets from the channels in which the side edges of the top cover rests (when in place).
5. To remove the bottom cover, turn the instrument over so that the top side of the instrument is facing down. Remove the screw on the back panel that is located midway between the two bottom feet (near the bottom edge of the instrument).
6. Slide the bottom cover straight off, towards the rear.
7. Remove the two RFI gaskets from the channels in which the side edges of the bottom cover rests (when in place).

Extension (And Lowering) Of The Front Panel

1. Remove the plastic trim strips at the top and bottom front edges of the instrument; place screwdriver tip into the slots near the end of the trip strip and lift up.
2. Remove the four screws (two on the top edge and two on the bottom edge) from the channels previously covered by the trim strips.
3. Pull the front panel outwards (towards the front) and down. The following is a list of methods you can use to pull the front panel out.

CAUTION

Don't attempt to pry the front panel outwards, from the front, by placing a screwdriver in the gap which runs around the perimeter of the front panel. That is, don't place a screwdriver between the front panel and the chassis frame and try prying the front panel out. This may fracture or otherwise cosmetically damage the front panel.

a) Hold the sides of the main front panel keyboard and pull, firmly, straight out.

b) If you need a better grip, try pulling the RF connector.

c) If you can't pull out the front panel using either one of the two methods described above, you can push on the guide mechanism (attached to the front panel, inside the instrument) and force the front panel outwards.

Disassembly Procedure For The Rear Panel

It should be pointed out that the rear panel disassembled view drawing (figure 8-659) used in conjunction with the following disassembly procedures is only for referencing various parts and assemblies discussed in those procedures. It is not meant to serve as a comprehensive component locator. Section #6 contains a copy of this drawing, which has been marked up so that it can be used to determine the relative locations and reference designators of various parts and assemblies.

DISASSEMBLY PROCEDURES (Cont'd)

Removal Of Reference Oscillators (19, 20 & 22) And Reference Assembly Casting (21)

The Reference Assembly casting (21) contains the 10 MHz Reference Oscillator (20), the Output Sum Loop VCO (19), and the Reference Sum Loop VCO (22). Any one or all of these three oscillator blocks can be removed from the casting. The Reference casting itself can also be removed, if necessary. In order to remove anything associated with the Reference Assembly, use the following procedures.

Removal of Reference Oscillator (20). The 10 MHz Reference Oscillator and the pc board lying immediately to the right of it (which contains the three pushbuttons and two BNC jacks) can be unplugged and removed from the Reference Assembly casting once the Reference Oscillator cover (3) and metal RFI gasket is removed. To take off the cover, unscrew the six screws which hold it in place. (4) is one of these six screws.

Removal of RS and OS Loop VCOs (19 and 22). There are four screws holding the RS and OS Loop VCO cover in place. (2) is one of these four screws.

1. Remove the RS and OS Loop VCO cover (1) and metal RFI gasket.
2. Remove all plugs and cables connected to the VCOs.
3. Both VCOs are fastened to a bracket which is held in place within the Reference casting by three screws near the inside back of the casting. These screws are visible and accessible from the rear of the instrument (but are not shown in the drawing) and can be removed with a medium sized phillips screwdriver. One of the three screws in the gap between the top of the OS Loop VCO and the Reference casting; the other two screws are located in the gap between the RS and OS Loop VCOs.
4. Once the three bracket screws have been removed you can pull the RS and OS Loop VCOs free of the instrument.

Removal of Reference Casting (21). In order to get at the feedthru capacitors (24) which are located in the left-hand side of the Reference Assembly, the entire Reference Assembly casting must be removed.

1. Remove the top and bottom covers of the instrument.
2. The only way the casting can be removed from the instrument is to slide it out of the right-hand side of the instrument (looking from the front). In order to do this, the right side strap and paneling must first be removed. To remove the side strap, take out the two screws (one at each end of the strap) which hold the strap in place.
3. Rest the instrument on its left side. Remove the screws which hold the right side rails to the front and back panels (as well as the internal assemblies) of the instrument. Between the two rails, about 30 screws in all must be removed. Once these screws are out, the side rails should come right off.

DISASSEMBLY PROCEDURES (Cont'd)

4. Take out the three screws (15, 23 and 25) and unscrew the cable clamps which hold down the wires leading from the mainframe of the instrument to the OS and RS Loop VCOs (which run over the top of the Reference Assembly casting (21). Once these clamps have been removed, slide the casting sideways (to the right, looking from the front) and pull it out of the instrument. Pulling this assembly out will not be easy. It rubs against several different parts and must be pulled out slowly.

NOTE

During re-assembly of the Reference Assembly casting, several things must be noted. First, when replacing the RS and OS Loop VCOs (19 and 22), you may have trouble replacing the three screws which hold these two VCOs to the bracket near the back of the Reference Assembly casting. They can be very difficult to replace unless a magnetic screwdriver is used or unless the screws are in some other manner temporarily fastened to the end of the screwdriver (try tape or some type of plastic tubing to hold the screw to the tip of the screwdriver).

When replacing the 10 MHz Reference Oscillator cover (3) and RS and OS Loop cover (1), the metal RF gasket must be laid in place first. Keeping these gaskets aligned with the Reference casting holes while putting the covers in place is difficult. Re-inserting the screws is even more difficult. Don't use tape or glue to hold the gasket to the cover while fastening the cover in place. The RFI gaskets are designed to prevent leakage of RF. If tape or glue is applied to them, then they become less effective at preventing the leakage of RF. Standing the instrument on end with the front panel facing downward (you will have to set up some sort of arrangement so that the front panel is not actually resting on the table top) will enable you to lay the gasket in place. Once the gasket is lying flat, the back cover can then be put in place. Getting the first screw in place to hold the cover down is difficult. Take your time. Move the cover and the gasket around until the holes line up and the screw falls into place. Do the same thing with the second screw. It should be easier to get in. The other remaining screws should fall into place with less effort.

Removal Of Fan (16)

1. Remove the fan cover (6).
2. Remove the fan.
3. Disconnect the ground wire at the chassis (26); disconnect the power line cord.
4. When re-installing the fan, be sure that the metal and rubber washers are placed on the studs before the nuts (5) are screwed on and tightened down. Don't over-tighten the nuts. The rubber washers act as shock mounts for the fan. If the nuts are over-tightened, they become ineffective.

Removal Of HP-IB Interconnect Assembly (29)

1. Remove the fan cover (6).
2. Remove the bottom cover of the instrument.

DISASSEMBLY PROCEDURES (Cont'd)

3. Remove the plugs connected to the underneath side of the HP-IB Interconnect board (29).
4. Remove the two screws holding the HP-IB Interconnect assembly in place. You will find one screw at either end of the HP-IB jack, just below the hex nuts. (30) is one of these screws. Once these screws have been removed, the HP-IB Interconnect assembly can be pulled straight out from the back of the instrument.

Removal Of Power Supply Assembly (50)

1. Remove the top and bottom covers of the instrument.
2. Remove the line filter and auxiliary transformer cover (8) at the rear panel of the instrument.
3. Remove the standoffs into which (9) and (10) were screwed. (17) is one of these standoffs.
4. Remove screws (48) and (49) at the right of the line filter assembly (looking from the rear).
5. Looking from the top of the instrument, remove screws (44) and (45). These screws hold the power supply module to the 'tongue' (which is fastened to the middle of the back panel of the instrument).
6. Remove the carrying strap and side panel from the left-hand side (looking from the front) of the instrument. To remove the strap, you must take out two screws (one at either end of the strap) which hold the strap in place.
7. Remove the last two screws holding the power supply module in place. The first screw is found in the top rail, five holes from the rear of the instrument. The second screw is in the bottom side rail, five holes from the rear of the instrument.
8. Before the power supply can be removed, the main harness near the bottom of the module must be unplugged. Once this harness is unplugged, the power supply module can be removed.
9. Remove the power supply module by pulling it straight down through the bottom of the instrument. It should be noted, before you begin pulling on the assembly, that the power supply is still connected to the instrument at the plastic connector (46). Rock the module back and forth as you pull it out of the instrument. This will make removal much easier.

NOTE

The plastic connectors must fit together properly when the power supply module is put back into the instrument. Don't push the assembly back in hard until you are sure that the connector halves are properly matched.

Removal Of Line Filter Assembly (13) And Line Filter Capacitors (18)

1. Remove the line filter and auxiliary transformer cover (8) by unscrewing (9) and (10) and loosening (11) and (12). The silver can (13) underneath the cover is the line filter assembly; the pc board (18) underneath it contains additional filter capacitors.
2. The line filter assembly is fastened to the instrument and pc board beneath it by two nuts, one at the top end of the line filter and one at the bottom end. (31) is one of these nuts. Remove these nuts with a

Power Supply Control Board A7A2 SERVICE SHEET 57

DISASSEMBLY PROCEDURES (Cont'd)

nut driver. The line filter can is electrically connected to the pc board by four wires, two of which are soldered to the upper end of the pc board, and two of which are soldered to the bottom. To replace the line filter assembly (can) or get at the pc board to replace the capacitors on it, these four wires must be unsoldered.

3. In order to unsolder the four wires which run from the line filter to the pc board, it is necessary to lift the line filter and pc board (as a unit) high enough so that you can get a soldering iron underneath the pc board. This can be made easier by unfastening the BNC connector panel. See "Removal Of BNC Connector Panel". When lifting the assembly, care must be taken not to pull or lift too hard.

NOTE

When re-installing a new line filter block, the two brown wires and two blue wires which get soldered to the pc board should be cut to about 2" in length before being soldered to the pc board, the pc board must be pulled high enough to get the soldering iron underneath it. Once the wires are reconnected, the pc board and line filter can be bolted down.

Removal Of Auxiliary Transformer (31)

1. Remove the top cover of the instrument.
2. Remove the line filter and auxiliary transformer cover (8).
3. Remove the cover panel (42) by taking out screws (41) and (43). This exposes the wires at the back side of the transformer. Before changing the transformer, wires from the old transformer must be unsoldered. It is a good idea to write down where each wire is connected, as they are unsoldered, for later reference.
4. Remove the auxiliary transformer (31) by unscrewing the four screws holding it in place. (32) is one of these screws.

Removal Of BNC Connector Panel (40)

1. Remove the line filter and auxiliary transformer cover (8).
2. Unscrew (37), (38), and (39). This provides full access to the back side of the assembly, enabling the connectors to be replaced.

Removal Of Power Cord Panel (34)

1. Remove the line filter and auxiliary transformer cover (8).
2. Unscrew (33), (35), and (36). This provides full access to the back side of the assembly, enabling replacement of parts.

NOTE

Both the line power jack and voltage selection switch are riveted in place on this panel. Should they require replacement, they can be drilled out and replaced with new parts. These new parts can be either re-riveted or bolted in place, whichever is easiest.

Removal Of RF (Opt. 001) Connector (27)

1. Remove the fan cover.
2. Unscrew the nut from the rear end of the RF connector and pull it out (to the rear) of the instrument.

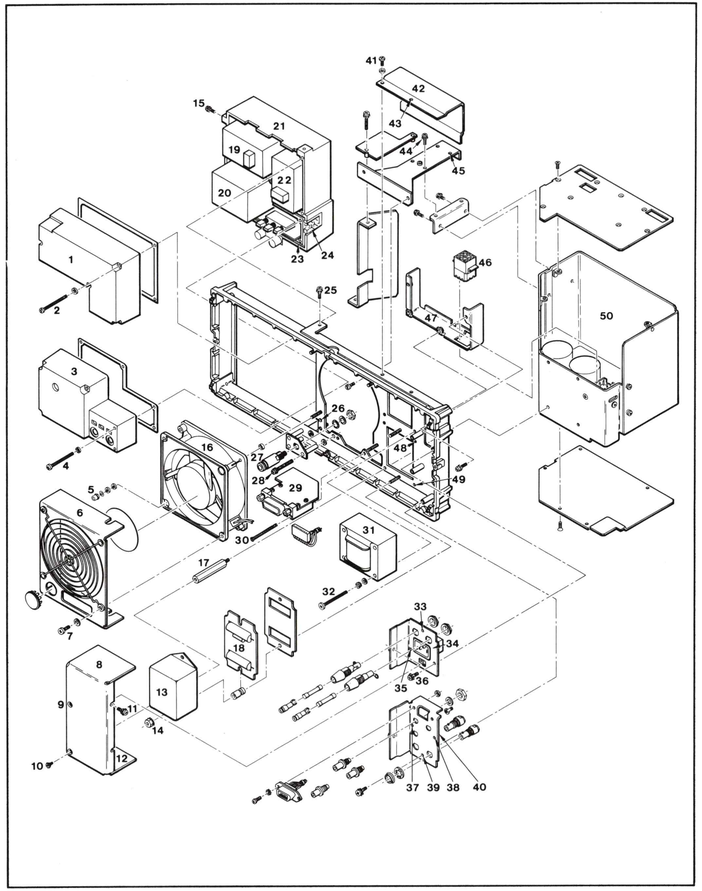


Figure 8-659. Signal Generator Rear Panel Exploded View

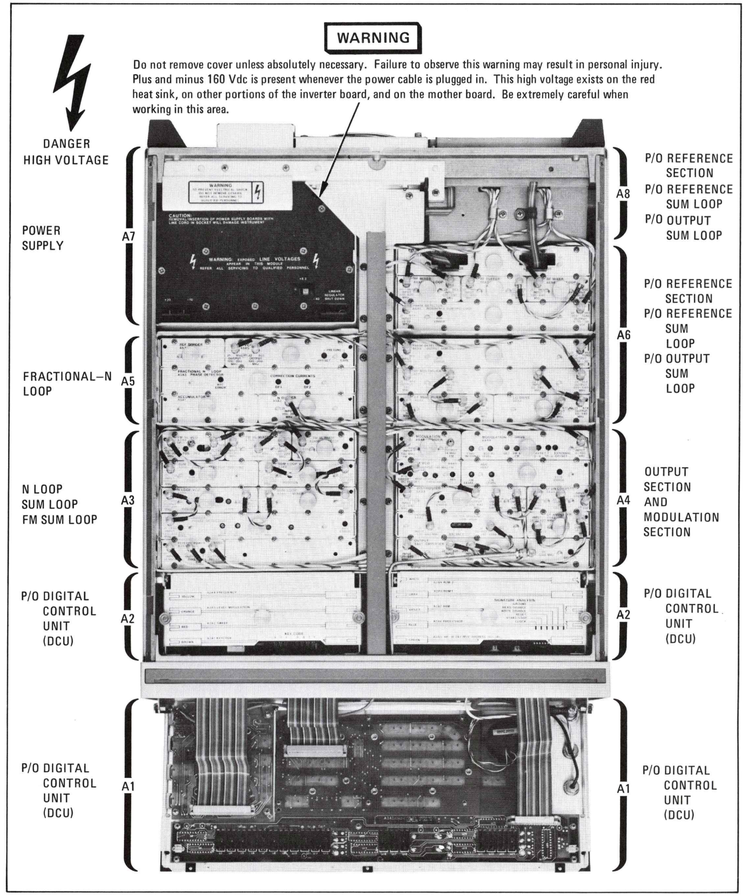


Figure 8-660. Signal Generator Top Internal View

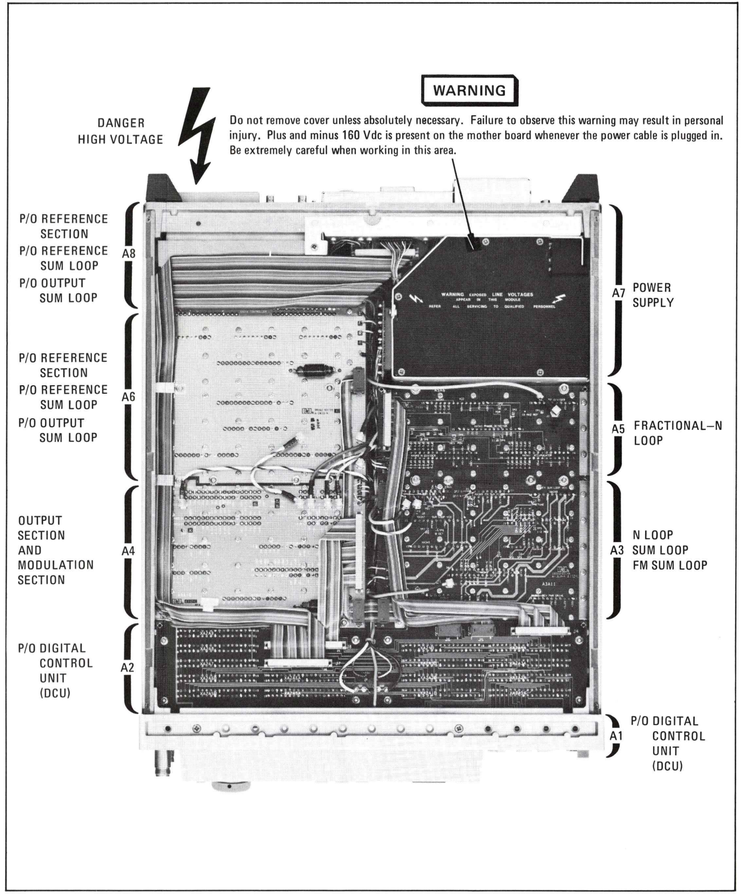


Figure 8-661. Signal Generator Bottom Internal View

Top and Bottom Internal Views and
Disassembly Procedures

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ADDRESS

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MODEL NO. SERIAL NO.

MODEL NO. SERIAL NO.

P.O. NO. DATE

Accessories returned with unit

☐ NONE ☐ CABLE(S)

☐ POWER CABLE ☐ ADAPTER(S)

OTHER

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TECHNICAL CONTACT PERSON

PHONE NO. EXT.

MODEL NO. SERIAL NO.

MODEL NO. SERIAL NO.

P.O. NO. DATE

Accessories returned with unit

☐ NONE ☐ CABLE(S)

☐ POWER CABLE ☐ ADAPTER(S)

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COMPANY

ADDRESS

TECHNICAL CONTACT PERSON

PHONE NO. EXT.

MODEL NO. SERIAL NO.

MODEL NO. SERIAL NO.

P.O. NO. DATE

Accessories returned with unit

☐ NONE ☐ CABLE(S)

☐ POWER CABLE ☐ ADAPTER(S)

OTHER

over

HEWLETT PACKARD

Should one of your HP instruments need repair, the HP service organization is ready to serve you. However, you can help us serve you more effectively. When sending an instrument to HP for repair, please fill out this card and attach it to the product. Increased repair efficiency and reduced turn-around time should result.

COMPANY

ADDRESS

TECHNICAL CONTACT PERSON

PHONE NO. EXT.

MODEL NO. SERIAL NO.

MODEL NO. SERIAL NO.

P.O. NO. DATE

Accessories returned with unit

☐ NONE ☐ CABLE(S)

☐ POWER CABLE ☐ ADAPTER(S)

OTHER

over

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over

Service needed

☐ CALIBRATION ONLY

☐ REPAIR ☐ REPAIR & CAL

OTHER _____

_____

Observed symtoms/problems

FAILURE MODE IS:

☐ CONSTANT ☐ INTERMITTENT

SENSITIVE TO:

☐ COLD ☐ HEAT ☐ VIBRATION

FAILURE SYMPTOMS/SPECIAL CONTROL SETTINGS_____

_____

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_____

If unit is part of system list model number(s) of other interconnected instruments. _____

_____

9320-3896 Printed in U.S.A.

Service needed

☐ CALIBRATION ONLY

☐ REPAIR ☐ REPAIR & CAL

OTHER _____

_____

Observed symtoms/problems

FAILURE MODE IS:

☐ CONSTANT ☐ INTERMITTENT

SENSITIVE TO:

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FAILURE SYMPTOMS/SPECIAL CONTROL SETTINGS_____

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